The Dissertation Committee for Xin Wang certifies that this is the approved version of the following dissertation:

Interference Cancellation in Broadband Wireless Systems Utilizing Phase Aligned Injection-Locked Oscillators

Committee:

Ranjit Gharpurey, Supervisor

Jacob Abraham

Arjang Hassibi

Adnan Aziz

Venkatramanan Raman

Interference Cancellation in Broadband Wireless Systems Utilizing Phase Aligned Injection-Locked Oscillators

by

Xin Wang, B.S., M.S.E.

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Dedication

To my wife Sen Sun, my daughter Ashley, my son Derek,

my parents Zhaohua Hu and Guangji Wang,

and Sen's whole family

for their love and support

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Interference Cancellation in Broadband Wireless Systems Utilizing Phase Aligned Injection-Locked Oscillators

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Xin Wang, Ph.D.

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Supervisor: Ranjit Gharpurey

Linearity enhancement, especially within the front end of a wireless receiver IC design, is highly desirable since it allows the front-end to withstand strong interferers from co-existing communication standards or other wireless radiators. We propose an interferer suppression method based on feed-forward cancellation that uses an injection-locked oscillator (ILO) to extract the interferer from the incident spectrum. The technique is expected to be useful in environments where a strong narrowband interferer appears along with a wideband desired signal, such as ultra-wideband (UWB) and emerging cognitive-radio applications. The ILO is further embedded within a phase-locked loop which provides several advantages including ILO center frequency self tuning and automatic phase alignment between the main signal path and the auxiliary path. An IC that uses this approach is implemented in a UMC 0.18μm RFCMOS process. In measurement, the chip demonstrates 20dB suppression for phase and frequency modulated interferers while maintaining around 18dB power gain and noise figure below

5dB, measured with an off-chip balun for the desired signal. Techniques for canceling amplitude modulated interferers, though not included in the integrated circuit, were also demonstrated with an off chip amplitude control loop. Over 20dB rejection was obtained with AM interferers with properly scaled envelop signal applied to the ILO bias port. A second LNA was connected in cascade with the system to emulate the input stage of a down-conversion mixer and the cascaded P1dB was improved over 16dB with cancellation on. Gain compression above 13dB was also observed when auxiliary path was disabled, at the same input level as the P1dB with cancellation applied.

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Chapter 1: Introduction

The recent years have witnessed the advent of wireless systems with bandwidth and data rates of the same order as several wired communication systems. While cellular wireless systems were intended for basic voice services, recent wireless systems and standards, such as WiMax, WLAN and W-CDMA, are now capable of supporting high-speed data communications over a wide range. New wireless applications such as video over cellular phones continue to emerge.

With the ever increasing number of applications, the available wireless spectrum continues to become more crowded. This increase in spectrum usage can lead to serious coexistence and interference issues in all systems. When an interfering signal is incident at much higher magnitude than the desired signal it can prevent the desired signal from being correctly retrieved by the receiver device. Such signals are often referred to as jammers or blockers. The ability to detect a weak desired signal in the presence of a much stronger interferer is indeed one of the major challenges faced by radio frequency integrated circuit (RFIC) receiver designers. To understand how this challenge impacts receiver design, it is helpful to review a typical radio receiver.

1.1 A TYPICAL RECEIVER DOWN-CONVERTER

Many modern receivers rely heavily on digital signal processing (DSP) technologies and advanced algorithms to boost the signal to noise ratio (SNR) under severe conditions such as multi-path fading and strong interference, and hence feature significant processing complexity, unlike early radio receivers that were designed for analog modulation schemes such as frequency or amplitude modulation. Despite the increase in complexity in the baseband sections of the receiver, the front-end task of down-conversion from the high-frequency received at the antenna to a low-frequency that

is suitable for demodulation remains substantially unchanged. Several architectures can be employed for the purpose of down-conversion, such as super-heterodyne (also referred to as heterodyne), direct down-conversion receiver (DCR), and low intermediate frequency (IF).

In a heterodyne receiver, input RF signal is translated to an intermediate frequency (IF) before further processing. In modern radio designs, the signal at IF is further down-converted to baseband for digital processing, although in some cases extra down-conversion steps can be employed before reaching the final baseband around DC. In a two step heterodyne receiver, for example, the choice of IF frequency involves a trade-off between the ease of channel selection and image rejection, or a trade-off between selectivity and sensitivity. This trade-off can be explained as following: When the local oscillator (LO) signal is distant from the RF frequency, the image is also far and thus easy to reject, but the resulting IF frequency is high due to which the IF filter design poses a challenge. On the other hand, if LO is very close to the RF frequency, IF frequency is very low for easy IF filter implementation but the image rejection filter characteristic becomes very sharp and thus difficult to design. In many implementations, the selection of the IF is further constrained by the availability of low-cost filters for channel selection and image-frequency rejection.

Direct conversion receivers use an LO signal with the same frequency as the RF carrier, resulting in a one-step down-conversion to baseband. The requirement for image rejection from another signal is now replaced by the requirement to ensure that the baseband I and Q channels are properly isolated and do not leak into one another, which could happen due to gain mismatch in the down-conversion paths, and non-ideal quadrature between these paths. Typical in phase (I) and quadrature (Q) matching requirement is driven by signal to noise ratio (SNR) while requirement on selectivity is

set by adjacent or alternate channel rejection specification. High quality factor (Q) filters are possible in IC form using commercial silicon technology, and thus the required channel selectivity can usually be achieved without resorting to off-chip filters. It should be noted that the front-end still requires some broadband selectivity to prevent saturation due to distant jammers. On the negative side, DCR's have well known performance limitations set by DC offset, second order interception point (IP2) and flicker noise (especially in CMOS designs).

When the separation between the LO signal and input RF signal is of the order of the channel spacing (CS), the receiver structure is generally referred to as low IF. Depending on the blocker profile and adjacent/alternate channel interference levels, the low IF receiver may offer better compromise compared with its direct conversion counterpart because it has reduced sensitivity to DC offset and flicker noise. An added advantage is when interfacing with digital chips it is possible to employ only one signal channel compared with the I and Q interface for the DCR.

In this thesis we consider the problem of enhancing selectivity in the radio front-end, a problem that is common to several radio architectures. Without loss of generality, we therefore assume a direct conversion receiver structure for all analyses in this dissertation except when stated otherwise.

As shown in Figure 1, a typical RFIC receiver chain starts with a low noise amplifier (LNA) for the initial amplification of the input RF signal. The LNA can be either single stage or consist of multiple stages and is followed by a down-conversion mixer, which converts the RF signal to baseband around DC. This mixer can be implemented using multiple techniques, including active current commutating or passive switch-based designs. In fact, passive mixers are not uncommon for CMOS direct conversion receivers (DCR) due to inherently low flicker noise, which addresses one of

the critical DCR problems. However passive mixers provide much lower conversion gain. Two mixers are usually employed with quadrature LO clocks, to derive the I and Q paths. The mixers are typically followed by a combination of filtering and programmable gain amplifiers (PGA). It is very important to accompany each amplification step with some level of filtering in the receiver design to accommodate all signals (interference included) within the limited dynamic range. The amplified and filtered I and Q signals are then fed into an analog to digital converter (ADC) and then applied to the baseband digital processor.

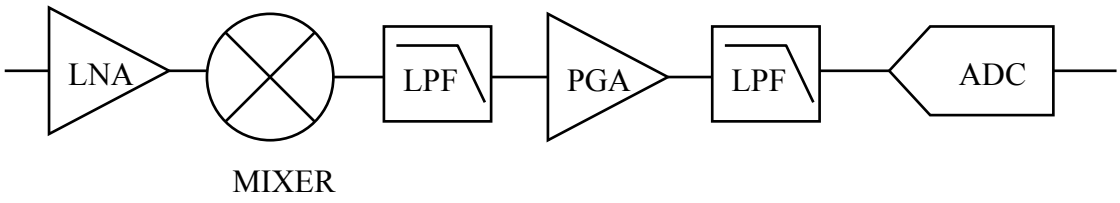


Figure 1: A typical RFIC direct conversion receiver (DCR) lineup. I and Q channels are not shown for simplicity.

1.2 INTERFERENCE IN VARIOUS SYSTEMS

Interferers can introduce distortion-related effects such as gain compression and inter-modulation, both leading to degradation of effective signal to noise ratio (SNR) of the desired signal, or more precisely the signal-to-noise and distortion ratio (SNDR). Interference signals can be either in band or out of band, where band generally refers to the frequency range occupied by all intended users of the system under discussion. The dynamic range of the receivers has to be made sufficiently large, such that the largest interferers do not degrade the effective SNR by an unacceptably large amount.

Each user can either occupy a dedicated channel within the band, or spread the information across the whole band in more advanced digital modulation schemes, such as direct sequence spread spectrum (DSSS), code division multiple access (CDMA), and orthogonal frequency division multiplexing (OFDM). In all cases, in band channels may also see interference from other users or other channels due to either finite adjacent channel leakage ratio (ACLR) or inter-modulation (IM) products. It is necessary to factor in all such in band interference effects during the system definition phase. In many cases these are well defined by the specific standard or regulation.

In the absence of interferers, the smallest signal which can be detected and demodulated while satisfying system performance metrics, such as bit-error-rate, is termed the sensitivity of the receiver. The sensitivity requirement directly relates to the noise figure of the receiver. In order to decrease the noise figure, that is to improve the sensitivity, it is usually necessary to use a large value of gain in the front-end of the receiver, namely in the mixer and the LNA. The upper limit on gain is set by the need to avoid compression in the presence of interference. As described in the next section, this introduces a fundamental trade-off between linearity and sensitivity. This trade-off poses an ever-increasing design challenge as the supply voltage of the technologies decreases with process scaling. The trade-off is of great significance in systems such as Ultra Wideband [1], since these systems are highly vulnerable to interference, owing to their large bandwidth.

1.3 LINEARITY BOTTLENECK

Referring to Figure 1 again, one can surmise that the key bottleneck for linearity in the RF down-converter is the mixer, since it is preceded by a non-selective front-end

low-noise amplifier, which amplifies the desired signal and interferers alike. The mixer linearity can be limited at its input or its output, depending on its gain. While there is normally no selectivity at the input of the mixer, a limited amount of passive low-pass filtering is usually applied at its output in several systems, such as GSM, W-CDMA and even multiband approaches to UWB, such as the WiMedia standard. This passive filter helps to reduce the level of out-of-channel interferers. For example, in the WiMedia standard, the LNA has to be broadband to cover over 7GHz, while the mixer output range only has to be around 264 MHz wide, which is half of the bandwidth of one of the fourteen sub-bands from the total 7GHz bandwidth. This allows passive filtering at the mixer load to attenuate any interferers that exist outside the desired sub-band and thereby relax the linearity, at the output of the mixer as well as at the input of subsequent active LPF blocks.

Since it is the mixer which poses the most severe constraint on non-linearity in the face of broadband interferers (both co-channel and out-of-channel or out-of-band), it is highly desirable to introduce a capability to attenuate interferers before the down-conversion, within the front-end.

1.4 INTERFERENCE AND BROADBAND WIRELESS

While any wireless receiver is ultimately constrained by interferers, in regards to its non-linearity, this problem is especially severe in emerging broadband wireless systems. Narrow-band receivers usually employ band-pass filters before the front-end LNA or between the LNA and the down-conversion mixers, to attenuate out-of-band interferers. However in the case of broadband wireless systems, even with some out-of-band rejection, the scope for in-band interferers from narrow-band jammers or other users is high. As mentioned above the UWB system represents one of the most challenging

cases for interferer rejection. This is due to two reasons. First, the desired signal may occupy the whole or any part of the 3.1 – 10.6 GHz frequency range. In multiband systems, for example the WiMedia system, the entire bandwidth is divided into fourteen 528MHz sub-bands shown in Figure 2. The front-end bandpass filter in such a case usually covers the entire 3.1-10.6GHz band, since current technology does not have good cost effective solutions for tunable selection of the 528MHz sub-bands. Second, the UWB uses unlicensed spectrum. By itself it is required to satisfy stringent FCC (standing for Federal Communications Commission) regulations on maximum power emission, so that it does not harm other systems. On the other hand, any narrow-band system within this bandwidth can appear as a large interferer at the UWB front-end. We use the problem of interference in such systems as the motivator for the architecture of interference detection and rejection as presented later.

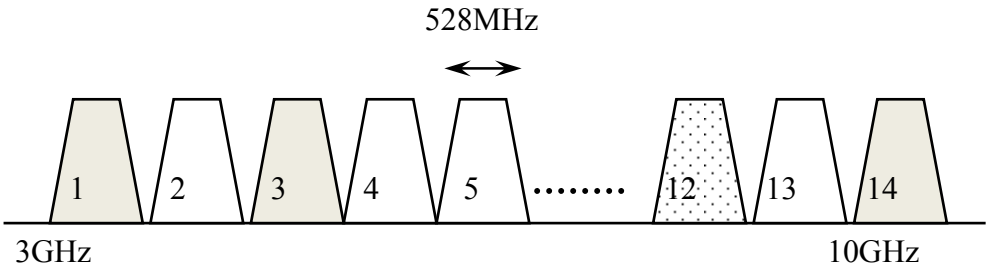


Figure 2: MB-OFDM UWB sub-bands lineup. Each sub-band occupies about 528MHz of spectrum.

In a multiband UWB system, interferers can either appear within a sub-band or outside the sub-band. One approach to address interference in such systems is to detect large interferers, and use only those sub-bands where the interference levels are below a

threshold (e.g., the dotted sub-band 12 in Figure 2). Hsieh et al. [2] reported an algorithm to quickly detect which one of the fourteen sub-bands has strong interference in 2006.

1.5 PROBLEM STATEMENT

As a summary for this chapter, the problem statement of this research project is presented as following: Assuming that a wideband desired signal is accompanied by a much stronger narrowband interference signal, this research seeks to provide an effective on chip mitigation to suppress the interference signal significantly while keeping the impact minimal on the desired one. A CMOS technology is employed in this work, as it is the technology of choice in many commercial applications, especially for SOC implementations.

We will use the multiband UWB system (such as the WiMedia system) as the system template for this work. Another assumption to start with, as discussed in the last section, is that the interferer lies out of the sub-band. As will be shown later, the proposed solution is indeed capable of suppressing the interference signal regardless where it locates relative to the desired signal's spectrum. The level of noise floor degradation to the desired signal will become the dominant concern. As a result, sensitivity level and system SNR requirement have to be considered besides linearity alone.

Chapter 2: Review of Existing Approaches

A wide variety of interference mitigation efforts have been reported for different application types and modulation schemes. In this chapter we provide an overview of prior work.

2.1 FIXED NOTCH FILTERS

One notable challenge for UWB designers comes from the currently popular 5GHz UNII band wireless LAN (the IEEE 802.11a standard) applications. The potentially strong signal levels generated by these base stations as well as clients may easily get much stronger than the WiMedia signals and pose linearity issues at the receiver. Cusmai et al. (2006) addressed this problem by applying a fixed notch filter in the UWB receiver design [3]. The notch was implemented as a double peak single notch reactive load for the LNA that effectively suppresses the whole 802.11a band.

By using such an approach one may need to permanently relinquish the use of sub-bands coinciding with the locale of the notch. If the 5GHz WLAN interferer is transient in nature, that is it does not exist at all times, then it is not necessary to avoid these bands at all times either. However, if the decrease in spectrum is acceptable, then this is an effective technique to attenuate the WLAN interferer. One aspect to note is that the ability to tune these notches is limited and therefore the approach may not be effective to reject interferers at arbitrary frequencies.

2.2 SPATIAL MULTIPLEXING

Spatial multiplexing originally refers to transmitting independent data signals from multiple antennas such that the physical space media is reused. On the receiver side, similarly, multiple antennas can be used in parallel to address multipath fading problems.

These parallel signal paths can then be combined with proper complex weighting factors to optimize the signal to noise ratio (SNR) in either the digital or analog domain.

Paramesh et al. (2005) demonstrated the on-channel interferer mitigation effect in multiple input multiple output (MIMO) systems [4]. The system exploited the fact that desired signals and interferers arrive at different angles, and through adequate combination, can add up either constructively or destructively. A mathematical explanation can be provided by referring to Figure 3 below.

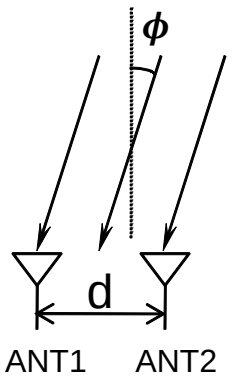


Figure 3: Input signal diagram of a two antenna receiver system.

Shown in Figure 3, for incident signals with angle ϕ, the phase difference between ANT1 and ANT2 is $2\pi(d/\lambda)sin\phi$, where d is the distance between the two antennas, and λ is the wavelength. Assuming the desired signal has an incident angle of ϕ_1 and the interferer has an incident angle of ϕ_2, with $\psi_{1,2}=2\pi(d/\lambda)sin(\phi_{1,2})$, the interference suppression task is translated to finding a solution for the following equations:

$$\begin{aligned}[exp\left(\frac{j\psi_1}{2}\right)\cdot\omega_1 + exp\left(-\frac{j\psi_1}{2}\right)\cdot\omega_2] &= 1\\ [exp\left(\frac{j\psi_2}{2}\right)\cdot\omega_1 + exp\left(-\frac{j\psi_2}{2}\right)\cdot\omega_2] &= 0\end{aligned} \tag{2.1}$$

where ω_1 and ω_2 are complex weighting factors for the correspondent receiving antennas. In the simplest case, ϕ_1 and ϕ_2 are assumed known *a priori*. However, [4] showed that with adaptive approaches only direction of arrival (DOA) of the desired signal is needed, which can be obtained during the channel estimation phase. Furthermore, in general *N-1* interferers can be suppressed in a similar fashion with *N* antennas.

Based on similar principles Neumann et al. (2006) reported an adaptive notch filter for UWB applications using least mean square (LMS) estimation [5]. In that work, two antennas are required, where the signal of the second antenna is phase rotated in such a way that the narrow band interferer is out of phase with the signal of the first antenna before they are combined. The phase rotation is done by weighting the in phase (I) channel and the quadrature (Q) channel separately, making it unnecessary to use the more expensive phase shifter components. Desired signal may also get degraded in this approach, however, at a much less degree due to the broadband nature of UWB.

The requirement of multiple receivers and antennas adds to both hardware and software complexity and cost in the above approaches. Furthermore, interferer cancellation based on spatial multiplexing is challenging before the down-conversion mixers, where the most severe linearity requirements often arise, due to the need for phase shifters at RF.

2.3 FEED-FORWARD CANCELLATION

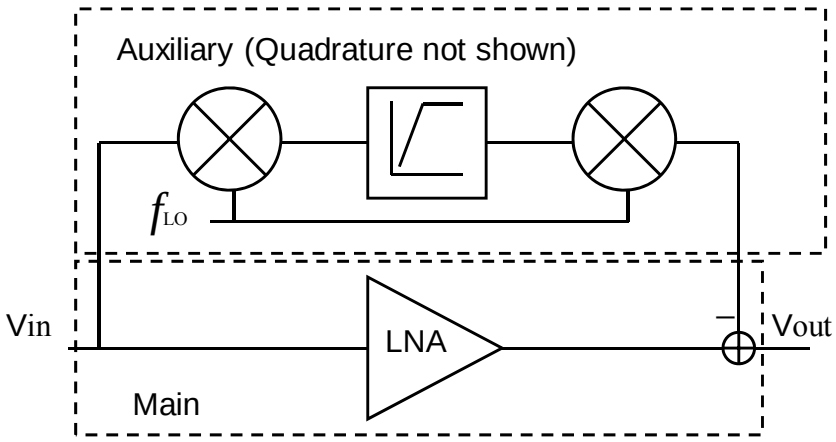


Figure 4: Block diagram of feed-forward cancellation scheme with auxiliary down-/up-conversions.

Gharpurey and Ayazian (2006) introduced a feed-forward interferer cancellation technique with auxiliary down/up-conversion paths [6, 7]. The main idea behind the approach is to shift the burden of designing a sharp notch filter in the RF domain to baseband where for the same frequency offset the filter Q factor can be greatly relaxed. In this approach, as shown in Figure 4, the desired signal is first down-converted to baseband using the same LO signal as the main signal path. As a result of this down-conversion, the desired signal now locates at baseband around DC while the interferer stays at some intermediate frequency (IF). A high-pass filter (HPF) is then used to select the interferer and reject the desired signal from the auxiliary path. The output of the HPF that mainly consists the interferer is then up-converted to RF, again with the same LO signal as the main signal path. This up-converted signal is then applied back to the main signal path for interferer cancellation.

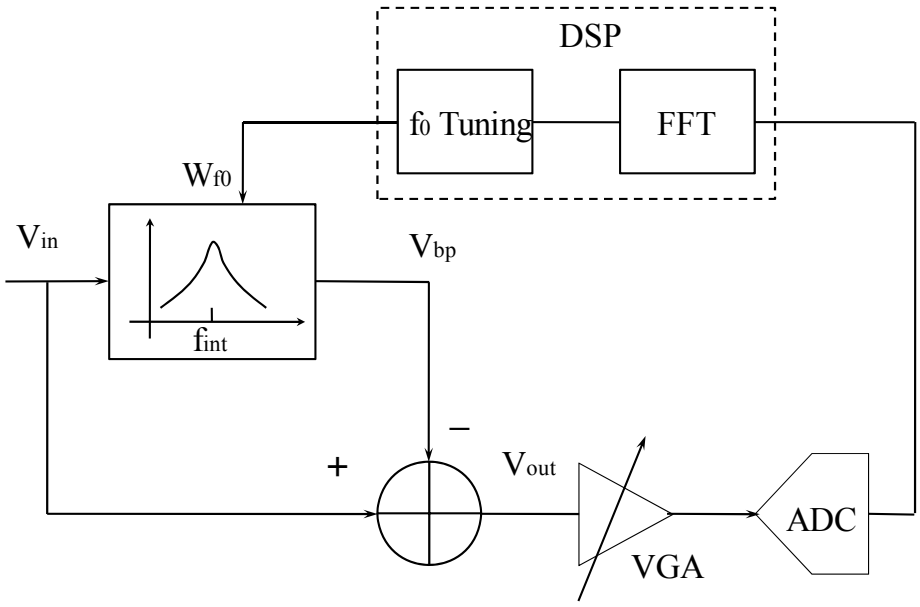
Since the desired signal is attenuated within the stop band of the high-pass, the architecture is not suitable for large co-channel interferers. Another aspect to be taken into account is that since the system utilizes feed-forward, gain and phase alignment between the main and auxiliary path is required for achieving perfect cancellation, namely the two paths must have equal magnitudes and be out of phase from each other. A tunable delay can be used which requires a one-time calibration to align the phase, and baseband variable gain amplifiers are utilized for gain calibration. Multi-tone cancellation is described in [7] and gain and phase calibration is required there as well. While not a performance limitation, gain and phase calibration requires additional hardware.

In a similar implementation, Darabi (2007) [8] demonstrated the feed-forward interference cancellation on silicon. This design assumed a blocker frequency well above the HPF corner frequency and was not suitable for attenuating close-in interferers. Further approximately 3dB worsening of noise figure was reported, with the auxiliary path, which utilized almost the entire margin on sensitivity allowed by the system in the presence of interferers, leaving little room for accommodating other sources of SNR degradation such as IM2 or reciprocal mixing.

2.4 FEED-FORWARD CANCELLATION WITH LMS DETECTION

Fischer et al. (2007) implemented an adaptive analog notch filter to suppress narrow-band interference (NBI) in MB-OFDM systems at baseband [9]. The notch filter is introduced between the LPF and the VGA. Shown in Figure 5, the notch filter is formed using a tunable bandpass filter that tracks the interference frequency after the direct down-conversion mixer as shown in Figure 5(a). The filter output is subtracted from the main signal path while its gain is controlled by the LMS engine to minimize the final interferer output level.

The interference detection is done through an FFT in the baseband, by checking whether peak to average energy ratio is above certain threshold in a given bin as shown in Figure 5(a). The bandpass filter's center frequency ω_0 is controlled by a digital word based on the equation $\omega_0 = \rho W_{f0}$, where W_{f0} is the digital word obtained by FFT, and ρ is the frequency step size in hertz between adjacent filter frequency settings. ρ has to be chosen carefully to balance good frequency coverage and search time. Due to the wide bandwidth for OFDM-UWB applications and added complexity such as frequency hopping, the searching algorithm to set the optimal center frequency on the bandpass filter is nontrivial.



(a)

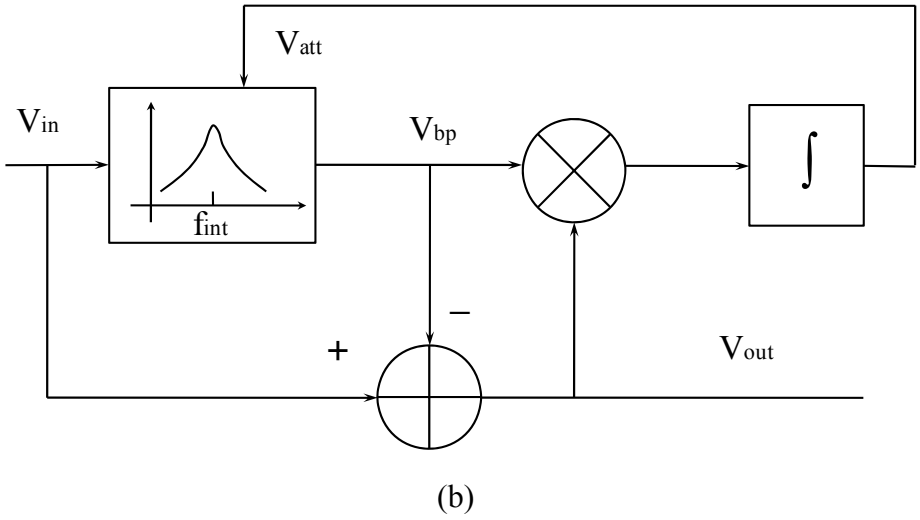


Figure 5: Block diagram of feed-forward notch filter. (a) Filter center frequency tuning. (b) Filter unity gain control.

Gain control is needed to address variation over process and temperature changes. As shown in Figure 5(b), the multiplier and integrator work together to form the LMS engine. When the passband gain of bandpass filter drifts away from unity, the interferer at the summer block will not be ideally cancelled, and the residual interferer energy is used to control the gain of the bandpass filter to bring it back to unity.

This approach allows for a tunable notch that potentially can cover arbitrary interferers with DSP control. However the interference cancellation is at baseband and thus does not alleviate the RF front end linearity requirements such as those for the down conversion mixer input stage.

2.5 AUXILIARY PATH CANCELLATION USING LPF FOR BROADBAND DESIRED SIGNALS

Instead of tuning the notch filter to track unknown interference, a different approach was used in [10] by Safarian et al. (2007), where a low pass filter (LPF) was used in an auxiliary path configured as a feedback loop as shown in Figure 6. Compared

with HPF based feed-forward approaches discussed in 2.3, this approach uses a different LO signal for the auxiliary down- and up-conversion such that for baseband portion the narrow band interferer is around DC while the desired signal at IF. The bandwidth of the LPF is set by that of the interferer instead of the signal.

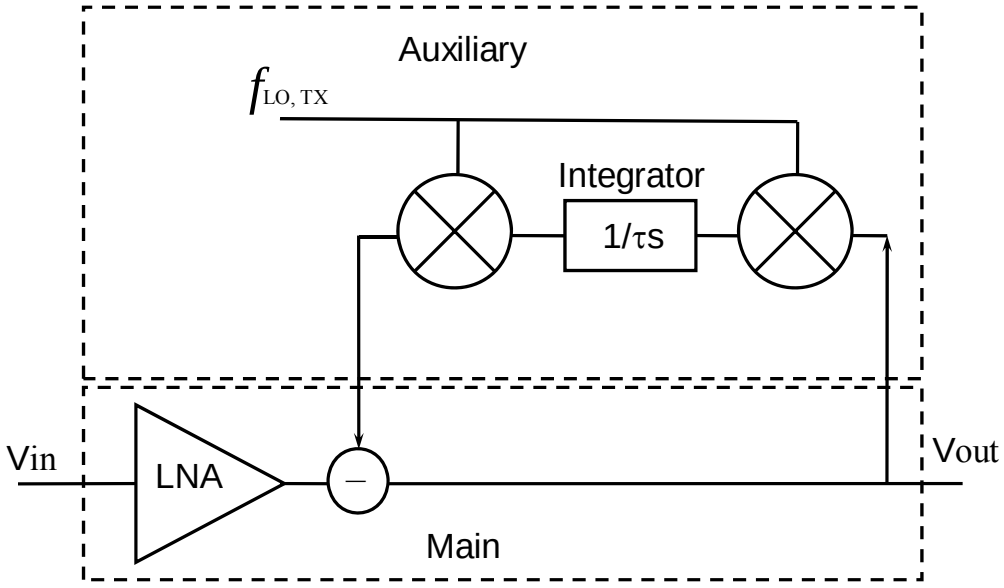


Figure 6: Block diagram of LPF based feedback auxiliary path cancellation loop.

The authors have offered several advantages for the feedback approach versus feed-forward including less stringent linearity requirement for the auxiliary mixers, robustness against non-idealities and mismatches, and less variation on the input capacitance when switching on/off the auxiliary path. A limitation of the feedback based approach however arises from the potential for instability. Since the group delay in the baseband LPF is significantly larger than that in the RF path, stability is in fact a key consideration in such systems. Thus while low-order filters (e.g. a first order filter

employed by the authors) can be employed, higher order filters, if necessary to implement, can lead to serious stability concerns.

Another aspect to consider is that for the general problem of interference suppression this approach would need to know the location of the interference a priori, and have a separate LO capable of tuning to all the necessary frequencies. Since this approach was demonstrated for rejection of the transmit path leakage in a WCDMA transceiver, the transmitter side LO could be easily employed for this purpose.

2.6 MATCHED COPY APPROACH WITH KNOWN INTERFERENCE SOURCE

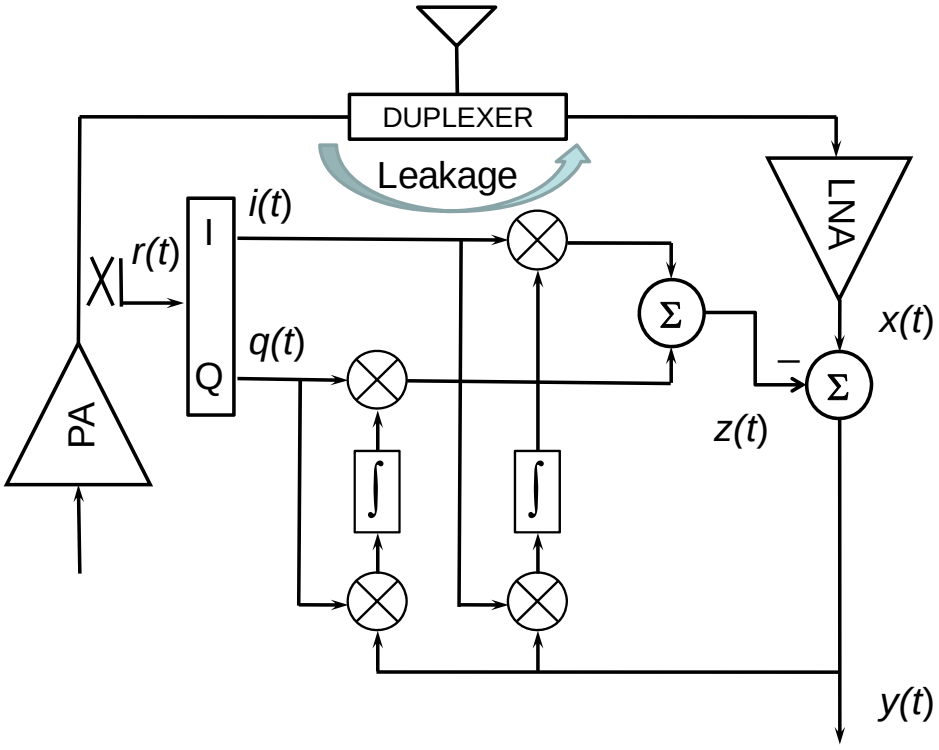


Figure 7: Block diagram of LMS based CDMA transmitter leakage interference cancellation.

Aparin et al. (2005) had previously reported another LMS based feed-forward interference cancellation for CDMA receiver applications [11], to reduce the impact of the transmit leakage. This approach was based on generating a matched copy of the transmit leakage using a power coupler at the output of the power amplifier (PA) and employing this copy for cancellation at the output of the front-end LNA.

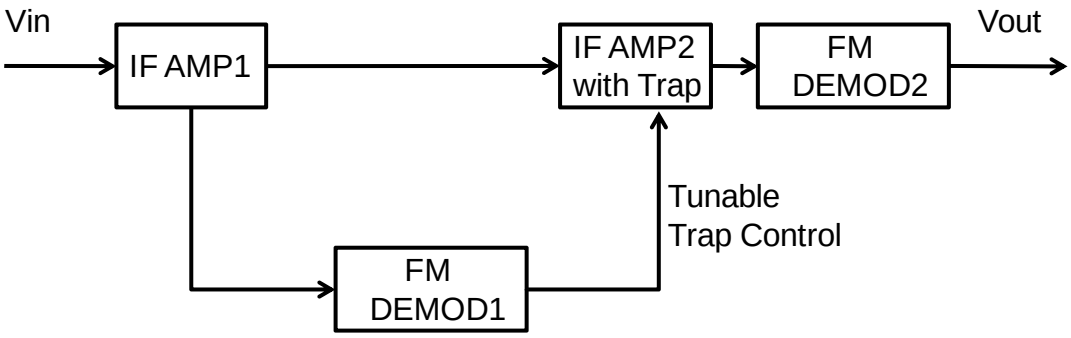
As shown in Figure 7, transmitter leakage reference *r(t)* is decomposed into quadrature terms *i(t)* and *q(t)* respectively, which after some proper scaling, are recombined into *z(t)* and subtracted from the LNA output signal *x(t)* to generate the final output *y(t)*. The scaling factors of *i(t)* and *q(t)* are generated by the correlation factor (done by multiplication and integration as shown) between themselves and the final output *y(t)* in a fashion similar to matched filters. Finally the LMS adaptation is achieved as a result of the negative feedback loop.

This approach achieved interference cancellation immediately after the LNA and potentially can handle much wider desired signal bandwidth than CDMA such as UWB. However, the approach requires the interferer to be locally available.

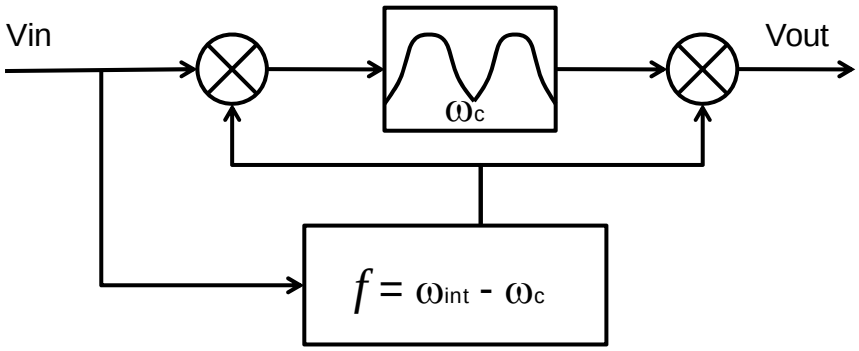
2.7 DYNAMIC TRAPPING SYSTEMS FOR FM RADIOS

It is instructive to also examine earlier approaches to dynamic trapping systems designed for FM radio systems. Baghdady [12] described two such schemes for FM.

The system is used for rejecting a large FM interferer and detecting a small desired signal. This is done by first demodulating the large interferer, and using it to tune a variable frequency FM trap within a second amplifier that rejects the large interferer (Figure 8a). The resultant final output signal is therefore dominated by the original weaker desired signal.



(a)



(b)

Figure 8: Block diagram of FM notch filter. (a) Variable tuned trap system. (b) General form of fixed trap system.

A fixed trap can also be utilized, as shown in Figure 8(b), in combination of down- and up-conversion mixers that is clocked by a third signal at an instantaneous frequency away from the interference signal ω_{int} by an offset equal to the fixed notch frequency ω_c. This third signal can be generated by two different ways. One method is to use the strong interference available from a conventional FM demodulator output to modulate the reactance of an oscillator. Alternatively without demodulating the strong

interference, the input IF signal can be used to multiply with a fixed frequency oscillator after passing through a weak signal suppressor.

Rich (1994) also utilized a fixed notch approach [13], but the input was shifted by a fixed frequency ω_c to DC. The advantage of doing this is to mitigate the non-ideal effects associated with the mismatch between the notch filter and ω_c, especially when the stopband of the notch filter is very narrow. Another enhancement proposed in [13] is to adopt the more accurate strong signal frequency estimation proposed by Sundresh et al. (1977) in [14], using cross coupled notch filter interference suppressor.

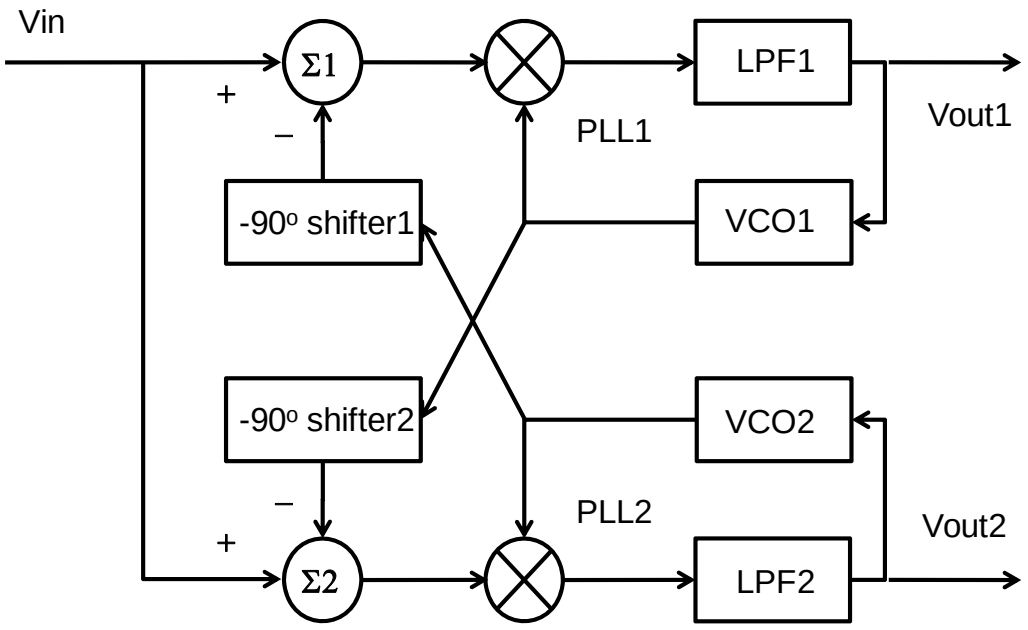


Figure 9: Cross coupled FM demodulator with enhanced interference frequency tracking accuracy.

As shown in Figure 9, input signal V_{in} consists both a weak desired signal and a strong interference. PLL1 locks onto and tracks the strong interference first. The VCO1

output phase is lagging by about 90 degrees from the input signal due to the quadrature multiplier used. Another 90 degree phase shifter ensures that the locally synthesized replica of the intererferer which is applied to Σ2 is out of phase relative to the strong incident interfering signal. Therefore the output of Σ2 largely consists of the weak desired signal as the interference has been cancelled out. Similarly, the output of Σ1 consists of only the large interference signal, compared with the case where no cross coupled phase shifters are used. As a result, demodulated output signals V_{out1} and V_{out2} provide cleaner signal component of the interference and the desired components respectively, and consequently provide better control on the effective notch filter center frequency in the original approach.

These FM interference suppression methods based on instantaneous frequency estimation are designed specifically for the FM radio system, and therefore cannot be directly applied to other modulation schemes.

2.8 SUMMARY OF EXISTING APPROACHES

While above interference cancellation approaches cover a wide variety of applications, each has its own assumptions and requirements, as described in the corresponding sections. These approaches are difficult to use for broadband wireless systems for rejection of co-channel or out-of-sub-band narrow-band interferers, due to either the requirement for narrow signal band, the requirement for knowledge of the interferer location, the requirement for calibration, or the need for extra hardware for multiple antennas and front-end radios. We propose an architecture here, which can provide a viable solution for the problem statement presented earlier.

Chapter 3: Description of the Proposed Architecture

3.1 Desired properties of the new design

Based on discussion of various aspects of active interferer cancellation techniques proposed in earlier work in Chapter 2, we summarize below the desirable features of the new interference suppression scheme.

1. Capable of handling interference level much stronger than desired signal;
2. Able to accommodate wideband desired signal such as the MB-OFDM version of UWB, or WiMedia;
3. Capable of relieving linearity requirement as early as possible in the receiver chain, preferably before the down-conversion mixer at RF front-end;
4. Capable of suppressing close in interference signal;
5. Does not require the use of multiple antennas or receivers, to minimize cost penalty;
6. Does not require an available carrier signal of the interference;
7. Minimal calibration requirement

3.2 Generation of a linearly independent copy of the input

A fundamental requirement for suppressing the interferer is to generate linearly independent copies of the interferer and the signal. One approach would be to implement a functional block that effectively rejects the much larger interference signal and allows the signal to pass through, which is a challenge at RF. Alternatively, one could develop a block that selects the large interferer but rejects the small desired signal, followed by subsequent cancellation of the interferer through feed-forward or feedback (e. g. [6][7][8][10]).

A possible approach is to employ an injection-locked oscillator (ILO). When a sufficiently strong signal appears at the injection port of an ILO, the positive feedback loop that helps sustain the original oscillation reaches a new stable state where the oscillation frequency becomes equal to that of the injected signal frequency. The small desired signal will appear as a sideband at the output of the oscillator, although with different amplification. This allows for a linearly independent combination of the desired signal and interferer at the output of the LNA.

It is important to ensure that the ILO amplifies the strong interferer differently compared to the desired signal, otherwise the ILO output signal will become a scaled copy of the original input and thus will not be useful for interference cancellation. Phasor analysis (e. g. [15]) will be followed in some later discussions in this report for theoretical analysis. For the time being, we make this assumption.

It is highly desirable to achieve as large a differential gain operating on the interferer and the signal as possible. As will be discussed in more details later, this is addressed by tuning the free running center frequency of the ILO towards the injected interference frequency. As a result, the tank and ILO circuit will provide certain level of sideband rejection that lowers the gain for the small desired signal. This sideband rejection effect can be further enhanced by improving the effective quality factor (Q) of the oscillator, as will also be discussed when individual block designs are covered.

In general, the interferers will be modulated. Thus the design must be able to track both amplitude and phase modulation of the interferer. This is discussed later in the text.

3.3 A HIGH-LEVEL DESCRIPTION OF THE PROPOSED STRUCTURE

Assuming an injection-locked oscillator (ILO) can be designed to meet all above mentioned characteristics, a feed-forward interference cancellation structure can be implemented, as shown in Figure 10.

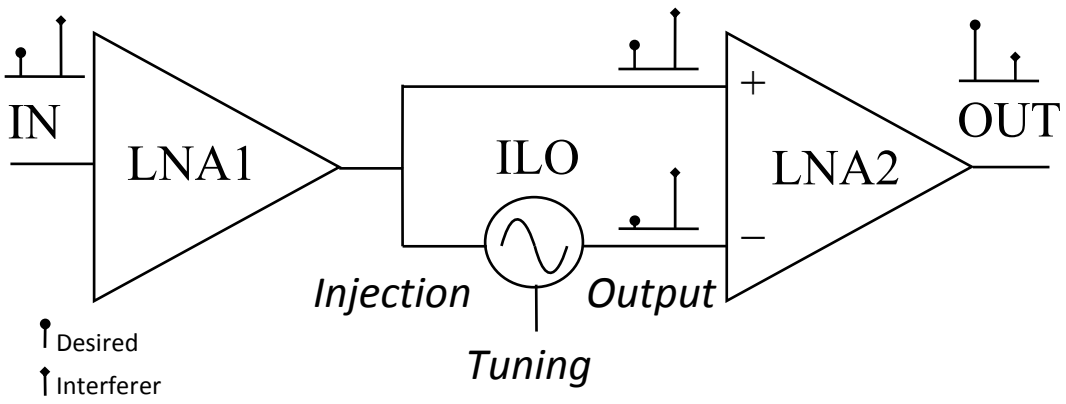


Figure 10: A high level block diagram of the proposed interference suppression scheme.

In the proposed scheme, both the interference and the desired signal are amplified by the first stage of a low noise amplifier (LNA1). The signal is split into two paths at its output. One path is applied to the non-inverting input node of a second LNA stage (LNA2) while the other path is applied to the injection-locked oscillator (ILO), the output of which is connected to the inverting input of LNA2. As discussed above, the ILO amplifies the large interference signal with higher gain compared to the small desired signal, making it possible for LNA2 to reject one of the two signal components because there are now two linearly independent copies of the net signal. Referring to Figure 10, if the interference components appearing at the differential input nodes of LNA2 are in-phase and equal in magnitude, an ideal cancellation should result at the LNA2 output.

Therefore the goal of suppressing the strong interference is achieved before it reaches the RF down-conversion mixer that normally immediately follows the LNA block.

With this high-level architecture, it is helpful to review the desired feature list summarized in Section 3.1. Items 1, 3, 5, and 6 are satisfied because the proposed scheme generates its own linearly independent copy of the auxiliary signal (to satisfy 5 and 6) and the ILO characteristic satisfies 1. Item 3 is satisfied simply from the location of the proposed scheme, namely within the LNA. Item 2 can also be satisfied, because no constraint has been set for the bandwidth of the small desired signal in the proposal. Item 4 and 7 requires extra attention and it will be shown in the next section that they are addressed together with another desired feature mentioned earlier that modulated interferer (versus simple CW tone) should also be handled.

3.4 DESCRIPTION OF THE FULL ARCHITECTURE

A dynamically adaptable notch filter can be realized with an ILO embedded within a phase locked loop (PLL) to provide self-tracking capability to address phase or frequency modulated interference. Furthermore, the auxiliary path can self-adapt to the interferer frequency with automatic phase alignment which is a highly desirable property. As will be discussed more in later sections, the automatic phase alignment also makes it possible to suppress close-in interference signal since the desired signal which is at an offset frequency does not get simultaneously phase aligned, unless other constraints such as noise floor degradation forbid it.

Figure 11 shows a block diagram of the full proposed structure. A two-stage LNA is used in the front end, where the output from the first stage (LNA1) is fed into the injection port of the oscillator with programmable negative resistance strength and center frequency (f_c). The frequency f_c can be programmed using coarse and fine settings, with

digitally controlled capacitors and analog varactors, respectively as shown in Figure 12. The output of the oscillator and LNA1 are also fed into a custom phase detector (PD). The transfer function of the PD is designed to have zero voltage at zero degree input phase offset. As in a classical PLL, the PD output drives an analog charge pump (CP) and a second-order loop filter (LF) to generate an analog tuning voltage that is applied to the oscillator's varactor tuning port.

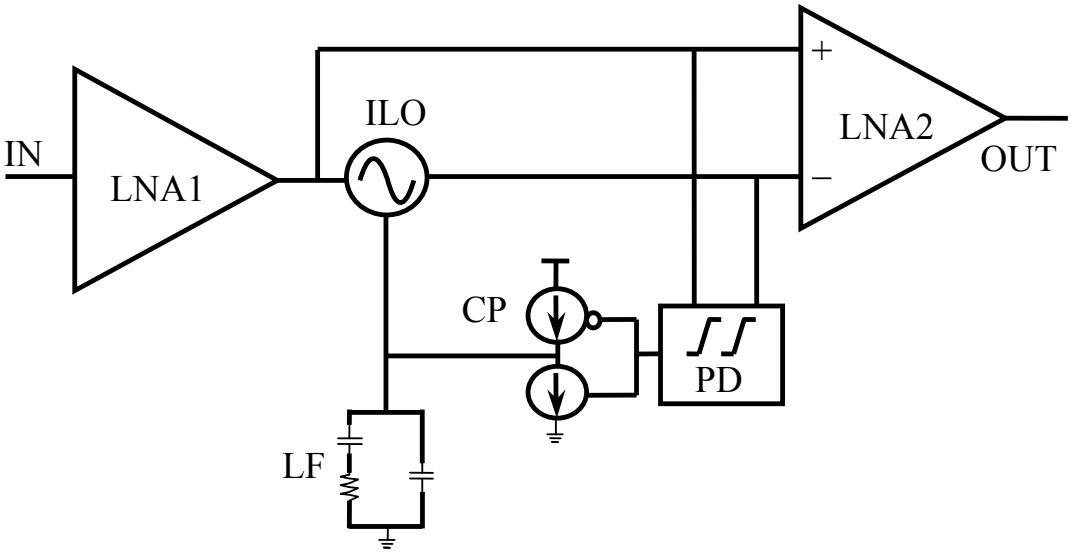


Figure 11: Block diagram of proposed interferer suppression technique with PLL shown in more details.

The second stage of the LNA is a differential buffer LNA2. When the phases of the interferers with equal amplitude from the output of LNA1 and the output of the oscillator are aligned, they will be accurately canceled at the output of the second stage LNA2. Amplitude control is necessary at the input of LNA2 to ensure that the

interference levels at the differential inputs of LNA2 are equal. The bias control of the ILO was used for setting the amplitude at its output. This makes the negative resistance strength of the oscillator directly related to the strength of the interferer and causes more systematic phase error due to second order behavior for small interferer amplitudes, which leads to non-ideal cancellation in LNA2. However since the amplitude of the interferer is small to begin with at this point, the system level impact is not significant.

If cancellation at small interferer levels is also important, a programmable gain amplifier (PGA) can be used to control the amplitude at the output of the ILO in the auxiliary path. A power detector at the output of LNA2 can be used to control the gain of PGA2. These features were not implemented in this design.

3.5 IMPLEMENTATION OF THE ILO

The oscillator circuit (Figure 12) is a cross-coupled NMOS core with an LC tank, with programmable bias. The oscillator's negative resistance strength can be programmed by either the cross-coupled latch device aspect ratio or the bias current level. While both were implemented in this design, it is preferred to utilize the bias control due to the more continuous nature for tuning. This control can also be employed for AM suppression that will be discussed more in later chapters.

The oscillator is initially operated in a low-Q non-oscillating mode, by employing a sufficiently low bias-current, which ensures that the losses in the tank are greater than the energy supplied by the negative resistance presented by the active devices. In this mode the oscillator is essentially a tuned buffer utilizing a shunt LC tank. The LC buffer amplifies the interferer with zero phase shift when its center frequency equals that of the interferer, at which point the tank presents a resistive impedance. This observation is used to tune the center frequency of the tank to be equal to that of the interferer (to the first

order), by embedding the buffer within a PLL which compares the phase of the RF interferer applied to the input of the LC buffer to that appearing at its output, and minimizes this difference by tuning the center frequency of the tank.

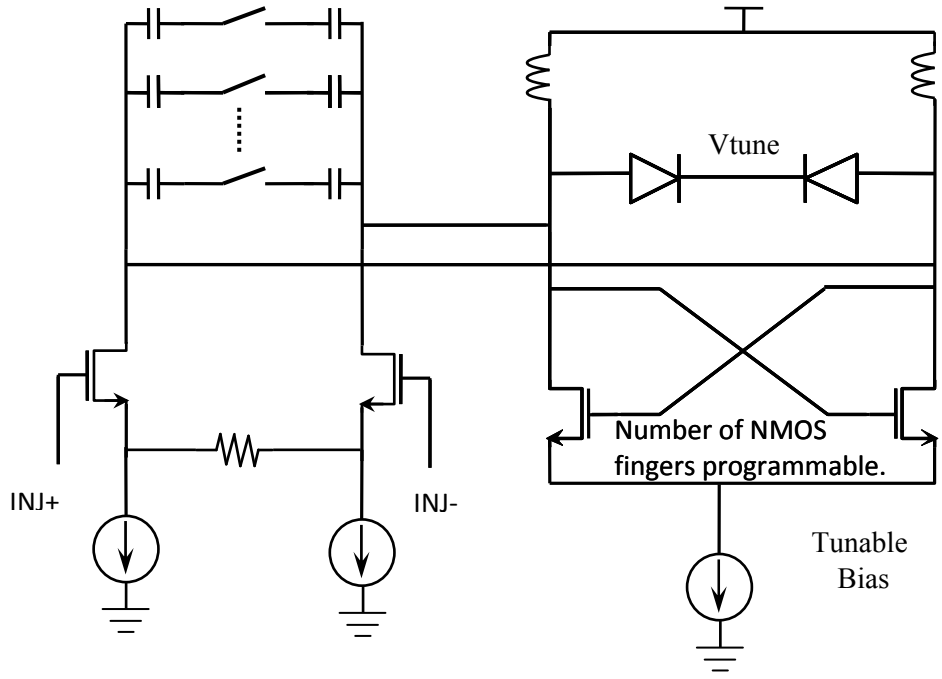


Figure 12: Schematic of the ILO.

Once this frequency tuning is achieved, the bias of the oscillator circuit block is increased incrementally, until it becomes unstable and enters oscillation. The strength of negative resistance shunting the LC tank in this mode can be tuned by adjusting the bias current, which also controls the amplitude of the interferer. Since the PLL sets the tank center frequency to be equal or very close to the interferer frequency, the oscillator injection-locks to the interferer, even if the negative resistance strength of the oscillator is programmed to a high value, without the risk of self oscillation at the oscillator's free running frequency. The ILO provides greater rejection of the RF signal compared with

the interferer, over that available in the passive LC tank used standalone, as will be discussed more in the next chapter.

From [15], the locking range of an ILO ω_{LR} is approximately given by

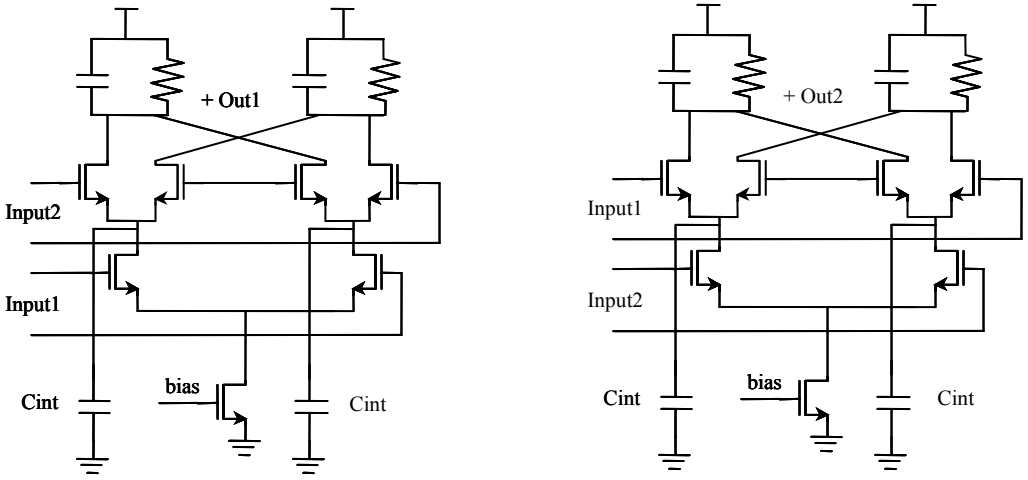
$$\omega_{LR} = \omega_0 I_{inj}/(2QI_{osc}) \tag{3.1}$$

where ω_0 is the center frequency, I_{inj} and I_{osc} are the drain currents of injection device and latch device of the ILO, respectively. For a given current consumption budget, locking range of the ILO is finite, and decreases when Q or I_{osc} increases. If the oscillator enters self-oscillation mode where it is not injection-locked to the interferer, there will be at least two separate strong tones, the interferer and the self oscillation output, and the phase detector will be effectively disabled with an average output of zero.

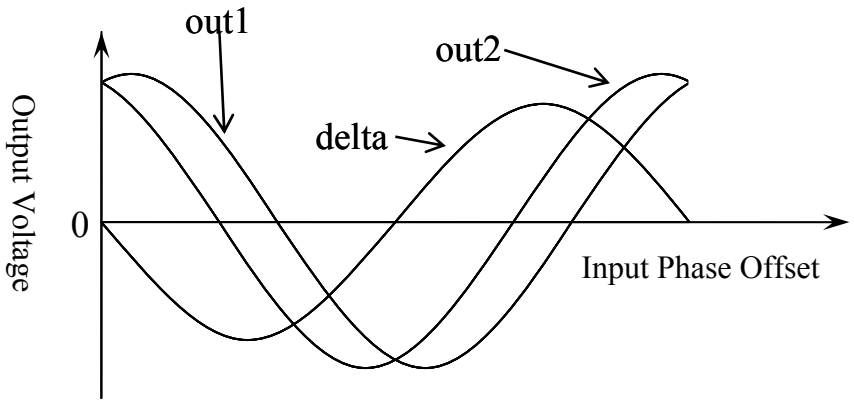
Therefore it is essential to use the PLL to initially bring the tank center frequency near the interferer frequency. It guarantees that even with large I_{osc}, which may be required for amplitude matching at the input of LNA2, the oscillator remains injection-locked and does not self-oscillate.

3.6 PHASE DETECTOR

A GHz PD is employed whose output voltage reaches zero when input signals are phase aligned. A traditional mixer-based PD employing a Gilbert cell ideally has zero output voltage with quadrature input signals, instead of having zero phase offset that is desired for interferer cancellation. Furthermore ideal quadrature zero crossing point is difficult to achieve at higher frequencies due to parasitic capacitance at common mode nodes in the Gilbert cell. The output zero crossing point actually shows significant variation at high frequencies.



(a)



(b)

Figure 13: (a) Schematic of the PD used in this approach. Cint's are 0.1pF extra capacitors. (b) Phase detector transfer function – the "delta" curve is the combined output of the new PD.

In this work, we used two Gilbert cell phase detectors with inverted input signal sequences for the two identical cells, as shown in Figure 13(a). We take the difference of the two output signals. Shown in Figure 13(b), 'out1' and 'out2' are output signals from

each cell and ‘delta’ is the difference signal whose zero output occurs exactly at zero input phase offset. For ideal case without parasitic capacitance on the common mode nodes, the PD output will be at zero as ‘out1’ and ‘out2’ overlap and cancel each other. Capacitors of value 0.1pF were added in the design to the common mode nodes in the Gilbert cells to offset ‘out1’ and ‘out2’ to address this. Note that as the capacitance is increased, the phases of 'out1' and 'out2' deviate in opposite ways, one taking on a positive phase shift and the other a negative phase shift compared with the case with zero parasitic capacitance.

3.7 SUMMARY

As discussed above, the proposed scheme seeks to attenuate strong incoming interference by injection-locking it to an ILO, phase aligning the ILO output signal to the input, and subtracting that output signal from the main signal path with amplitude equalization.

Critical circuit blocks have been discussed in this chapter. More details on these blocks and other circuits will be covered in next chapter along with simulation results.

Chapter 4: Circuit Design and Simulation

The design was implemented in UMC's 0.18μm RFCMOS process. The design was optimized in the sub-2GHz frequency range, due to this choice of process. As a result, the test circuit operates around a center frequency of 1.5GHz, instead of a point within the 3.1 – 10.6GHz range. Consequently, this work demonstrates the proof of concept although at a lower frequency. Some simulation results using a more advanced technology, namely UMC's 0.13μm process, will also be presented in the Appendix to justify the applicability to higher frequency operation with a faster technology.

4.1 LOW NOISE AMPLIFIER (LNA)

A two stage LNA is used for two main reasons. In order to minimize noise degradation, output from the auxiliary path has to be preceded by an amplifier. Further, having more than one stage also makes broadband design more flexible with staggered peak frequencies for different stages. Both stages use identical structures as shown in Figure 14, with slightly different device sizes to accommodate for different loading capacitance as well as the staggered peak gain locations. Load inductors are connected with series resistors to lower the quality factor Q such that a relative broadband behavior can be achieved for individual stages.

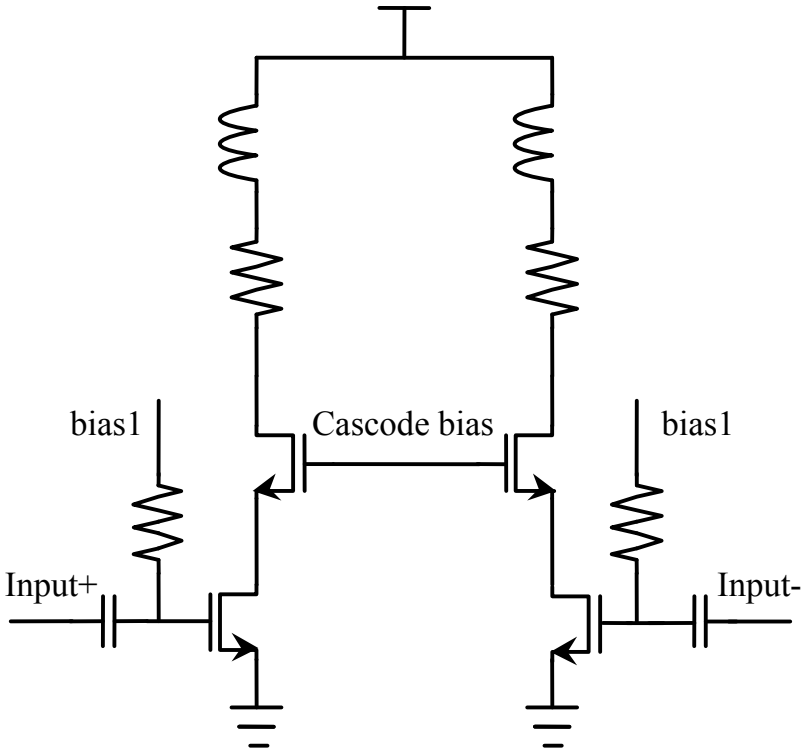


Figure 14: Schematic of one LNA stage.

4.1.1 LNA topology with pseudo differential input stage

As shown in Figure 14, each stage of the LNA uses common source input devices with cascode devices for better reverse isolation. The pseudo-differential input structure was chosen over a more traditional differential pair with tail current device for better linearity, because this structure provides built-in class-AB behavior that boosts the input linearity.

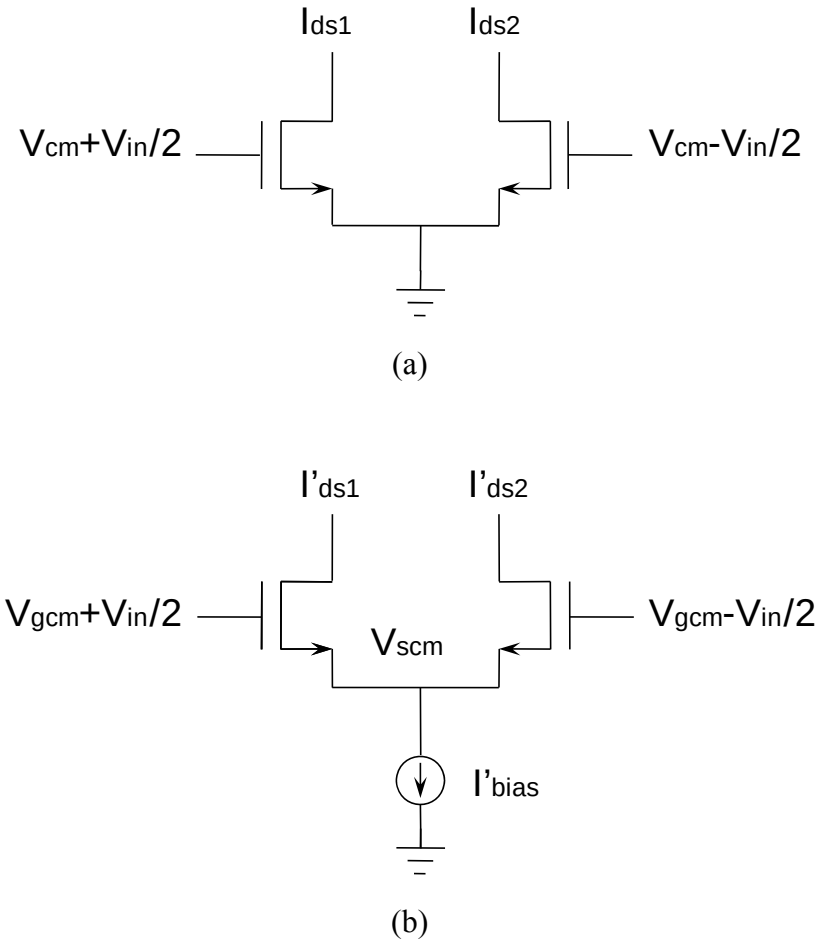


Figure 15: (a) A pseudo differential input stage. (b) A true differential input stage.

Intuitively, the class-AB effect arises from the effective increase of the gate bias point under overdrive condition, which does not happen in the case of true differential pairs for which DC bias current is set by the tail current device. As shown in Figure 15(a), assuming saturation mode for both input devices,

$$I_{ds1,2} = \frac{1}{2}\mu C_{ox}((V_{cm} - V_{th}) \pm \frac{1}{2}V_{in})^2 \qquad (4.1)$$

where $I_{ds1,2}$ is the drain to source current of one of the two input devices, μ is the mobility, C_{ox} is the unit gate oxide capacitance, V_{cm} is the input common mode gate bias voltage, V_{th} is the threshold voltage of the MOS devices, and V_{in} is the differential input voltage. Taking the difference between the two currents, differential output current I_{ds} is given by

$$I_{ds} = \mu C_{ox}(V_{cm} - V_{th}) \cdot V_{in} \tag{4.2}$$

As can been seen from (4.2), I_{ds} is a linear function of differential input voltage to the first order even for large signal. Compared with the true differential pair case, the small signal behavior is the same. To confirm the intuitively correct linearity improvement mathematically, equation (4.1) can be modified slightly for the true differential case shown in Figure 15(b) to be

$$I'_{ds1,2} = \frac{1}{2}\mu C_{ox}[(V_{gcm} - V_{scm} - V_{th}) \pm \frac{1}{2}V_{in}]^2 \tag{4.3}$$

where $I'_{ds1,2}$ is the drain to source current of one of the two true differential pair devices, V_{gcm} is the common mode gate bias voltage, and V_{scm} is the common mode source voltage shared by the two devices. Similarly, taking the difference between I'_{ds1} and I'_{ds2}, the differential output current can be written as

$$I'_{ds} = \mu C_{ox} V_{in}(V_{gcm} - V_{scm} - V_{th}) \tag{4.4}$$

Comparing (4.4) to (4.2), the only difference is the extra term V_{scm} for the true differential case. If V_{scm} were constant, the transfer functions would be identical in the two scenarios, which in reality is not the case. This is because V_{scm} can only be regarded as a constant voltage for small signal analysis approximation, which is commonly referred to as the 'AC ground'. In reality, even for real small signal input, total current is set by I'_{bias}, i.e., $I'_{ds1} + I'_{ds2} = I'_{bias}$. According to (4.3) that gives a quadratic V-I transfer function, V_{scm} has to partially follow the positive side of input voltage signal to achieve a balanced change of I'_{ds1} and I'_{ds2}, and this behavior becomes more significant when input signal goes larger. In the extreme case, when the negative swing is large enough to effectively shut down the correspondent NMOS device, the NMOS on the positive side behaves like a source follower biased with a constant current I'_{bias}.

As a result of the partial source follower behavior for the true differential pair structure, output current experiences gain compression effect even within the small signal domain and eventually gets clipped at the limit set by I'_{bias}. On the contrary, as shown in (4.2), for the pseudo differential pair is fully switched, the V-I curve remains linear to the first order, as long as both devices have positive current levels if V_{th} is treated constant and channel modulation effect is ignored. From (4.1), it is clear that the linear input range for the pseudo differential case is $2(V_{cm} - V_{th})$.

4.1.2 LNA input match

Input matching network design is one of the most critical steps that directly affect several LNA performance parameters such as noise figure (NF) and power gain.

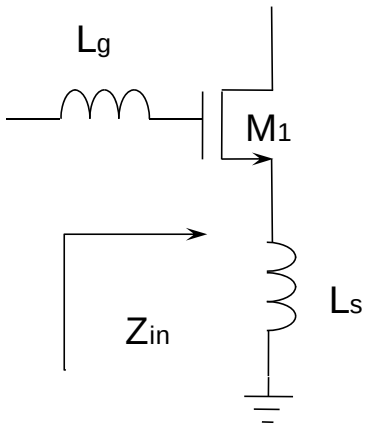


Figure 16: CMOS LNA common source input stage with source degeneration inductor.

For CMOS LNA design, a source generation inductor is often used to facilitate input matching. Bond wires can often economically provide this source degeneration inductance, which forms the real part of input impedance Z_{in} as shown in (4.5),

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}} \tag{4.5}$$

where L_g and L_s are matching inductors at the gate and source of input device M_1, respectively, as shown in Figure 16. g_m and C_{gs} are the transconductance and gate to source capacitance of M_1. At resonance, the input impedance is real and equals to $g_m L_s / C_{gs}$.

This matching approach, however, is more applicable for narrow band signals since the reactive terms in (4.5) only get cancelled at certain frequency. For UWB applications, special techniques are needed to address the bandwidth requirement. Ismail et al. (2004) reported an LC ladder filter based broadband matching network using BiCMOS process [18] while Bevilacqua et al. (2004) independently reported a similar

approach implemented in CMOS process [19]. Both filter matching approaches achieved flat gain across the whole 3.1–10.6 GHz band with acceptable noise performance. However, both implementations require large die area due to the inductors needed to compose the filter. To address this concern, Gharpurey (2005) reported a resistive shunt feedback approach to achieve the broadband matching with significantly smaller die size although at the expense of a slightly higher noise figure within the band of interest [20].

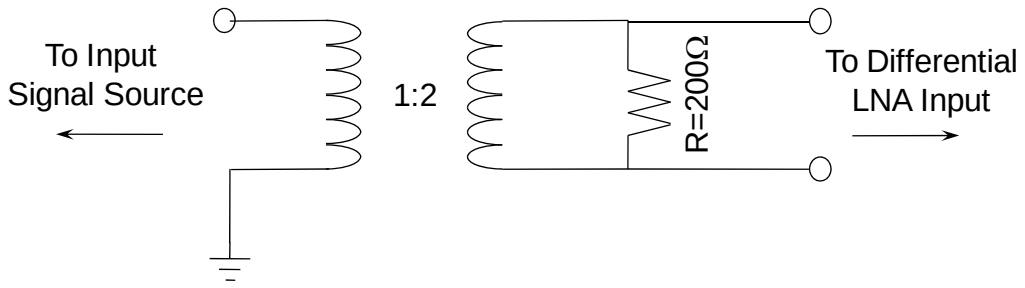


Figure 17: Simple resistor input match with 1:2 balun and 200Ω physical resistor in shunt with LNA input.

While similar matching techniques like those used in [17-19] could have been applied for this project, a simple resistor match with a 1:2 balun was used for simplicity. As shown in Figure 17, the 1:2 balun transforms the 200Ω resistor back to 50Ω that is desired for the normal 50Ω impedance signal source. To be more precise, the 200Ω resistor is in shunt with the LNA input capacitance. However, at sufficiently low input frequency, this shunt capacitance will not change the input impedance significantly. A direct drawback of using such a matching scheme is the degradation on noise figure (NF), which is close to 3dB. Although this degradation is known and can be accounted for

without affecting the interference cancellation performance much, it is still desirable to be able to evaluate the chip without seeing this extra NF degradation.

A simple way to reduce NF degradation is to switch out the 200Ω resistor such that the 1:2 balun is the only component for input matching. As expected, this will degrade the input return loss but improve the NF. The higher input return loss mainly affects the voltage standing wave ratio (VSWR) on the printed circuit board (PCB) traces connecting to the LNA input. The higher VSWR is a significant concern, especially if the discrete component such as a balun or an RF filter preceding the LNA has strict load impedance matching requirement. This is because for non-unity VSWR values, the discrete component will see different load impedance values at different frequencies, resulting in ripples in the frequency domain transfer function, which is highly undesirable, especially for UWB applications. To minimize the variation in VSWR across frequency, caution has to be exercised during PCB design and assembly to ensure that the LNA is placed very close to its preceding board component and therefore the PCB trace length is minimized.

4.1.3 LNA gain staggering

A flat gain response from LNA is needed to make sure that both the interference and the desired signals experience the same gain, similar to what a WiMedia system provides. As mentioned earlier, the design was optimized for sub-2GHz range, given that the technology utilized was 0.18μm. Consequently while this design cannot be used directly for UWB, it is intended to prove the interference cancellation principle.

As shown in Figure 14, both LNA stages in this design use tuned loads formed by an inductor and a resistor in series. While this structure is broadband, it is not adequately so to provide a flat response to cover GHz frequency ranges as indicated by simulation.

To achieve the desired flat response between 1.5GHz and 3GHz range without layout parasitics, peak gain frequencies of LNA1 and LNA2 have been staggered such that the total final gain is relatively flat, as shown in Figure 18.

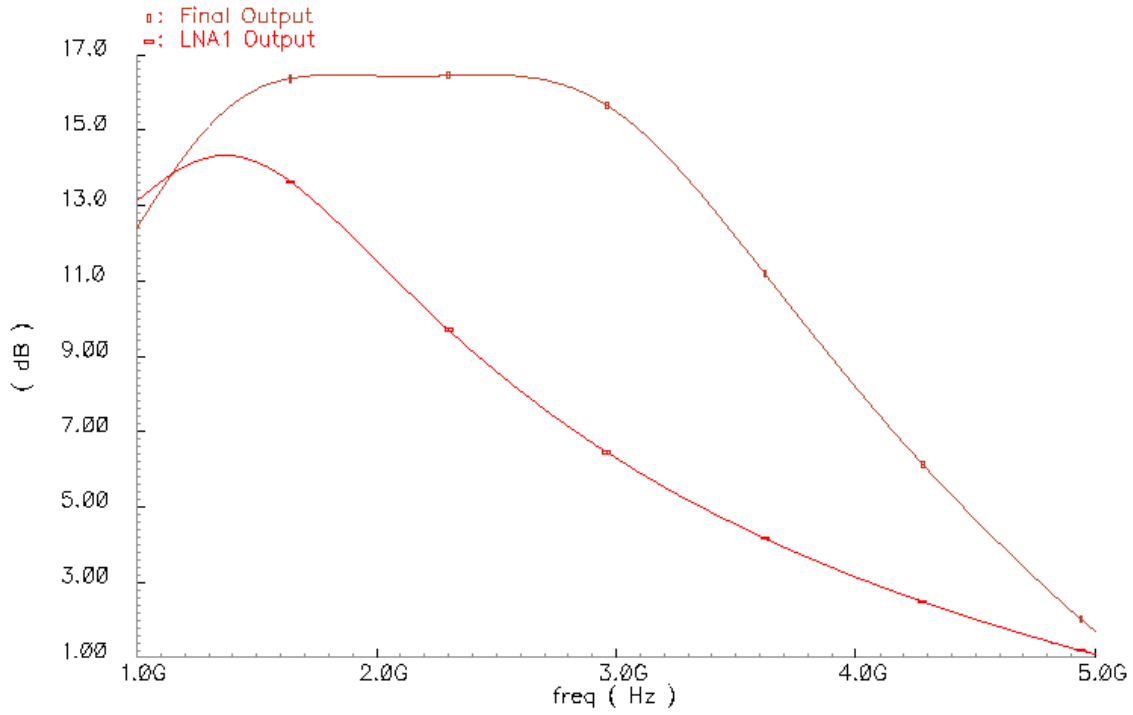


Figure 18: AC analysis simulation plot for LNA design (without layout parasitic). LNA1 output has a peak frequency around 1.4GHz while final output is flat due to the gain staggering from LNA1 and LNA2.

It should be noted that the staggering may complicate the rejection of interference because it experiences different gain line up than the desired signal, if the frequency offset is sufficiently large. This effect will be most noticeable when one of the two signals sees a high enough gain peak from LNA1 that leads to compression of LNA2 input stage while the other signal does not. Therefore caution has to be exercised during

the design and the testing phases such that this potential issue does not mislead the overall analysis.

4.1.5 LNA noise and matching simulation

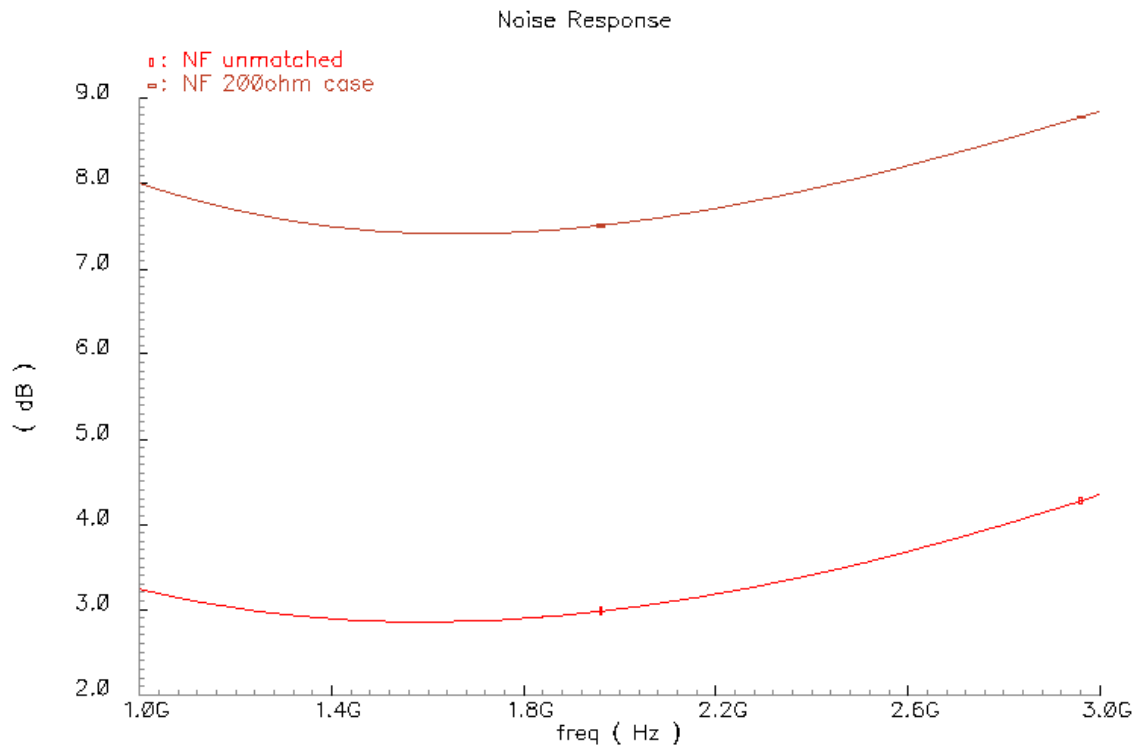


Figure 19: Noise analysis simulation plot for LNA design (without layout parasitics). Simple resistor matching with 200Ω shows much worse NF than the unmatched case (with the 1:2 balun only).

Small signal noise analysis simulation was performed to depict the degradation from the resistive matching using the 1:2 balun and 200Ω resistor on the balanced side. From the single ended input side the resistance would appear to be 50Ω due to the 4:1 impedance transform ratio provided by the balun. The degradation is shown in Figure 19

to be about 4.5dB. Besides noise contribution from the physical 200Ω resistor itself, different input matching condition as well as increased LNA gain in the unmatched case also impacts the difference.

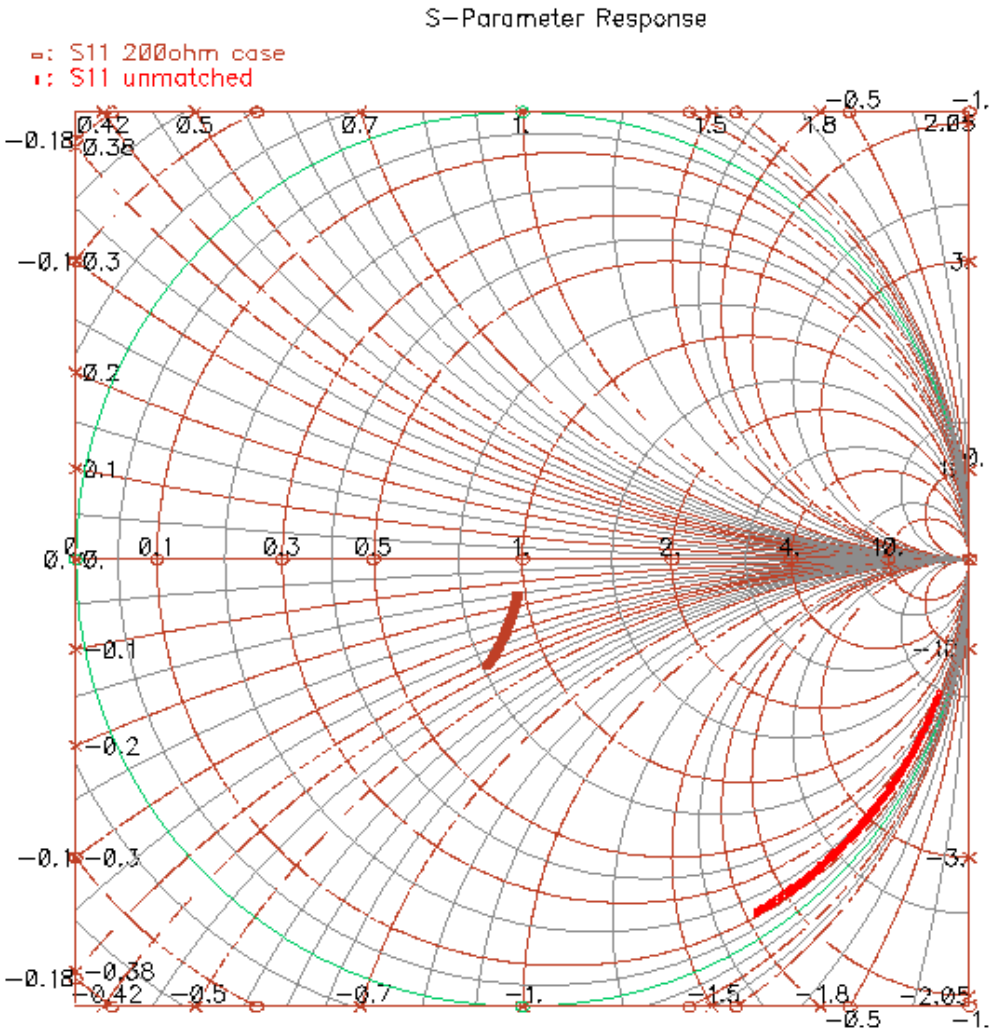


Figure 20: S-parameter analysis simulation plot for LNA design (without layout parasitics). Simple resistor matching with 200Ω shows better S11 than the unmatched case (with the 1:2 balun only).

Simulation results comparing input matching and voltage gain between the resistive matching with 200Ω and unmatched case are shown in Figure 20 and Figure 21, respectively. From Figure 20, in the unmatched case, the input impedance appears as a shunt capacitance with a large real part, while in the 200Ω matching case the input impedance is reflected as a 50Ω resistor in shunt with the same capacitance as expected.

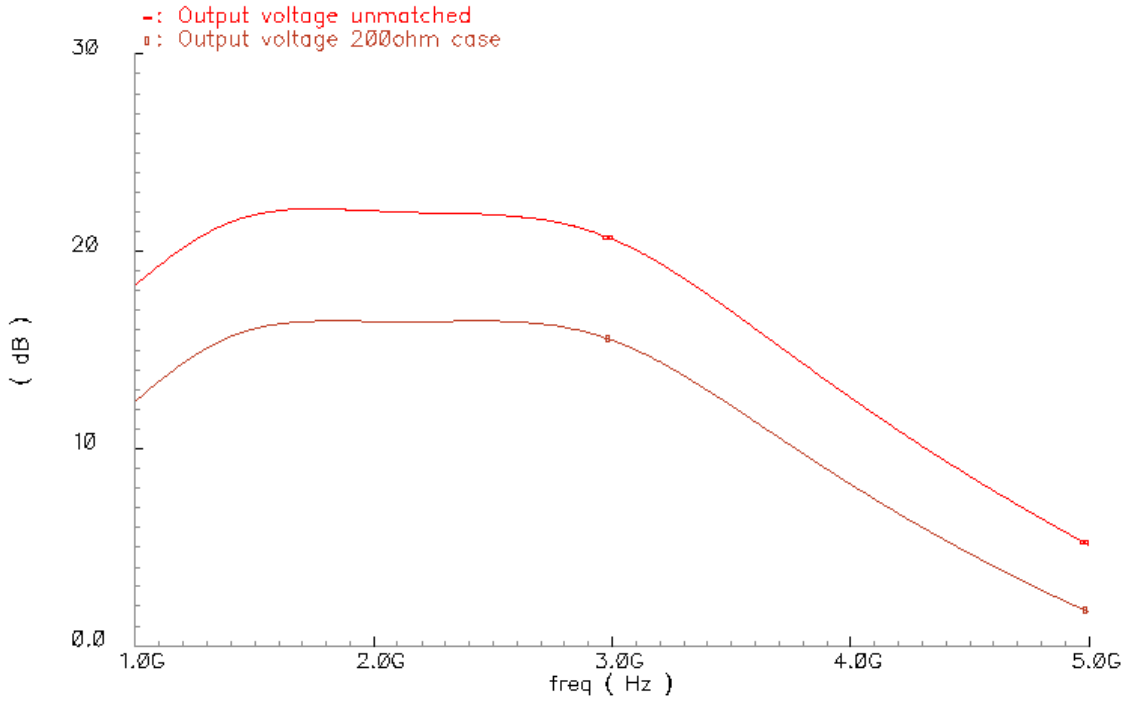


Figure 21: Small signal AC analysis simulation plot for LNA design (without layout parasitics). Simple resistor matching with 200Ω shows lower output voltage than the unmatched case (with the 1:2 balun only).

From Figure 21, the unmatched case has higher voltage gain compared with the matched case. This is because the input voltage actually increases in the unmatched case compared to using a resistive match. It should be noted that the 200Ω resistor is a sub-

optimal match. A better match would be to employ a multi-stage tuned LC, which would in effect provide a large voltage gain from the input of the tuning network to the gate of the input device. The unmatched LNA is ultimately limited in its voltage performance due to shunt capacitance arising from the bond-pads, package and board-traces. Therefore when measured in the lab, the gain difference between the cases with and without the 200Ω was found to be much smaller than predicted by the ideal simulations of Figure 21.

4.1.4 Source follower

To be able to measure the LNA performance off-chip, a source follower block is used as an output driver. To avoid unnecessary attenuation from the traditional source follower structure that will add to high frequency loss, a technique presented in [20] was adopted in this design. A diagram of the source follower is shown in Figure 22.

AC-coupling capacitors are connected between the gates of current mirror devices (M3, M4) to the gates of opposite polarity source follower devices (M2, M1), respectively. Similar to [20], to the first order, the gain of such a source follower device can be given as

$$V_{out+,-} = \frac{g_{m1,2}+g_{m3,4}}{g_{m1,2} + g_{mb1,2} + 1/R_{out+,-}} \cdot V_{in+,-} \qquad (4.6)$$

where $R_{out+,-}$ is the single ended load impedance at the output node $V_{out+,-}$. $g_{m1,2,3,4}$ and $g_{mb1,2}$ are the correspondent transconductance and body transconductance for the respective MOS devices in Figure 22.

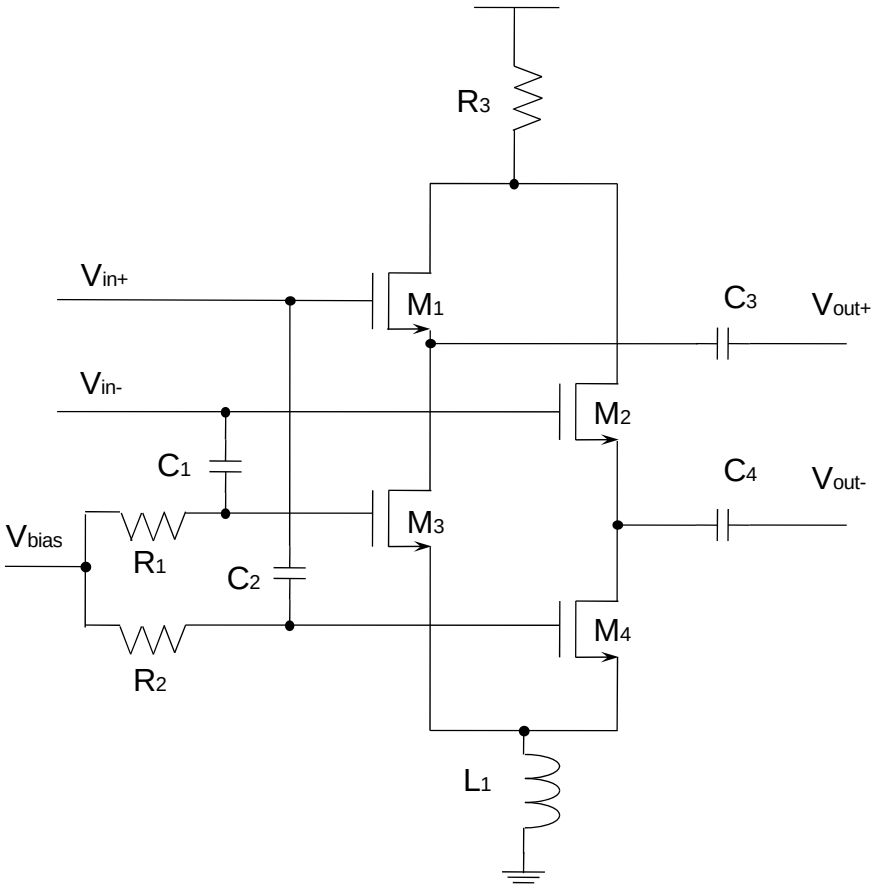


Figure 22: Source follower diagram with positive feedback gain boosting capacitors.

Assuming $g_{m3,4} \sim g_{mb1,2} + 1/R_{out+,-}$, (4.6) shows that the gain of the source follower is boosted by about 6dB to provide unity gain with this technique, if the load impedance $R_{out+,-}$ is assumed equal to $1/g_{m1,2}$ for output matching purpose when $g_{mb1,2}$ is ignored. In reality, even without a perfect matching, the gain boosting is still achieved and therefore desired.

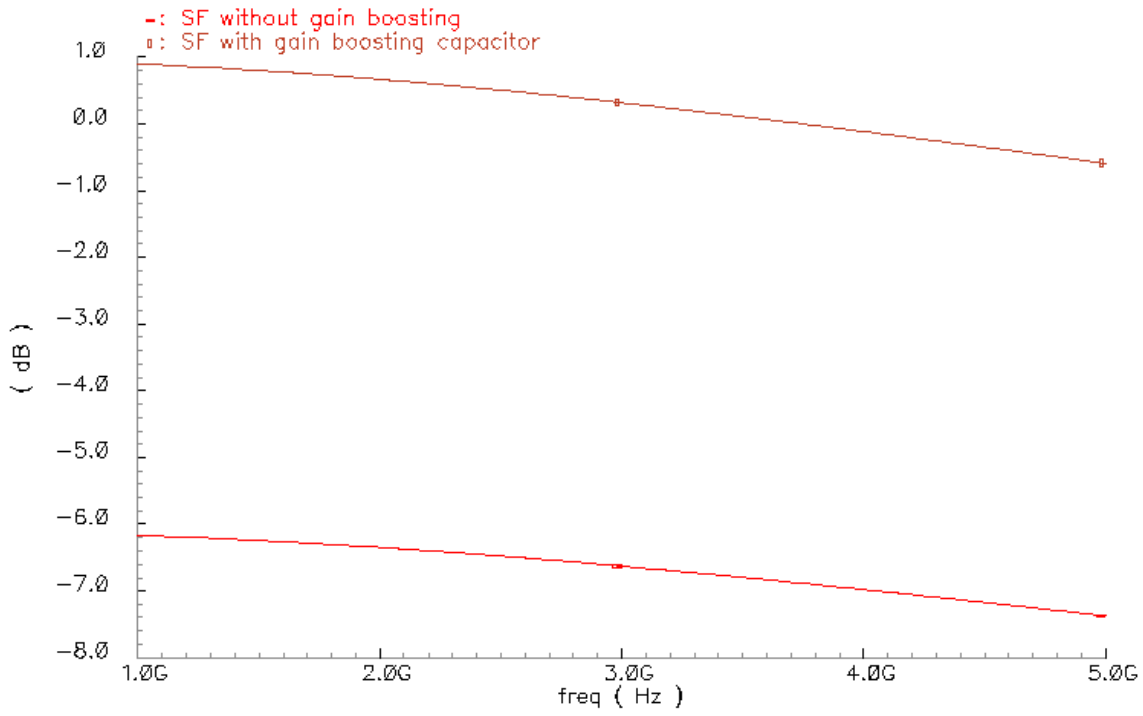


Figure 23: Small signal AC analysis results for source follower circuits with and without gain boosting technique.

The small signal AC analysis result is plotted in Figure 23 to compare the cases with and without the gain boosting. As can be seen, the source follower did achieve close to unity gain with the boosting capacitors and also demonstrated roughly 6dB loss without such technique.

4.2 INJECTION-LOCKED OSCILLATOR (ILO)

As discussed in Section 3.2, the ILO plays the core role of generating linearly independent copies of the signal and interferer in this approach. A study of injection locking has been provided in [15] [16].

Shown in Figure 24, Z_{tank} is the total shunt impedance of the LC tank that presents a purely resistive load at the resonant frequency $\omega_0 = 1/\sqrt{LC}$. Following [15], I_{tank}, I_{mos}, and I_{inj} are the currents of the NMOS device, total LC tank, and the injection block respectively. The gain block with gain of -1 models the cross coupled connection of the NMOS devices in a classical LC tank based oscillator and G_{meff} represents the effective averaged value of the NMOS G_m over one cycle required to maintain the oscillation. Compared with a normal free running oscillator that requires a 360^o phase shift around the loop, the ILO has one extra current injection component but requires the same amount of total phase shift to achieve a stable injected locking oscillation condition.

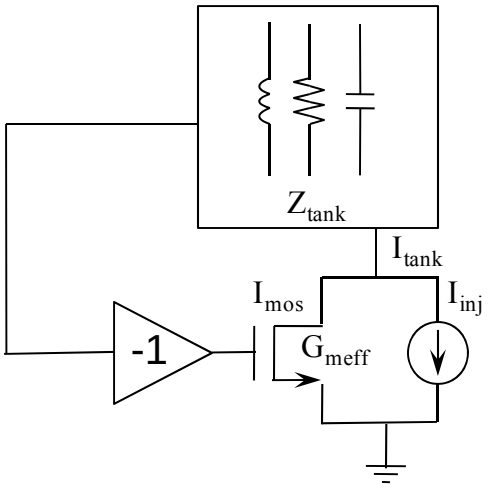


Figure 24: Simplified equivalent circuit model for an ILO.

Figure 25 gives the vector relationship among I_{tank}, I_{mos}, and I_{inj}, which is derived with the 360^o total phase shift around the loop mentioned earlier. In Figure 25(a), the offset between the free running frequency ω_0 and the injection frequency ω_{inj} projects onto the LC tank phase characteristic curve and sets a phase shift ϕ_{inj}. Meanwhile due to

the loop phase condition, the phase difference between the tank current I_{tank} and the NMOS device drain current I_{mos} also equals to ϕ_{inj}, assuming no phase shift from the effective transconductance G_{meff}.

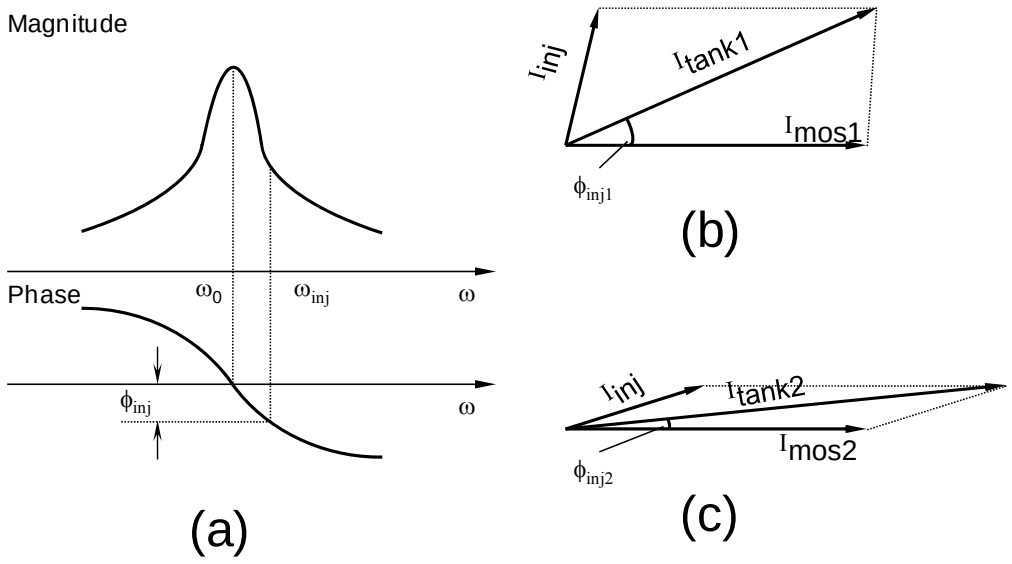


Figure 25: ILO phasor diagram. (a) Magnitude and phase of the tank impedance versus frequency. (b) Vector diagram 1. (c) Vector diagram 2 with a different phase offset.

Figure 25(b) and 25(c) shows the vector relationship of I_{tank}, I_{mos}, and I_{inj}, with different value of ϕ_{inj}, which is also described by the following equation

$$I_{tank} = I_{mos} + I_{inj} \tag{4.7}$$

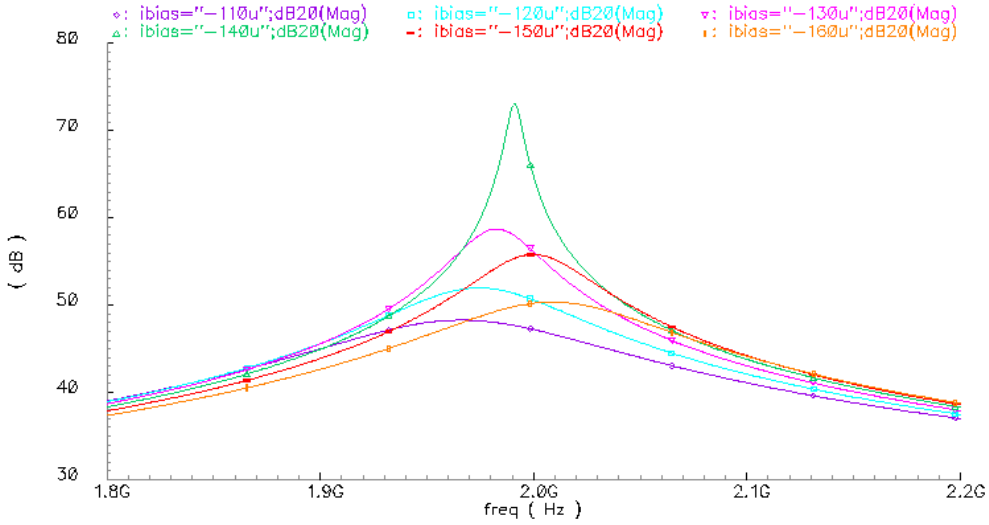
4.2.1 ILO topology description

The ILO schematic has been shown in Figure 12 in last chapter. It is formed by a conventional LC based oscillator with cross coupled NMOS devices to provide the small signal negative resistance required to offset the parasitic resistance of the tank. A common source injection stage is used with resistive source degeneration. The degeneration is necessary to make sure that the ILO itself does not compress before the RF down conversion mixer. The oscillator core has a large headroom and therefore the linearity bottle neck is the injection stage. It should be noted that the injection stage does not require much gain.

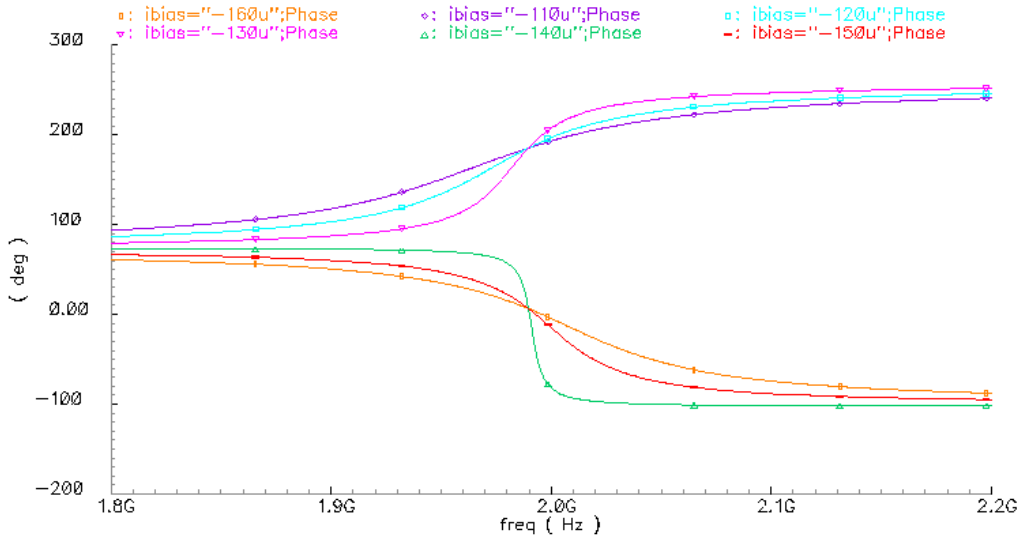
The LC tank is formed with spiral inductors and analog varactors along with digitally programmable metal-insulator-metal (MIM) capacitors. High quality factor (Q) inductors and capacitors are desired for the LC tank. However, varactors have relatively low Q factor due to the gate resistance. When switching in MIM capacitors, the series resistance from CMOS switches also degrades the quality factor (Q) and the bias current of ILO has to be adjusted to keep that relatively constant in order not to further complicate the PLL design, as will be shown later with simulation results.

The strength of the negative resistance determines the oscillation magnitude and must be programmable to achieve the goal of good interference cancellation. There are two ways to program this. One is to adjust the total bias current of the ILO, which changes the transconductance of the cross coupled NMOS devices, and thus the negative resistance. The other way is to program the aspect ratio of the cross coupled NMOS devices.

4.2.2 Tank impedance versus bias current



(a)



(b)

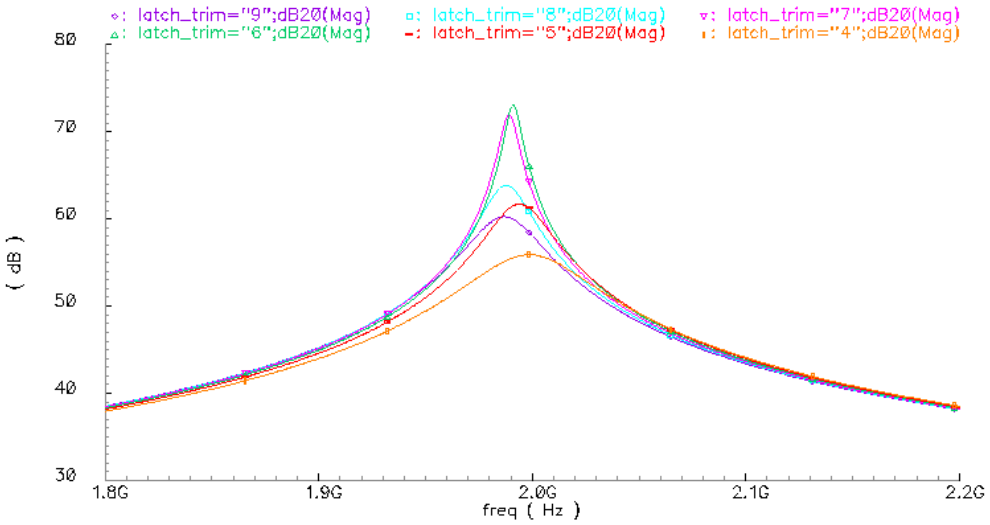
Figure 26: ILO tank impedance versus bias current sweep. (a) Magnitude in dB. (b) Phase.

Small signal impedance of the loaded ILO LC tank was studied by injecting an AC current into the ILO output nodes and monitoring the resultant AC voltage level. The simulation results for both magnitude (in dB) and phase of the LC tank impedance are shown in Figure 26(a) and 26(b). The bias current was swept from -160uA to -110uA in 10uA steps. The built-in bias circuit provided over 200uA to the ILO and therefore to observe the change in the polarity of the impedance, a negative extra bias current is needed. On the real PCB board setup, the extra negative bias current can be realized by connecting a resistor from the ILO bias pad to an adjustable voltage potential.

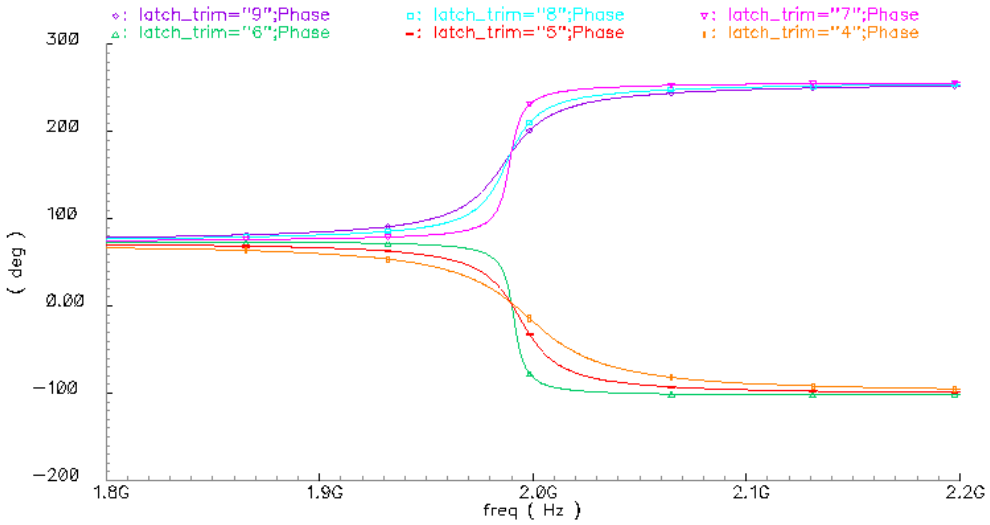
From the phase plot in Figure 26(b), the polarity of the impedance at resonance around 2GHz changes between the bias level of -140uA and -130uA. To be specific, the impedance phase at resonance appeared as 0 degree for the applied bias levels of -160uA, -150uA, and -140uA but was 180 degree for the bias levels -130uA, -120uA, and -110uA. Corresponding to this change, in Figure 26(a) the impedance magnitude at resonance was observed to peak when the bias level was -140uA, with the next largest peak at -130uA, confirming that small signal negative impedance provided by the cross coupled NMOS devices reached a level very close to the parasitic shunt impedance of the physical LC tank at approximately these two bias levels.

Note that these are small signal analysis impedance levels only. To obtain a sustainable oscillation which is a large signal behavior, the bias level should provide some margin to allow the average negative impedance during one full cycle to compensate the energy dissipated in the parasitic tank loss, which occurs at a larger positive bias current level from the perfect cancellation point in small signal analysis.

4.2.3 Tank impedance versus NMOS aspect ratio



(a)



(b)

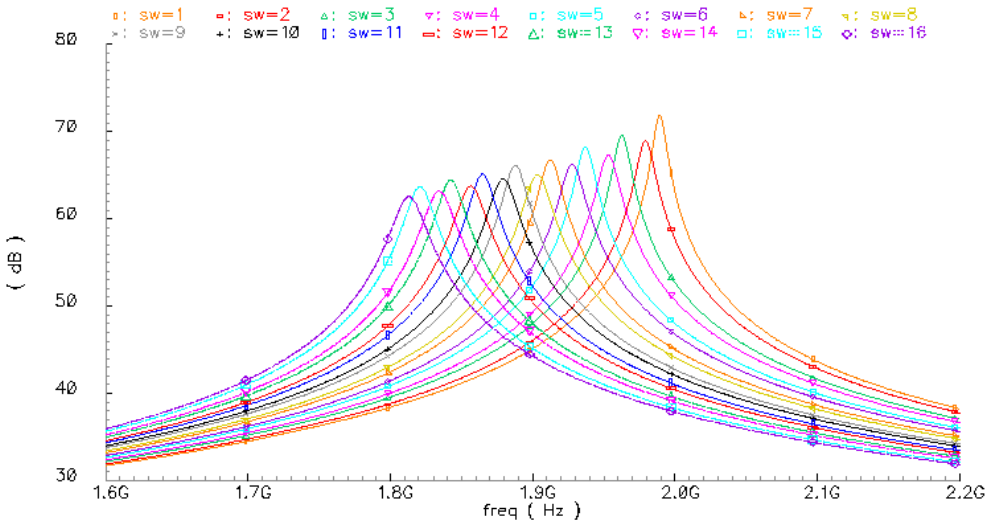
Figure 27: ILO tank impedance versus cross coupled NMOS aspect ratio sweep. (a) Magnitude in dB. (b) Phase.

Similarly, loaded tank impedance can be varied by changing the aspect ratio of the cross coupled NMOS devices. In the design, 16 identical parallel unit cells were implemented as the NMOS device and can be independently switched in and out to provide different transconductance levels.

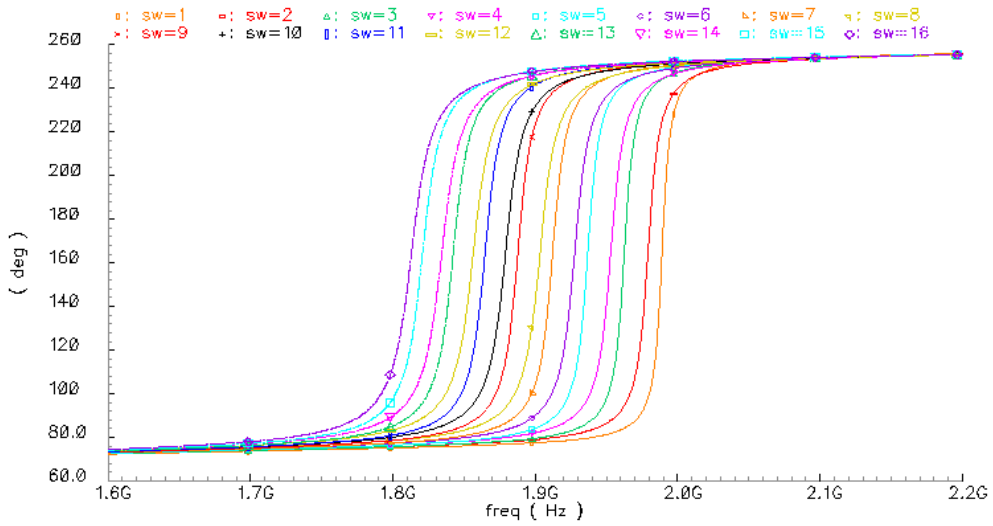
As shown in Figure 27(a) and 27(b), 4 to 9 unit cells were switched on incrementally to present a change in the polarity of the resonance impedance between the cases where 6 and 7 unit cells were turned on. Similar magnitude (in dB) and phase plots were obtained to the ones shown in Figure 26.

4.2.4 Tank impedance versus digital capacitor programming

As mentioned earlier, the center frequency of the LC tank can be programmed both digitally with series switches and capacitors as well as with analog varactor tuning. For digital switching, to offset degradation of quality factor (Q) due to CMOS switch resistance, the ILO bias current is adjusted accordingly when more switches are turned on in order to keep a relatively flat response, as shown in Figure 28(a) and 28(b).



(a)



(b)

Figure 28: ILO tank impedance versus digital capacitor programming sweep. (a) Magnitude in dB. (b) Phase.

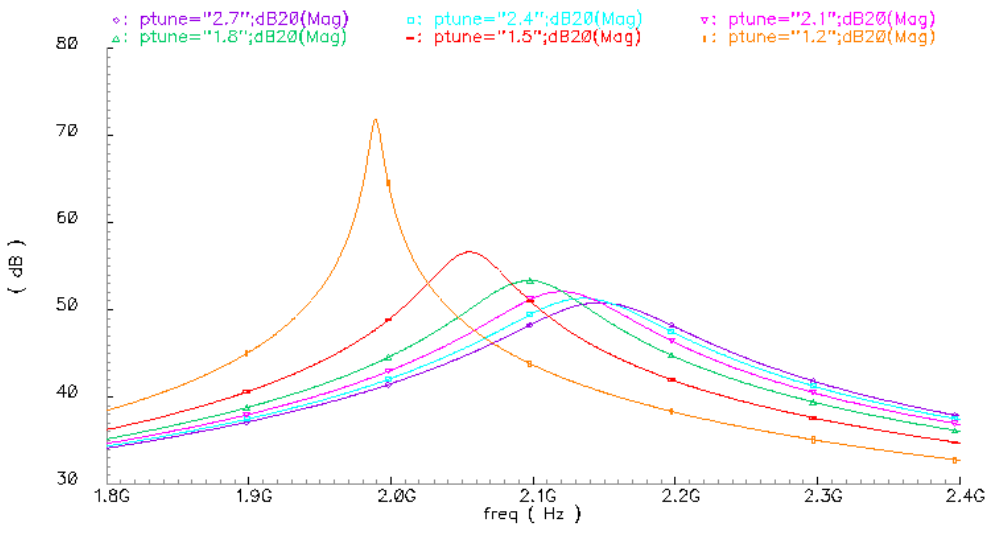
A total of 16 thermometer code settings were implemented in the design. The entire programmable frequency range that was obtained through digital switching is shown to be close to 200MHz. While it is possible to expand the digital programmable range by adding more switch and capacitor branches, the range is effectively limited by the quality factor (Q) degradation mentioned earlier. For a more advanced technology with shorter channel length, the on-resistance of the device is smaller per unit width of the device. It is thus possible to expand the digital trimming range by using smaller switch devices, which are desirable due to their correspondingly lower parasitic capacitance.

4.2.5 Tank impedance versus analog varactor programming

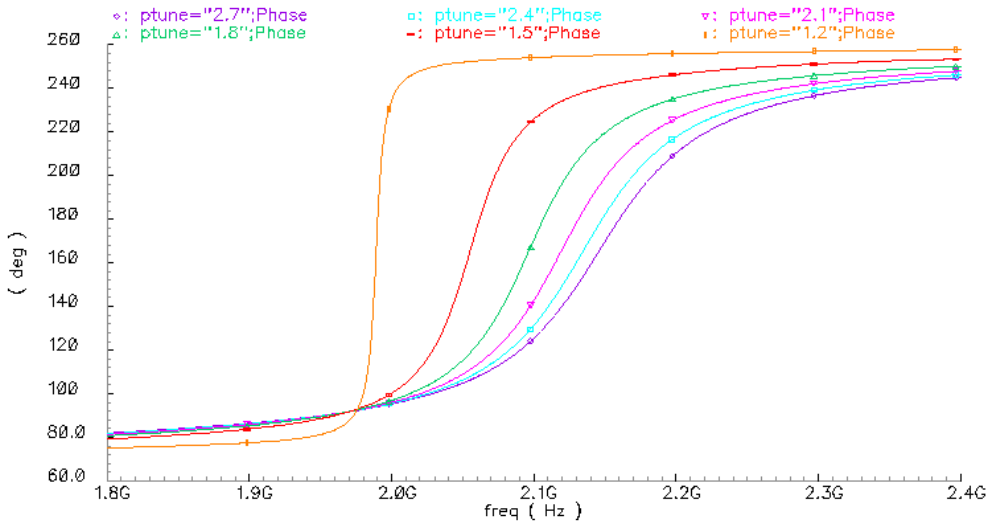
Besides the digital capacitor programmability, varactor tuning is also available for the analog control of the VCO and PLL locking. As shown in Figure 29, the analog

tuning range is approximately150MHz for this design. One noticeable effect during the varactor tuning voltage sweep is that the loaded quality factor (Q) of the oscillator varies. The loaded quality factor (Q) includes the contribution from all impedance tied to the LC tank, such as cross coupled NMOS and gate capacitance of the load stage. This is in contrast to the intrinsic Q factor of the LC tank where only parasitic resistance from the tank itself is considered.

Besides a reduced Q factor of the tank inductor, the parasitic gate resistance of varactors can also be used to account for the Q factor degradation at lower frequencies that correspond to lower tuning voltages. Referring to the ILO schematic shown in Figure 12, we observe that the anode of the varactor is DC shorted to the 1.8V power supply through an inductor and the tuning voltage controls the cathode of the varactor. Therefore for lower tuning voltages, the varactor becomes less reverse biased and presents a higher capacitance, which degrades the overall Q.



(a)



(b)

Figure 29: ILO tank impedance versus analog varactor tuning sweep. (a) Magnitude in dB. (b) Phase.

4.2.6 Phase shift versus injection frequency

As mentioned at the beginning of Chapter 3, one of the goals in the design of this architecture was to include gain and phase control within the implementation. Gain control is necessary not only to equalize the magnitude of the auxiliary path and the main signal path, but also to address amplitude modulation (AM) based interference signals. However, phase calibration is automated in this approach by aligning the ILO resonance frequency at the center of the interferer.

The LC tank impedance is purely resistive at the resonant frequency, and thus no phase shift is observed in its current to voltage transfer function. The transconductor devices in the injection block also should not provide significant phase shift from their voltage to current transfer function to the first order, if the devices are sized to ensure that

the charge transfer in the device capacitors does not have a significant impact on the transfer function.

Based on this observation, by embedding the ILO within a PLL it is possible to achieve automatic phase alignment between the input and output voltage signals of the ILO while tuning the ILO center frequency towards the interference signal. The ILO preferentially amplifies the interference signal, which is near the resonant frequency of the LC tank, relative to the desired signal which is at a sideband. Thus its output and input signals can be applied directly to the second stage of the LNA (LNA2) to achieve interference cancellation without any extra phase calibration. Amplitude equalization is still required and can be done by monitoring the interference level at the output stages of the receiver, such as in the baseband, while tuning the ILO bias level.

Meanwhile, to compensate for the phase offset that appears between the ILO injection block input voltage and output drain current signals, due to the flow of current into the parasitic capacitance at the drain node, the tank impedance has to provide the same amount of phase offset. When the effective loaded quality factor Q of the LC tank is increased, a smaller frequency offset is needed to achieve the desired phase offset and therefore the resonance frequency moves closer to the interference frequency, which is desired. Otherwise for large values of the Q factor, if the frequency offset is large, the interference signal will be amplified by a relatively smaller value, even if the ILO bias is increased.

In small signal analysis, to guarantee the oscillation can start successfully, the total shunt impedance of the LC tank has to be real and negative. As the oscillation builds up, the net impedance assumes negative real values for part of the cycle that compensates for the energy lost in the positive real impedance near the zero crossing of oscillator output. Referring to the LC tank impedance simulation plots in Figure 26 – Figure 29, it

would appear that the effective impedance of the tank decreases for large negative values of the impedance, since the phase function becomes progressively smoother. It should be noted that this negative value is observed near the zero crossing. In order to compensate for a more conductive negative part of the impedance near the zero crossing, the amplitude would need to increase, to ensure that the net energy delivered to and dissipated in the tank is zero in one cycle, even though the smoother phase function may lead one to intuit otherwise. Ultimately the amplitude will be limited by the amount of bias current used in the oscillator.

4.2.7 Rejection of sidebands

Employing an ILO instead of a passive LC filter helps to increase the rejection of the desired signal prior to LNA2. Although a passive LC filter provides certain selectivity, it is very difficult to make its center frequency tunable at RF without incurring significant degradation of tank Q due to switch resistance or other potential parasitic effects depending on how the tuning is implemented. For the case of ILO, the Q degradation can be overcome with the negative resistance provided by the cross coupled MOS devices. Furthermore, since the ILO combines a passive LC tank with the shunt impedance of the active (negative) transconductance devices, more rejection over the desired signal at a sideband can be achieved compared to a purely passive filter.

To elaborate on the second point mentioned above, it is helpful to revisit the concept of average impedance in the linearized model (over one cycle of oscillation). While the analysis is approximate, it is intended to provide an insight into sideband suppression as a function of the injection current. As mentioned earlier in this chapter, the average transconductance of the cross coupled NMOS device is denoted as G_{meff} and the

following relationship can be used as a reference as how the averaging should be carried out.

$$I_{tank} \cdot Z_{tank} \cdot G_{meff} = I_{mos} \tag{4.8}$$

where Z_{tank} is the total impedance of the passive LC tank by itself.

Also as shown in Figure 25, vector balance of tank current I_{tank}, NMOS current I_{mos}, and injection current I_{inj} can be expressed by equation (4.7). For the case where injection frequency ω_{inj} is very close to the free running tank resonance frequency ω_0, the phase offset between these vector currents also becomes negligible. Therefore as an approximation, the scalar version of (4.7) also holds as $I_{tank} = I_{mos} + I_{inj}$. Strictly speaking, $I_{tank} = I_{mos} - I_{inj}$ can also become a solution for the scalar version of (4.7). However, Mirzaei et al. [21] pointed out that this is not a stable solution.

As a special case, when there is no injection input, the self running oscillator yields $I_{tank} = I_{mos}$. Replacing I_{tank} with (4.8), it follows that

$$R_{tank} \cdot G_{meff}^{0} = 1 \tag{4.9}$$

where G_{meff}^{0} is the average transconductance for the free running case and R_{tank} is the tank impedance at resonance. (4.9) has another physical interpretation if rewritten as $G_{meff}^{0} = 1/R_{tank}$, which shows the that large signal negative resistance exactly cancels out positive tank resistance to sustain the oscillation. In a similar manner, the following equation can be obtained for the case when the injection input is nonzero.

$$I_{inj} = I_{tank}^{inj}(1 - R_{tank} \cdot G_{meff}^{inj}) \tag{4.10}$$

where I_{tank}^{inj} and G_{meff}^{inj} represent the tank current and average NMOS transconductance under the injection condition. For a nonzero I_{inj}, from (4.10) one can infer that

$$R_{tank} \cdot G_{meff}^{inj} < 1 \tag{4.11}$$

Comparing (4.9) and (4.11), it is clear that $G_{meff}^{inj} < G_{meff}^{0}$. Further by rewriting (4.10) in the form $I_{inj} = I_{mos}(1/R_{tank}G_{meff}^{inj} - 1)$, we observe that G_{meff}^{inj} must decrease as the injection level increases, under the constraint that I_{mos} stays unmodified to the first order, for the case where current clipping is observed. For a sideband input current signal from the injection port, the effective trans-impedance consists of a parallel combination of the tank impedance at the sideband frequency in shunt with the negative impedance given by G_{meff} and is given by

$$Z_{sb} = \frac{-\frac{Z_{tank}^{sb}}{G_{meff}}}{Z_{tank}^{sb} - \frac{1}{G_{meff}}} = \frac{Z_{tank}^{sb}}{1 - Z_{tank}^{sb} \cdot G_{meff}} \tag{4.12}$$

Since G_{meff} decreases with increasing level of the main injection tone at resonant frequency, the sideband input signal incident along with the main injection tone from the injection port should thus decrease in amplitude as the amplitude of the main injection tone increases.

To verify the above reasoning, a Cadence Specter PSS-PAC simulation was run and the result is shown in Figure 30. The PSS was run for either the free running oscillation mode where the main injection tone is zero or for the injection-locking mode. The sideband response is simulated using PAC simulation.

As shown in Figure 30, when the injection tone current is swept from 0 to 20mA in 2mA steps, the oscillator output frequency is relatively constant as expected as the large injection tone is at a frequency very close to the free running oscillation frequency. Output level for the injection tone increases with the input tone itself, which is expected. The sideband tone, assumed to be at 100MHz offset frequency shows decreasing output level, except for the two lowest settings. The behavior at low injection levels needs further investigation. However, as the injection level is increased, the increasing rejection of the sideband is clearly observed.

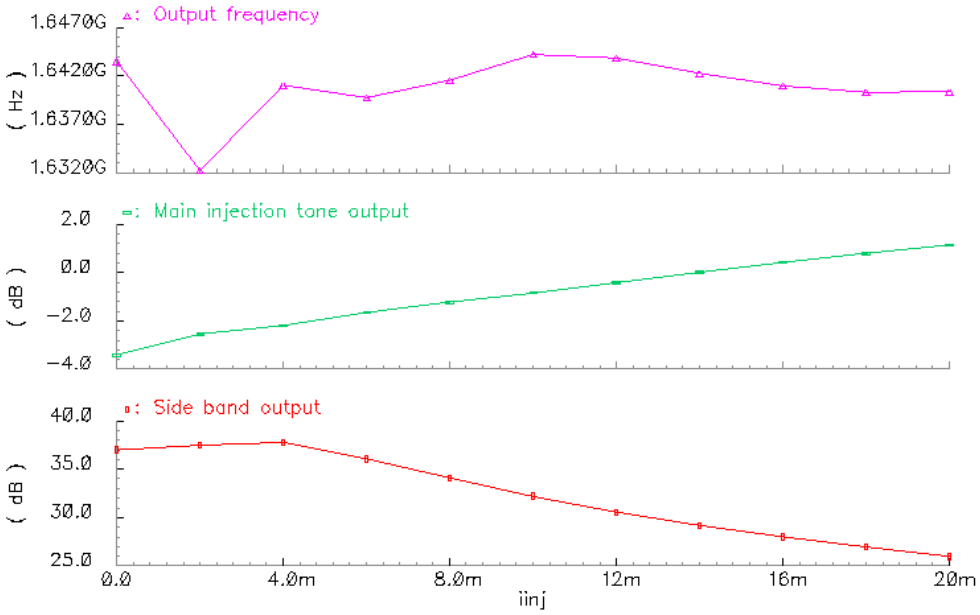


Figure 30: PSS-PAC simulation result for sideband response when the resonance frequency injection tone is swept.

The trans-impedance gain for the sideband current input is given by equation (4.12). For the main injection tone close to the resonance frequency, using equation (4.10), the gain from injection current to ILO output can be expressed as

$$\frac{V_{inj}}{I_{inj}} = \frac{(I_{tank}^{inj} \cdot R_{tank})}{I_{tank}^{inj}(1 - R_{tank} \cdot G_{meff}^{inj})} = \frac{R_{tank}}{1 - R_{tank} \cdot G_{meff}^{inj}} \qquad (4.13)$$

Comparing (4.13) with (4.12), the I-V relations for the main injection tone close to resonance and the sideband tone have the same form, except that different tank impedance is seen by different tones. With increasing ILO bias current or higher aspect ratio of the cross coupled NMOS devices, G_{meff}^{inj} will become larger. Based on (4.12) and (4.13), both the sideband tone and the main injection tone should increase with G_{meff}^{inj}. However, since the sideband tone sees a much lower Z_{tank} due to roll off of the tank reactance at the sideband frequency, the impact of the increase in G_{meff}^{inj} will be relatively smaller. Therefore it can be predicted that with increasing ILO bias current, the main injection tone at resonance increases by a relatively larger amount than the sideband tone.

Simulation data shown in Table 1 for the full design confirmed this prediction. The two tone input signal from the injection block experienced different gains from the ILO block, as shown in equations (4.12) and (4.13) mainly due to different tank impedance seen at different frequencies. For accurate verification of the above discussion, it is important to make sure that the main injection tone stays very close to the free running resonance frequency of the LC tank ω_0. Since device parameters including parasitic capacitance vary with the bias current, it is difficult to track ω_0 with a fixed main injection tone frequency. Therefore the top level loop simulation where the PLL adjusted the LC tank frequency toward the injected interference frequency was used to obtain the data in Table 1.

The left column (except for the first data row) shows the incremental ILO bias from the starting point (not shown) with a shunt resistor to ground. The middle column

shows the corresponding sideband output level and the right column shows the corresponding main injection tone output level, except for the first data row. The first data row gives the signal levels of both tones at the input of the injection block (and thus also the ILO).

Extra ILO Bias (A)	Sideband Tone (dBV)	Main Injection Tone (dBV)
Input	-27.46	-9.58
1.00E-05	-65.53	-21.14
2.00E-05	-65.26	-19.49
3.00E-05	-65.06	-17.57
4.00E-05	-64.92	-16.11
5.00E-05	-64.8	-14.93
6.00E-05	-64.71	-13.96
7.00E-05	-64.65	-13.11
8.00E-05	-64.6	-12.38
9.00E-05	-64.57	-11.72
1.00E-04	-64.54	-11.12
1.10E-04	-64.52	-10.58
1.20E-04	-64.5	-10.07
1.30E-04	-64.48	-9.6
1.40E-04	-64.45	-9.15
1.50E-04	-64.42	-8.73
1.60E-04	-64.38	-8.34

Table 1: Response of main injection and sideband tones from full loop simulation when ILO bias is increased.

As shown by the data, with the increasing ILO bias current from 10uA to 160uA, the main injection tone output changed from -21.14dBV to -8.34dBV that eventually exceeded the input level of -9.58dBV. Meanwhile, the sideband tone (at 500MHz offset)

almost stayed constant around -65dBV for a -27.46dBV input level. The trend confirmed the prediction based on equations (4.12) and (4.13) very well.

This behavior is in fact similar to the improvement in phase noise which one would expect as the bias current in an oscillator is increased, as long as the oscillator is not voltage limited. As such, we can anticipate that much of the literature and approaches devoted towards analysis of phase noise can be applied here, and are a good area for future investigation.

4.2.8 More on the estimation of oscillation magnitude

Using the proposed average transconductance/impedance model, several important trends can be explained and verified by simulation as shown above. More rigorous derivations on ILO analysis using differential equations and/or numerical methods have been attempted in the past [15, 21-25]. In [26], Dehghani et al. (2003) proposed an analytical method with a simplified oscillator circuit model to predict oscillation amplitude that correlated to simulation result quite well.

A point to note is that for current clipped oscillators, the NMOS device current magnitude I_{mos} can be approximated by $4I/\pi$ using the Fourier coefficient of the fundamental frequency [21], where I is the total bias current from the tail device of the oscillator. This approximation, however, can be shown to be approximate, mainly due to the parasitic capacitive charging and discharging currents. For qualitative explanations, it is still useful to refer to it (with an empirical scaling factor to account for the parasitic currents if necessary) to assume a fixed I_{mos} amplitude.

4.3 PHASE DETECTOR (PD)

The phase detector (PD) is one of the core components for a phase locked loop (PLL). In typical frequency synthesizer applications of PLLs, the PD is normally

operated at low frequencies, and used to compare the reference clock frequency and the divided down version of the oscillator clock frequency. Therefore many implementations are possible, including an XOR logic gate.

For this design, phase comparison between the injection input signal and ILO output signal needs to be performed at RF, which makes it inappropriate to use a PD based on low speed CMOS XOR logic gates. Instead, a Gilbert cell based multiplier is used to generate the phase offset information. As discussed in Chapter 3 briefly, a traditional Gilbert cell multiplier with low pass filter has zero output voltage when the input signals are 90^o apart from each other, and therefore cannot be used directly for the PLL for this work that requires perfect phase alignment between the two input signals. As a consequence, a custom dual cell Gilbert cell PD was implemented as shown in Figure 13 with the desired transfer function.

4.3.1 Traditional mixer-based PD

From Figure 13(a), the PD cells have a built in low pass filter with the shunt R-C load, which attenuates the high frequency signals. Let us express two input signals applied to the PD as:

$$\begin{aligned} V_1 &= A_1 \cdot \sin(\omega_1 t + \varphi_1) \\ V_2 &= A_2 \cdot \sin(\omega_2 t + \varphi_2) \end{aligned} \tag{4.14}$$

Multiplying the two equations in (4.14), the output voltage V_{out} can be obtained as below

$$V_{out} = \frac{1}{2} A_1 A_2 \cdot \{\cos[(\omega_1 - \omega_2)t + (\varphi_1 - \varphi_2)] - \cos[(\omega_1 + \omega_2)t + (\varphi_1 + \varphi_2)]\}$$

Due to the built-in low pass filter at the output of the PD, the high frequency term at $\omega_1 + \omega_2$ is mitigated and the above equation can be approximated by

$$V_{out} \sim \frac{A_1 A_2}{2} \cdot \cos[(\omega_1 - \omega_2)t + (\varphi_1 - \varphi_2)] \quad (4.15)$$

For two input signals at the same frequency, (4.15) reduces to a simple *cosine* function of the phase difference $\varphi_1 - \varphi_2$ in (4.16) and the origin of the 90^o phase offset at the zero crossing locations can be thus understood.

$$V_{out} = \frac{A_1 A_2}{2} \cdot \cos(\varphi_1 - \varphi_2) \quad (4.16)$$

4.3.2 Non-ideal high frequency behavior in Gilbert cell

As mentioned in Chapter 3, another reason why a traditional Gilbert cell multiplier cannot be directly applied for this design lies in its high frequency behavior. At low frequency, the zero crossing point for the PD output occurs when the two input signals have 90^o phase offset as can be seen from equation (4.16). For high input signal frequencies e. g. in the GHz range, the zero crossing is no longer observed at an exact 90^o phase offset, mainly due to parasitic capacitance at different nodes in the Gilbert cell.

As shown in Figure 31, while lower frequency (100MHz) input signals result in zero crossing points near 90^o, which corresponds to a quarter of the clock cycle in the plot, higher frequency input signals clearly have zero crossing points that deviate from

that location. For example, when the input frequency is 3.162GHz, the plot shows a zero crossing around 0.4 clock cycle, or 144^{o}.

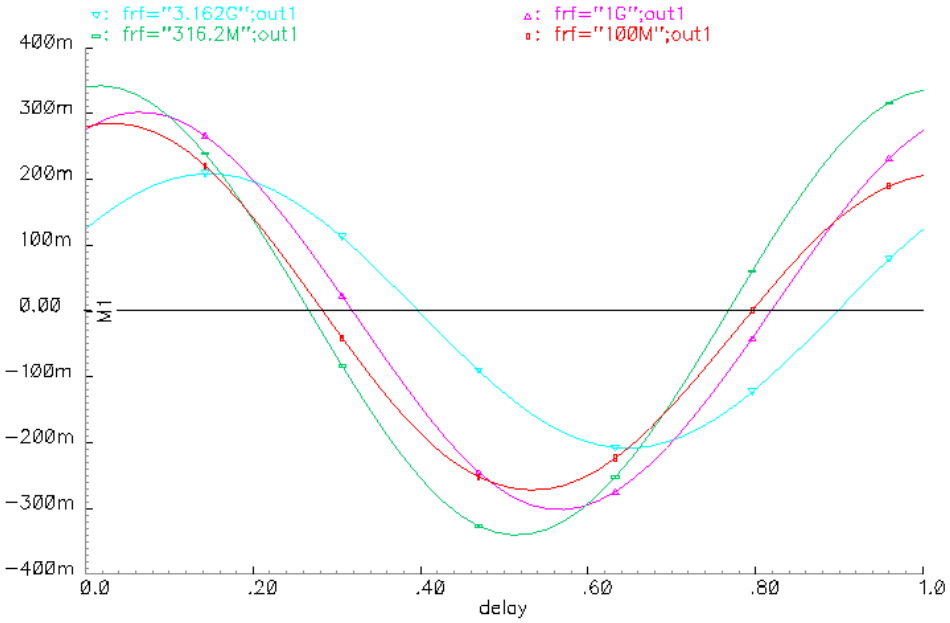


Figure 31: Traditional Gilbert cell output has different zero crossing points when signal frequency goes higher into the GHz range.

4.3.3 Dual cell PD simulation

To overcome the above non-ideality and provide a zero crossing point at zero phase offset between the input signals, a dual cell PD was introduced as shown in Figure 13(a) and described in Chapter 3. To verify that the new design does meet the expected transfer function shown in Figure 13(b), a simulation plot is provided in Figure 32.

As shown in Figure 32, while both individual cell output ‘out1’ and ‘out2’ deviate significant from the 90^{o} zero crossing point, the final output ‘delta’ taken as the difference between ‘out1’ and ‘out2’ shows perfect zero crossing points at 0^{o} and 180^{o}.

Zero crossing points for ‘delta’ appear exactly at 0^o and 180^o because ‘out1’ and ‘out2’ curves are actually mirror images around the vertical axis located at ‘$x = 0.5$’ in Figure 32.

To gain some insight into this behavior, assuming the extra phase delay introduced by parasitic capacitance and the extra capacitor to be $\Delta\varphi$ that is frequency dependent, ‘out1’ and ‘out2’ curve can be written as

$$V_{out1} = \frac{A_1 A_2}{2} \cdot \cos(\varphi_1 - \varphi_2 + \Delta\varphi)$$
$$V_{out2} = \frac{A_1 A_2}{2} \cdot \cos(\varphi_2 - \varphi_1 + \Delta\varphi) \qquad (4.17)$$

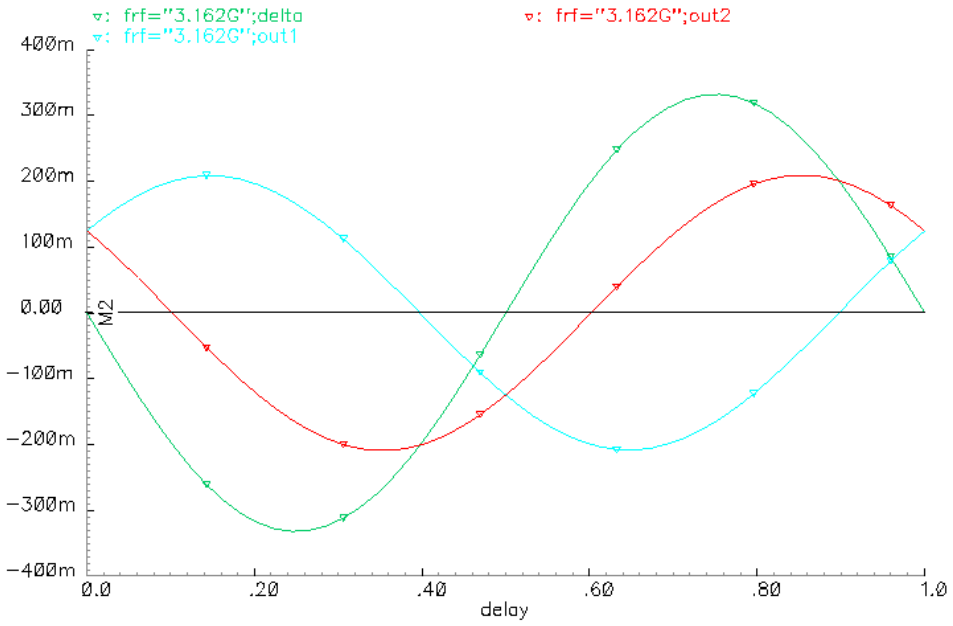


Figure 32: Output signal ‘delta’ of the proposed dual cell PD.

From (4.17), when $\varphi_1 - \varphi_2$ is swept from 0 to 360°, phase of the 'out1' curve changes from $\Delta\varphi$ to $360^o + \Delta\varphi$, while phase of 'out2' curve changes from $\Delta\varphi$ to $\Delta\varphi - 360^o$, or alternatively from $360^o + \Delta\varphi$ to $\Delta\varphi$, clearly a mirrored image of 'out1'.

There should be no ambiguity arising from the two zero crossing points because the 'delta' curve is always negative between 0° and 180° and positive between 180° and 360°, and therefore a correct choice of the charge pump polarity can always guarantee that the PLL will settle to the desired phase offset point, which is 0° in this design.

4.3.4 Effect of intentional capacitors at common mode nodes

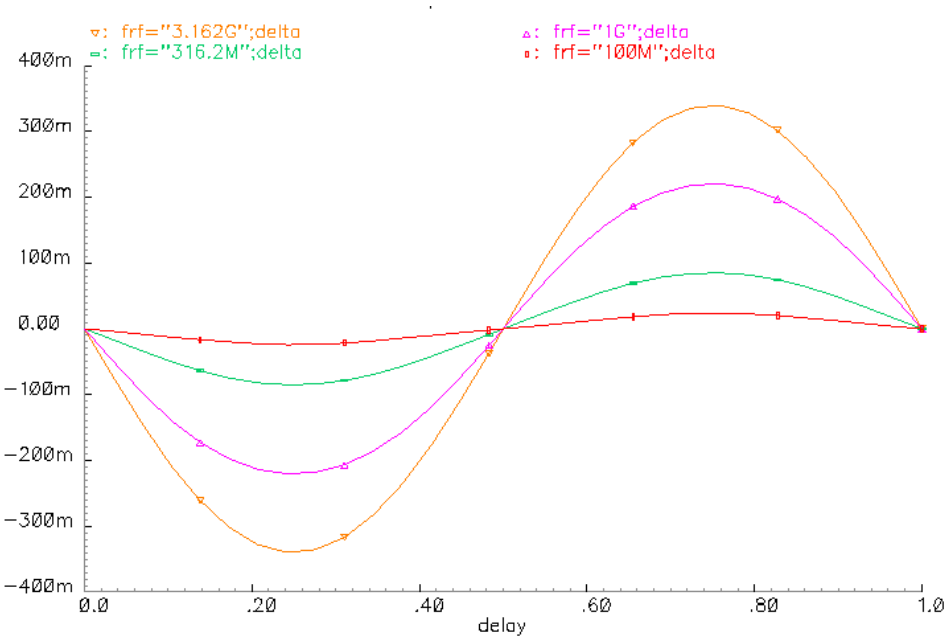


Figure 33: Output signal 'delta' versus input signal frequency for 1fF extra capacitor.

From equation (4.16), it can be seen that without the parasitic phase offset effect at high frequency discussed in Section 4.3.2, 'out1' and 'out2' curves in Figure 32 will

actually overlap with each other and generate a zero curve for ‘delta’. Therefore in the new PD design, the parasitic capacitance becomes necessary and to enhance this effect, intentional capacitors were added to common mode nodes in the Gilbert cells, as discussed earlier in Chapter 3.

To illustrate the effect of the parasitic cap on the ‘delta’ output signal, Figure 33 shows ‘delta’ for different input signal frequencies. It is clear that at lower frequency case such as 100MHz, the ‘delta’ curve is close to zero regardless what the input offset is.

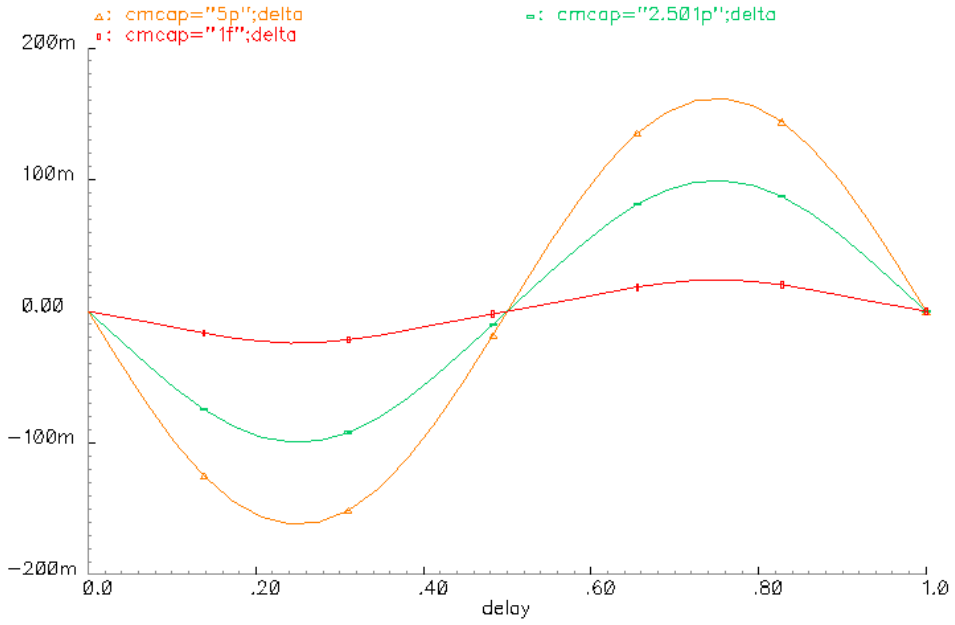


Figure 34: Output signal ‘delta’ versus added intentional capacitor size for 100MHz input.

Another way to examine this effect is to sweep the added intentional capacitor size for the 100MHz case. Based on the above discussions, larger extra capacitors cause larger deviation for ‘out1’ and ‘out2’ from the 90^{o} zero crossing point at opposite

directions due to the difference of the input sequence in the two Gilbert cells. Therefore the final output signal ‘delta’ generated from the difference between ‘out1’ and ‘out2’ increases in amplitude with increasing extra capacitor size, as shown in Figure 34 in which extra capacitors were swept as 1fF, 2.5pF, and 5pF for the 100MHz input signal frequency.

4.3.5 Effect of self oscillation

Another important conclusion drawn from equation (4.15) is that the two input signals to the PD must have the same frequency to derive the phase-offset dependant output signal ‘delta’. If the input frequencies are different, ‘delta’ will be a sinusoidal signal at the beat frequency of two input signals. Depending on whether the beat frequency is lower than the PD load filter corner frequency and/or the PLL loop filter bandwidth, the PD output may be averaged to zero or show substantial time variation. Either way, no valid phase offset information can be obtained.

Similarly, if each input signal to the PD has more than one frequency component, beat frequencies will be observed and the PD transfer function will be modified. One potential scenario that makes this happen is when the ILO enters its self-oscillation mode, e.g. when the main injected tone is beyond the ILO’s locking range. In that case two strong tones with similar frequencies, one from self oscillation and the other from injection, will generate a beat tone that passes through the PD output. This effectively disrupts the PLL since the desired phase offset information is no longer available.

4.3.6 Effect of two distant tones

Another scenario involving two tone inputs is when there are more than one strong interference signals present. Although the topic itself is beyond the scope of this research, it is interesting to observe the PD response in this case and provide some

insights on what might be done in future work to address this issue. Assuming two distant strong interference tones at the LNA input, it can be shown below that unless one of the two tones sees significant attenuation from the ILO block, it is difficult for the PD block to generate useful phase delay information at its output to drive the charge pump.

To analyze the PD response when each input has two tones, we first model the two input signals as

$$\begin{aligned} V_1 &= A_1 \sin(\omega_1 t + \varphi_1) + A_2 \sin(\omega_2 t + \varphi_2) \\ V_2 &= A_3 \sin(\omega_1 t + \varphi_3) + A_4 \sin(\omega_2 t + \varphi_4) \end{aligned} \tag{4.18}$$

V_1 represents the input signal while V_2 represents the output signal of the ILO. Note that no attenuation is assumed from the ILO for either of the two input interference tones. Additional tones may also exist in V_2 due to beat products within the ILO. However, because of the low pass filtering at the PD output structure, these extra tones will not produce low frequency or DC terms after multiplying with V_1 and therefore have been ignored in this analysis.

As shown in (4.18), each input to the PD consists of two frequency tones, namely ω_1 and ω_2, with different phases for each tone. Multiplying V_1 by V_2, and ignoring all sum frequency terms, the PD output can be written as

$$\begin{aligned} V_1 V_2 = {} & \frac{A_1 A_3}{2} \cos(\varphi_1 - \varphi_3) + \frac{A_2 A_4}{2} cos(\varphi_2 - \varphi_4) \\ & + \frac{A_1 A_4}{2} \cos[(\omega_1 - \omega_2)t + (\varphi_1 - \varphi_4)] \\ & + \frac{A_2 A_3}{2} \cos[(\omega_1 - \omega_2)t + (\varphi_3 - \varphi_2)] \end{aligned} \tag{4.19}$$

There are four terms in (4.19). Even if $\omega_1 - \omega_2$ is assumed far beyond the PD output filter and can be effectively suppressed, equation (4.20) still yields two terms. It is difficult to achieve the same transfer function with zero crossing points around zero phase offset, especially when the two tones have independent phase shifts in the two input paths.

$$V_1 V_2 = \frac{A_1 A_3}{2}\cos(\varphi_1 - \varphi_3) + \frac{A_2 A_4}{2} cos(\varphi_2 - \varphi_4) \tag{4.20}$$

4.3.6.1 Two tone simulation with tones of equal strength

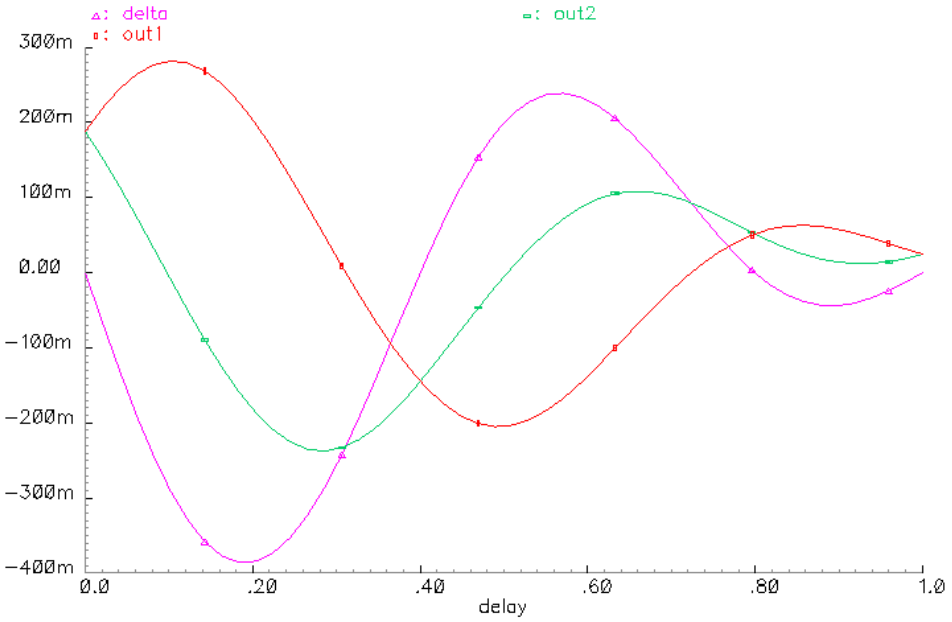


Figure 35: PD response when both input signals have two strong tones and same delay time is swept for both tones in the second input signal.

If both interferers have similar strength at the PD input, they will appear as two tones of equal strength in (4.18). To observe the effect with such inputs, a simulation was performed with A_1, A_2, A_3, A_4 all equal to 100mV and $\omega_1 = 2GHz$, $\omega_2 = 3GHz$. The delay between ω_1 and ω_2 tones are the same for V_1 and V_2, and the time delay between V_1 and V_2 is swept as the input phase offset. The result is plotted in Figure 35 where the 'delta' output is quite different from Figure 32. Most noticeably there is one more zero crossing point when the 2GHz signal offset is swept for one full cycle. This can be explained by noting that a 3GHz tone with the same amplitude is present. Therefore sweeping one cycle delay for 2GHz signal actually covers 1.5 cycle for the 3GHz signal, which causes one more zero crossing point. The final plot is a superposition of the two curves and therefore has more zero crossing locations than the single tone case. Analytically it can also be explained by referring to equation (4.20). A sweep of time delay generates different phase values for φ_3 and φ_4, because they are at different frequencies. Therefore different zero crossing points will be seen as a function of $\varphi_3 - \varphi_4$.

A more careful analysis reveals that the time delay sweep used to generate Figure 35 is not valid in general. It assumes the same time delay between the two input signals V_1 and V_2 for both ω_1 and ω_2 tones. However different tones experience different group delays due to non-linear phase response. In the ILO case, if two tones are far apart and one of them is close to the resonance frequency, the other tone will experience approximately a constant 90^o phase shift, with the polarity depending on the polarity of the frequency offset from the resonant tone. The 90^o phase shift is actually desirable because it makes the second term in (4.20) zero. However, high frequency behavior discussed earlier prevents this from occurring.

Shown in Figure 36 is an improved input phase offset sweep that only applies to one of the two tones in the input, which is the 2GHz tone for this case. The second tone at 3GHz is assumed to be far separated from resonance and thus is expected to experience a 90^o phase shift through the LC tank of the ILO. To observe the high frequency behavior caused by parasitic and extra intentional capacitors, this 90^o phase shift is also varied to be 0^o, 45^o, 90^o, 135^o, and 180^o, respectively. In Figure 36, these phase shift values correspond to normalized periods of 0.8, 0.675, 0.55, 0.425, and 0.3 because the other input arising from the 3GHz tone has a fixed phase shift of 0.8 cycle. Recall that based on the mirror image derivation from equation (4.17), it is expected that only the 0^o and 180^o cases (corresponding to 0.8 and 0.3 cycle cases in Figure 36) provide the desired 'delta' waveform similar to the single tone case in Figure 32 – 34, which is explained in more details below.

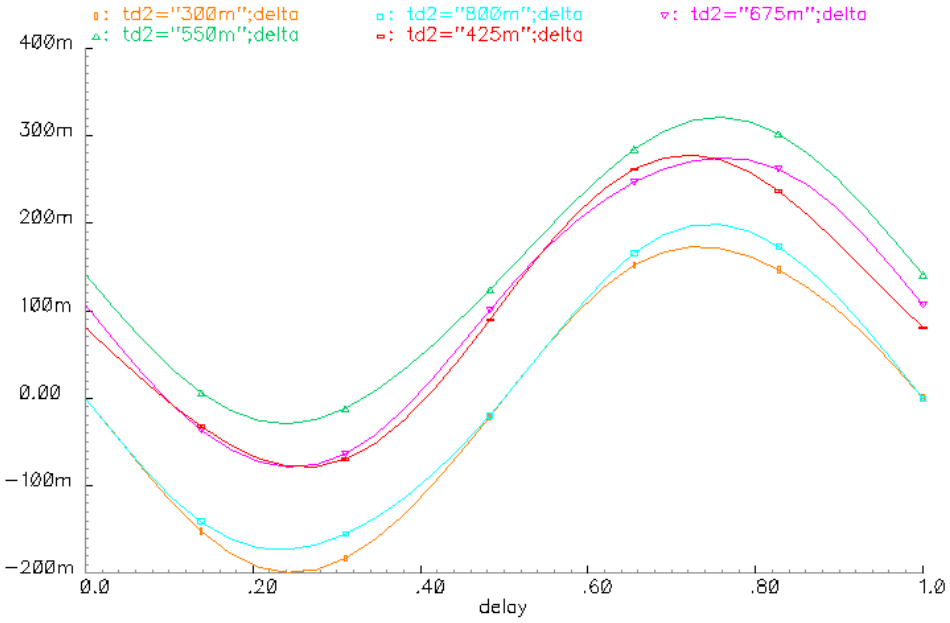


Figure 36: PD response when both input signals have two strong tones and delay time is swept for one tone in the second input signal.

The second term in (4.20) gives a PD output contribution from the second tone at 3GHz in this case. Due to the extra phase shift $\Delta\varphi$ caused by parasitic and intentional extra capacitance, this term should be rewritten as

$$\frac{A_2 A_4}{2} cos(\varphi_2 - \varphi_4 \pm \Delta\varphi) \tag{4.21}$$

The sign $\pm$ in (4.21) is for the dual cell output 'out1' and 'out2' respectively. From the shape of the cosine curve, only when $\varphi_2 - \varphi_4$ is 0^o and 180^o, can the term expressed in (4.21) be fully cancelled between 'out1' and 'out2' in order to achieve a desired behavior for 'delta' approximating the case for the single-tone input .

The ILO provides 90^o phase shift for the distant tone. Thus the above effect is not desirable in order for the implementation to be useful for the two tone case. However, since the ILO also significantly attenuates the distant tone's magnitude, a more realistic case is when one of the two input signals to the PD has one strong tone from the ILO output signal while the other input may still have two strong tones corresponding to the ILO input.

4.3.6.2 Two tone simulation with a single strong tone

Consider the case where two parallel auxiliary paths are employed to suppress two interference tones with similar strength but located far apart from each other. Each path has its own corresponding ILO tuned to the frequency of the specific interferer. As a result of this tuning, at the output of each ILO, two interference signals should have different magnitudes since they experience different gains after passing each ILO block, although they have similar signal strength at the input of each ILO.

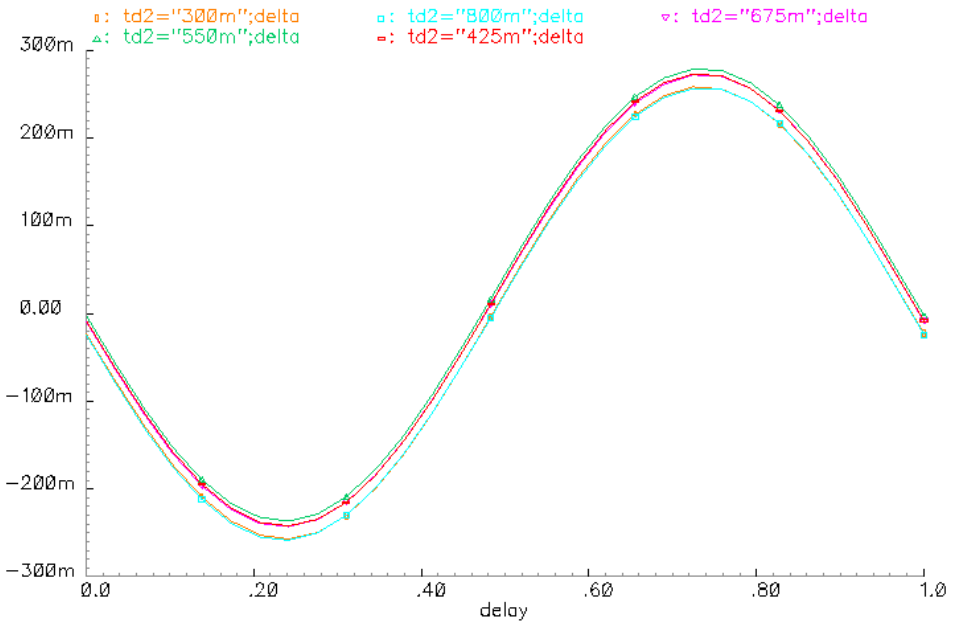


Figure 37: PD response when only one input signal has two strong tones and delay time is swept for one tone in the second input signal.

A similar simulation like the one of Figure 36 was performed for the case where one of the two input signals to the PD has one strong tone while the other input signal has both. The delay for the weak tone, which is assumed to have 10% of the magnitude of all other strong tones, was varied to be 0^{o}, 45^{o}, 90^{o}, 135^{o}, and 180^{o} (corresponding to 0.8, 0.675, 0.55, 0.425, and 0.3 cycle offset annotated in Figure 37), similar to the previous simulation that provided Figure 36. The new simulation result is shown in Figure 37. As can be seen from the plot, all 'delta' output curves stay closer to the single tone case where the zero crossing point happens at zero input phase offset, regardless of the value of the delay time of the weak tone.

This result is good for potentially using the proposed interference cancellation approach with parallel auxiliary paths for multiple interferers that are distant from each other. Since ILO's in each path would be tuned to different frequencies to address

different interferers, the output of each ILO ideally will only have one strong tone, corresponding to the frequency of the specific interferer under attack with that specific path. Therefore with the PD behavior shown in Figure 37, each path should be able to independently operate its own PLL. The small offset voltages of 'delta' at the zero input phase offset point shown in Figure 37 can be either ignored as the compromise between the number of interferers and the accuracy of cancellation, or investigated further for improvement. This area requires further examination.

4.4 HIGH PRECISION CHARGE PUMP

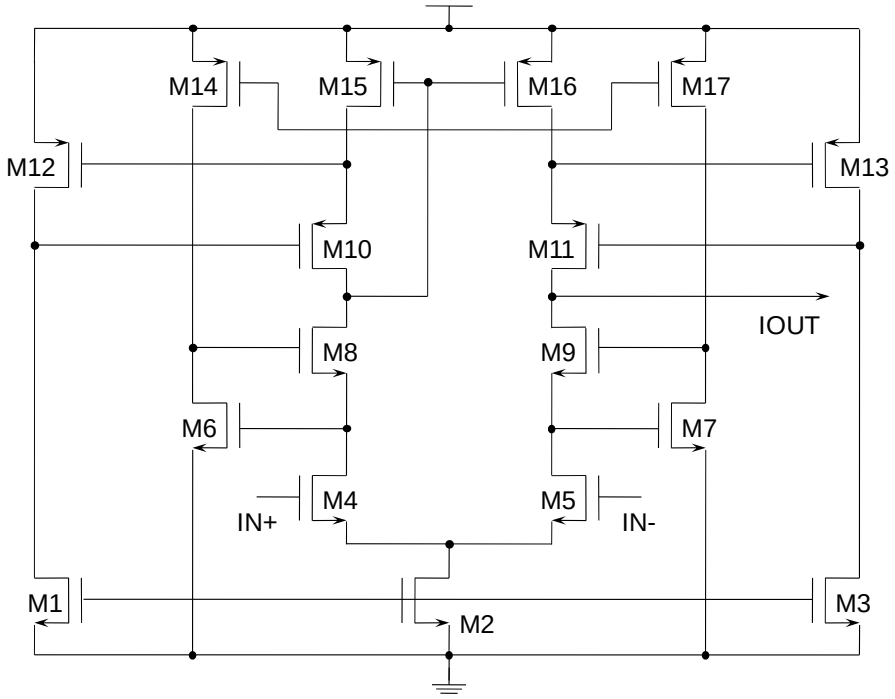


Figure 38: Schematic of the high precision charge pump circuit.

The charge pump has to provide very high accuracy to minimize phase offset between the main signal path and the auxiliary path. A boosted cascode current mirror structure is used for this design as shown in Figure 38.

4.4.1 CP topology

Compared to a regular cascode current mirrors, the boosted cascode mirror offers an output impedance that is amplified approximately by the gain of a common source MOS stage, i.e. of the order of $g_m r_{ds}$, where r_{ds} is the output resistance of the MOS device. To understand this amplification we assume that all MOS devices in Figure 38 have the same value of g_m and r_{ds}. Without the extra feedback for impedance boosting, it is well known that the output impedance of a regular cascode current mirror is of the order of $g_m \cdot r_{ds}^2$. With the local feedback loop formed by M11, M13, and M16, when the drain voltage of M11 increases by v_x, the source voltage of M11 is given by $v_x/(g_{m11} \cdot r_{ds11})$ in the open loop mode, and therefore the drain of M13 decreases by $v_x \cdot (g_{m13} \cdot r_{ds13})/(g_{m11} \cdot r_{ds11})$ that is equivalent to a lower drain voltage of M11 equal to

$$v_x \cdot (g_{m13} \cdot r_{ds13} - 1) \cdot (g_{m11} \cdot r_{ds11})/(g_{m11} \cdot r_{ds11}) \qquad (4.22)$$

for the same change in current.

If all MOS devices are assumed to have the same g_m and r_{ds} respectively, from (4.22), the loop gain for the negative local feedback loop is approximately $g_{m13} r_{ds13}$. Since the negative loop gain provides a negative voltage to offset the original small signal change of v_x, the resulting small signal current change will be smaller compared to the open-loop case. Therefore the output impedance for the boosted cascode mirror to the first order is larger by a factor of the loop gain, namely, $g_{m13} \cdot r_{ds13}$ compared with a

regular cascode whose output impedance is on the order of $g_m \cdot r_{ds}^2$. Thus the output impedance of the boosted cascode mirror is of the order of $g_m^2 \cdot r_{ds}^3$.

The output current *Iout* in Figure 38 drives the charge pump to create a tuning voltage for the varactor tuning port of the ILO. As shown in the ILO schematic in Figure 12, the anode of the varactor is DC shorted to the positive power supply around 1.8V. Therefore for the charge pump circuit that operates at power supply of 3.3V, it is necessary to level shift the output node by about 1V in order to avoid forward-biasing the varactor diode. A PMOS source follower was used for this purpose in the design.

4.4.2 DC simulation

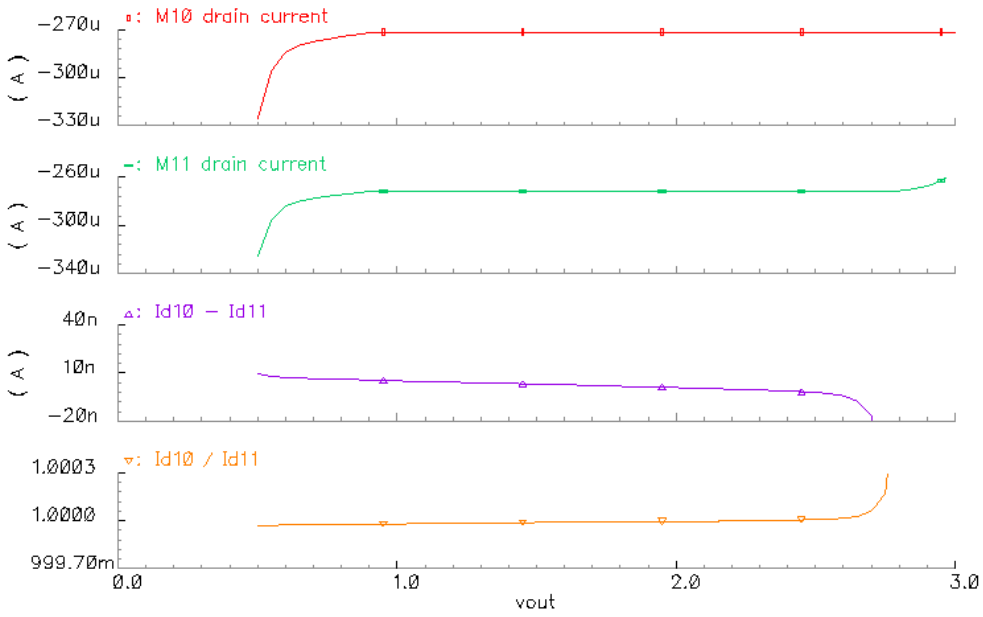


Figure 39: DC sweep simulation for the charge pump circuit.

In Figure 39, charge pump output voltage was swept to monitor the output current variation. As shown in the plot, for an output between 0.5V and 2.6V, the drain current of M11 shows negligible change, confirming that the boosted cascode current mirror provides a large output impedance.

In Figure 40, DC transfer function of the charge pump was obtained by sweeping the input voltage and monitoring the output current. As shown, the curve is relatively linear and more importantly, for zero input voltage, output current is almost zero, indicating a negligible offset current.

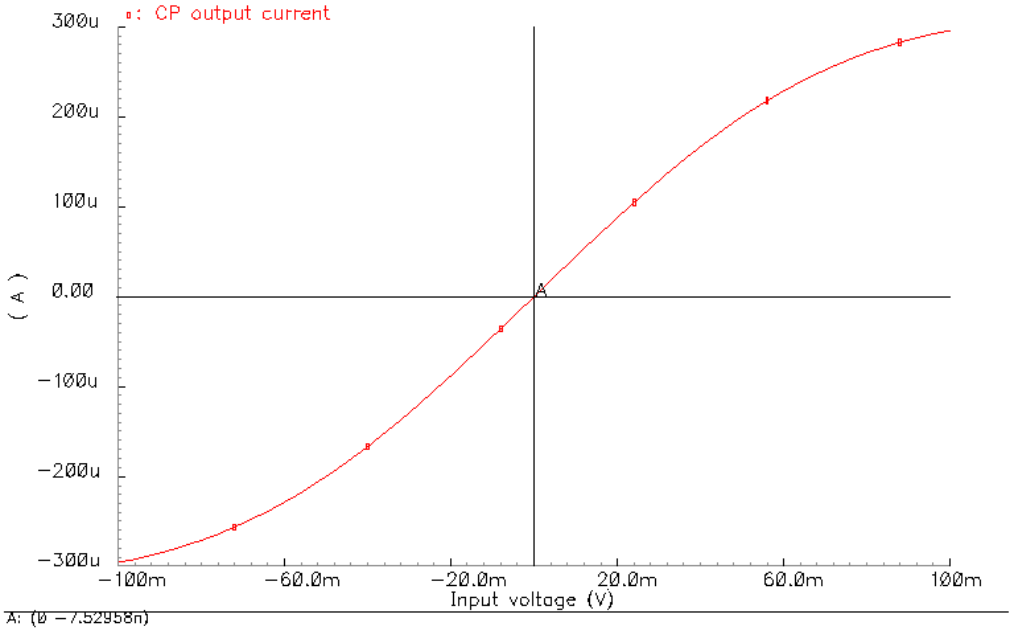


Figure 40: DC transfer function simulation for the charge pump circuit.

4.5 PLL STABILITY WITH AN EMBEDDED ILO

A second order loop filter was used in the PLL, which helps achieve the necessary phase alignment for interferer cancellation when combining the auxiliary path and the main path. In contrast to a traditional PLL loop, the ILO based loop design is unique due

to its different transfer function from the input tuning voltage to the output phase change. The oscillator gain K_{vco} is different for the VCO in a traditional PLL in this design, which uses an ILO. For a VCO based PLL, K_{vco} is given by $d\omega/dV_{ctrl}$. The VCO operates as a phase integrator, owing to the relation between frequency and phase, and this introduces an extra term of 1/s in the transfer function. For this system, on the other hand, assuming an injection-locked state, the oscillation frequency is invariant to the first order. A phase change, however, arises from the different tank center frequency that results in a different set of vector current relationships governed by equation (4.7). Because the phase change in this case involves both the PLL and ILO actions, an analytical representation for the loop behavior is challenging to obtain.

An exact stability analysis that models the effects of the interaction between the ILO and the PLL was not performed. However, to estimate the stability of the PLL, a simulation-based approach was adopted by starting with regular VCO based PLL loop design and adjusting loop filter component values for improving stability, which was checked with transient step response. Detailed stability analysis will be addressed in future work.

4.6 SIMULATION PLOT FOR OPERATING PROCEDURE OF THE LOOP

As discussed above, it is critical that the ILO does not self-oscillate, since that would effectively open the phase locked loop as no valid phase offset information can be retrieved from the phase detector output. The operating procedure of the loop has been described in Chapter 3 and will not be repeated in this section. Instead, simulation plot is presented to provide a better understanding.

As shown in Figure 41, the ILO bias current was stepped up gradually. At lower bias levels, the ILO operates as a tuned buffer instead of an oscillator, only providing

attenuation instead of gain, in order to ensure the phase alignment provided by the PLL between the output and input of the ILO without causing any self oscillation. With the incrementally increasing bias current of the ILO, the output of the ILO mainly consists of the interference signal. As a result of cancellation between the auxiliary path and the main path, the final output of the LNA decreases with the stepped current. The optimal cancellation is seen at 5.6us as shown in Figure 41 where the output signal of the ILO reaches its minimum amplitude, because the strong interferer signal is largely attenuated due to amplitude matching between the main and the auxiliary paths at that setting.

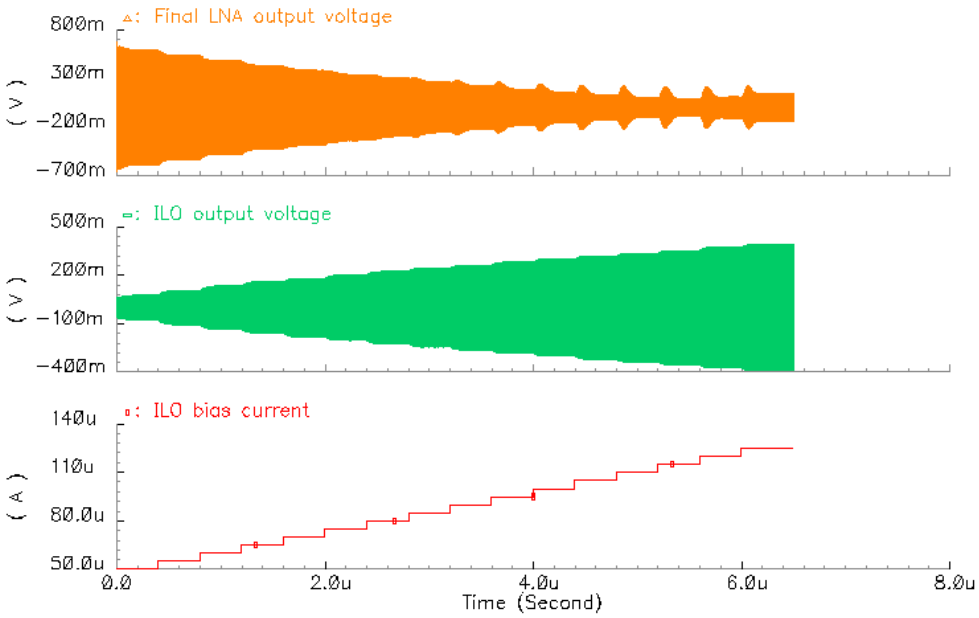


Figure 41: Full system transient simulation with ILO bias current ramping up incrementally.

To evaluate the level of the interferer cancellation at 5.6us, a Discrete Fourier Transform (DFT) was performed for both the output and input signals of the ILO for the period between 5.4us and 5.6us. The input signal spectrum, as shown in Figure 42, is composed of a strong interferer of -25.2dBV at 2.1GHz, which is about 20dB stronger than the desired signal of -45.1dBV around 1.6GHz. The desired signal shows a gain of around 20dB and is amplified to -24.0dBV at 1.6GHz, while the interference signal at 2.1GHz is heavily suppressed to about 32.4dBV, -8.4dB below the desired signal.

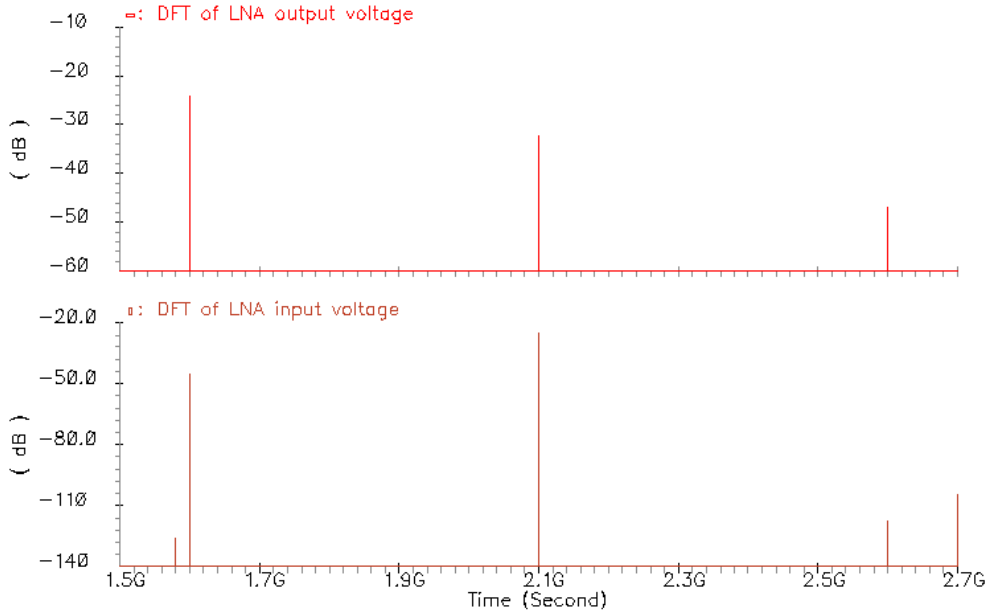


Figure 42: Discrete Fourier Transform (DFT) on LNA input and output signals between 5.2us and 5.6us.

A similar simulation was performed with a much closer offset of 20MHz between the interference and desired signals. As shown in Figure 43, for the same input setup where the interference signal at 2.1GHz was 20dB stronger than the desired signal at 1.8GHz, the output desired signal was observed to be 3dB stronger than the interference,

thus providing about 23dB of rejection. The limit for such a small offset frequency will be set by the noise floor degradation, as will be discussed later.

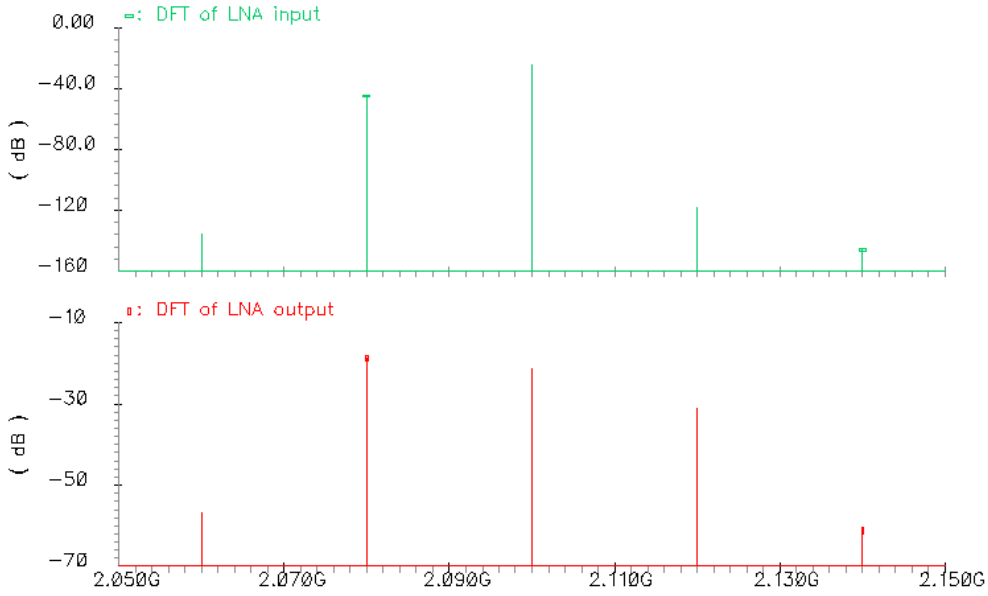


Figure 43: Discrete Fourier Transform (DFT) on LNA input and output signals for 20MHz offset case.

4.7 AM INTERFERER SUPPRESSION

It is clear that for the proposed interference cancellation scheme, extra phase calibration is unnecessary while gain calibration is needed to align the main and auxiliary paths. In order not to disturb the automatic phase alignment of the input and output interference signals of the ILO, the optimal circuit location to realize the gain control is the ILO bias block, as was used for simulation shown in Figure 41 and Figure 42.

Based on the gain control, the design can be used to suppress amplitude modulation (AM) interference signal as well by making the ILO bias current a function of the AM envelope signal. This requires additional envelope conditioning because the

output level of the ILO is not a linear function of its bias current level. Theoretically, the inverse of the functional dependence of the output amplitude of the ILO on its bias current can be utilized for pre-distorting the gain control. A simple AM interference attenuation setup was demonstrated with a two point data fitting to implement an AM envelope based ILO bias current approximation that achieved relatively good cancellation result, as will be shown in the next chapter.

Another advantage of using ILO bias as the gain control mechanism is that it avoids self oscillation of the ILO when the interference signal has a large amplitude variation. For example, for double side band suppressed carrier (DSBSC) signals, the envelope signal periodically crosses zero. This will cause self oscillation of the ILO due to the lack of injection amplitude when the envelope goes to zero. However, since the ILO bias is dependent on the envelope signal it can be transformed into a non-oscillating tuned buffer when needed through proper design. In such a case it should be possible to avoid self oscillation.

4.8 ILO NOISE SIMULATION

Noise floor degradation is the dominant factor that determines the minimum frequency offset between the interference signal and the desired signal for this design to work satisfactorily. In addition to the traditional sources of noise in the LNA circuits, the auxiliary path adds its own noise. At the frequencies of interest, which is normally tens or hundreds of MHz from the interference signal, the ILO noise will dominate because the PLL noise transfer function operates as a high-pass filter for the oscillator and a low pass filter for the blocks preceding the loop filter, with the corner frequency set by the loop filter. For this design, the loop filter bandwidth is of the order of a MHz, therefore most extra noise degradation to the desired signal arises from the ILO phase noise.

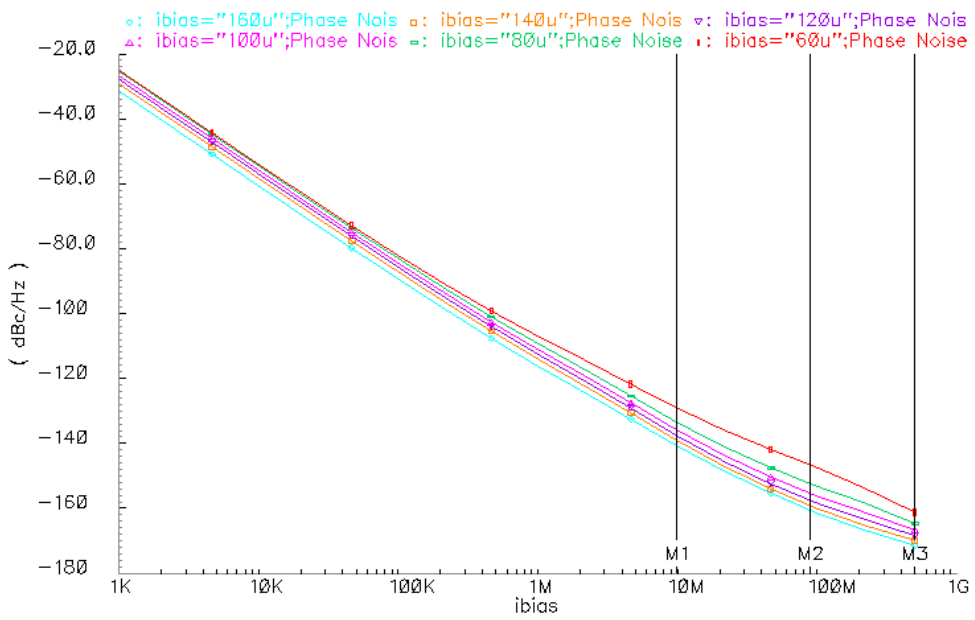


Figure 44: PNOISE simulation for ILO using ideal series L-R with bias level swept.

A periodic phase noise (PNOISE) simulation was performed with ILO bias current swept from 60uA to 140uA with PSS analysis to observe the noise contribution of ILO at different offset frequencies with varying bias levels.

This result is shown in Figure 44. Vertical cursors at 10MHz, 90MHz, and 500MHz are used to obtain intercept phase noise values at those frequencies and the data are shown in Table 2. Assuming a 3dB main LNA path NF that effectively implies a -171dBm/Hz noise power at the input of the LNA, in order not to degrade the net NF with the auxiliary path to above 4dB, the input referred noise density of the ILO should be kept below -177dBm/Hz at the input of the LNA. An interference level of -12dBm thus imposes a phase noise requirement of -165dBc, at the specific offset frequency determined by the difference between the interference and the desired signal frequencies.

As shown in Table 2, at 500MHz offset the ILO approximately provides the noise performance of this order.

For lower offset frequencies such as 10MHz and 90MHz, the noise performance is worse, resulting in higher than desired degradation of noise floor in the desired signal band. To reduce this degradation, improved oscillator performance is needed.

Offset Frequency	Phase noise (dBc) for different ILO bias levels					
	160uA	140uA	120uA	100uA	80uA	60uA
10MHz	-140.8	-139.2	-137.7	-136.0	-133.6	-129.1
90MHz	-160.4	-159.0	-157.3	-155.1	-152.1	-146.4
500MHz	-171.4	-169.8	-168.4	-166.7	-164.6	-161.2

Table 2: Phase noise data at 10MHz, 90MHz, and 500MHz offset from free running center frequency of ILO.

While this parameter was not optimized here, it is noted that excellent oscillator phase noise had been previously reported [27-29]. In all three quoted references, phase noise at 20MHz offset was reported around -165dBc/Hz in order to meet the GSM requirement, pointing to potential room of noise floor improvement even for close in frequency offsets.

Chapter 5: Measurement Results

The architecture was designed and implemented in UMC's 0.18µm RFCMOS process. The design has a die area of 2mm^2 and the auxiliary path draws about 10mA current from a 1.8V supply and 2~3mA from a 3.3V supply. The system was designed around 1.5GHz, due to the choice of process, and is used to provide a proof of concept. The same principle can be applied at higher frequencies, using a faster technology, such as 0.13µm CMOS.

5.1 SUPPRESSION PERFORMANCE FOR SINGLE TONE INTERFERENCE

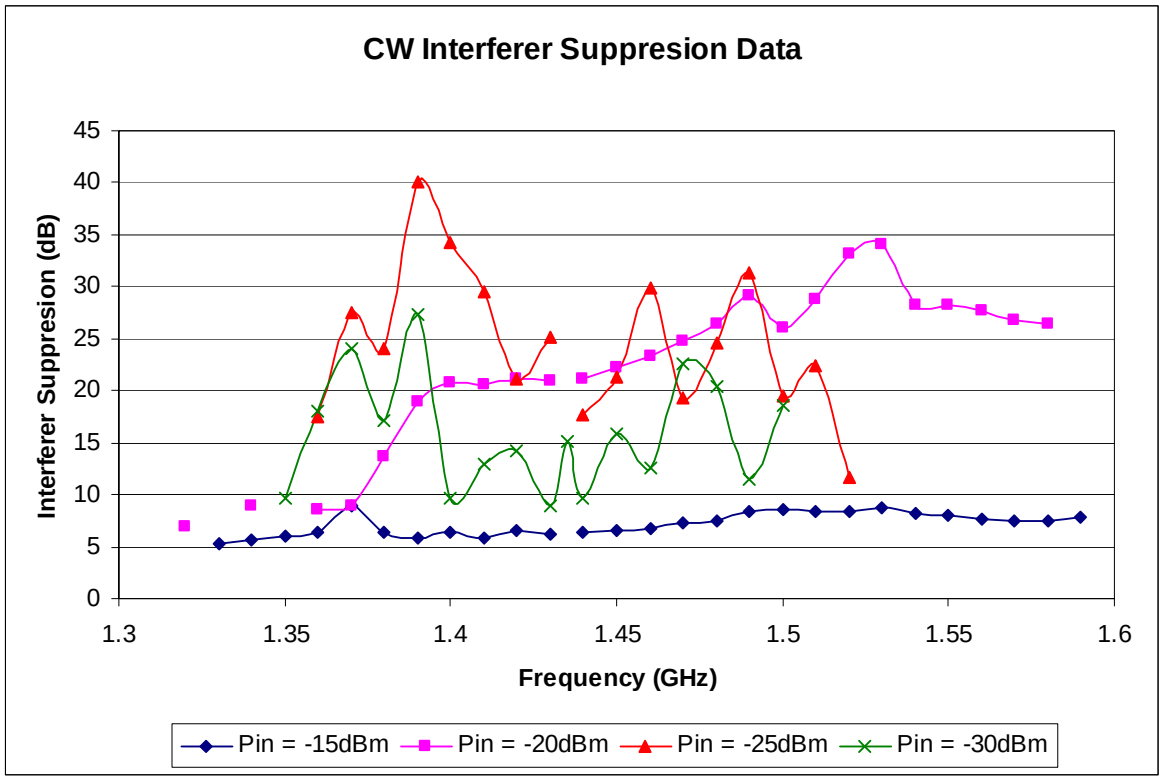


Figure 45: Interferer suppression measurement data.

Input power level of the interferer was swept for four different levels and the suppression achieved was recorded with the best digital tuning setting for ILO of each frequency point within the range between 1.35GHz and 1.56GHz. The result is plotted in Figure 45.

For input power level between -20dBm and -25dBm, most frequency points achieved better than 20dB of interferer suppression. For -30dBm level, most data points lie between 10dB and 20dB. For -15dBm level, suppression ranges between 5 and 10dB. At this power level, LNA1 entered compression, which degraded the achievable cancellation.

Freq (GHz)	Pin (dBm)	Pout1 (dBm)	Pout2 (dBm)
1.45	-30	-19	-17.55
1.44	-30	-19.3	-18.53
1.43	-30	-19.6	-19
1.42	-30	-19.9	-19.4
1.41	-30	-19.7	-19.53
1.4	-30	-19.4	-19.8
1.3	-30	-17.8	-17.6
1.2	-30	-17.8	-17.4

Table 3: Desired signal behavior with interferer cancellation loop on.

Measurement was performed on a separate board to observe the impact of the cancellation on the desired signal while the frequency offset between the desired signal and the interferer was varied. This is reported in table 3. In this measurement, the desired signal was set at -30dBm. An interferer was applied at 1.47GHz with a power level of -20dBm. Without the cancellation loop, the interferer power at the output is -8.4dBm which is reduced to -40dBm when the cancellation loop is applied. As shown in Table 3,

the desired signal actually shows a slightly higher gain when the loop is enabled (Pout2) than disabled (Pout1). This is due to the gain compression effect caused by the strong interferer level when the loop is not enabled. The gain slope between 1.2GHz and 1.4GHz for the desired signal is caused by the bandwidth limitation of the power combiner for measurement input.

Compression performance with and without cancellation was determined in another measurement using an interferer at an offset of 120MHz from the signal. The 1dB compression point (P1dB) with cancellation was observed at an output of -7.9dBm. Without the cancellation active, the interferer at the output increased to -2.1dBm at the same frequency where P1dB was measured, causing a gain compression of 2dB.

To estimate P1dB improvement directly, a second LNA was connected in cascade with the system shown in Figure 10, to emulate the input stage of a mixer. Cascaded P1dB was improved by over 16dB with cancellation on. Gain compression above 13dB was also observed when auxiliary path was disabled, at the same input level as the P1dB with cancellation applied

5.2 MODULATED INTERFERER

The above measurements were performed with single tone interferers. For modulated interferers, we employed a standard GSM pattern supplied with Agilent N5182A vector signal generator as the interferer and observed similar suppression effect of over 20dB, as shown in Figure 46. In a similar setup, an FM interferer with 100kHz modulation bandwidth also achieved similar level of suppression.

The integrated design did not address amplitude modulated interferers such as QAM, since we did not implement the amplitude control loop on-chip. However if the modulation bandwidth is lower than the PLL loop bandwidth, such interferers can also be

rejected once the interferer amplitude envelope information is available, e.g. through an AGC loop using a power detector to detect the interferer amplitude, along with bias adjustment for the ILO.

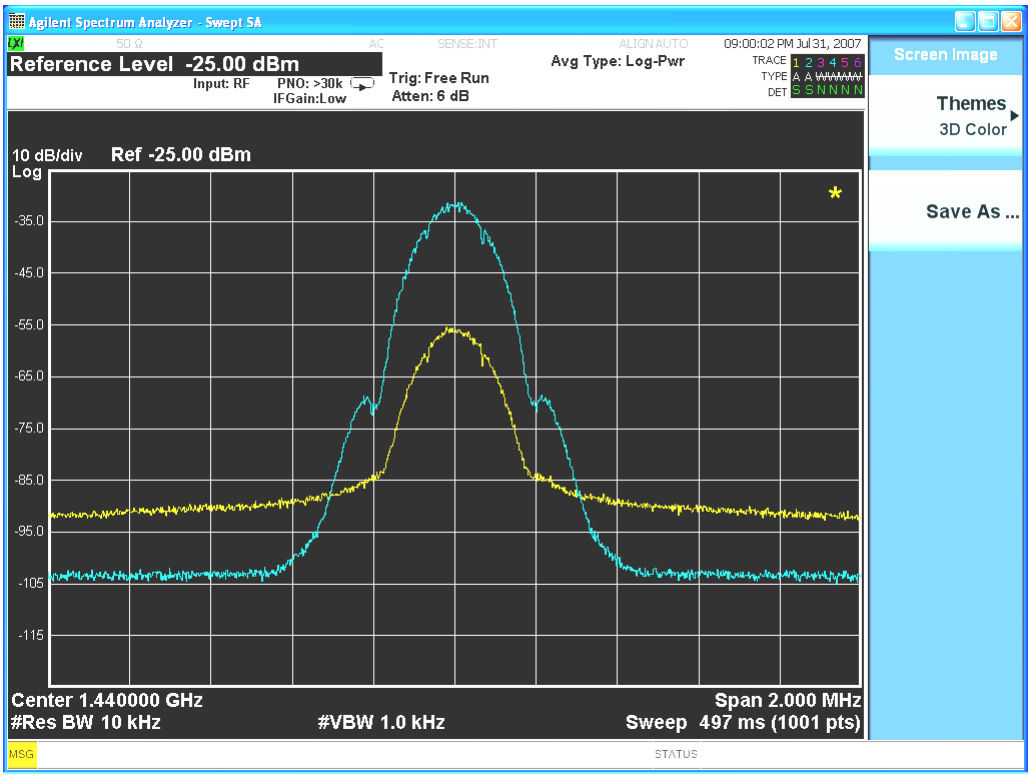


Figure 46: GSM interferer suppression plot shows better than 20dB cancellation without degrading desired signal (not shown).

To demonstrate the approach for rejecting AM interference, a test-setup was implemented with off-chip components for the ILO bias control. The envelope signal of the AM tone was directly retrieved from the signal generator and fed to the ILO bias port with proper linear scaling and DC level shifting. This simple signal conditioning procedure was observed to be effective. As shown in Figure 47, the main carrier and both

sideband tones of the interferer were attenuated. Overall more than 20dB of rejection of an AM modulated interferer was obtained, measured separately with channel power integration over a span of 100MHz range.

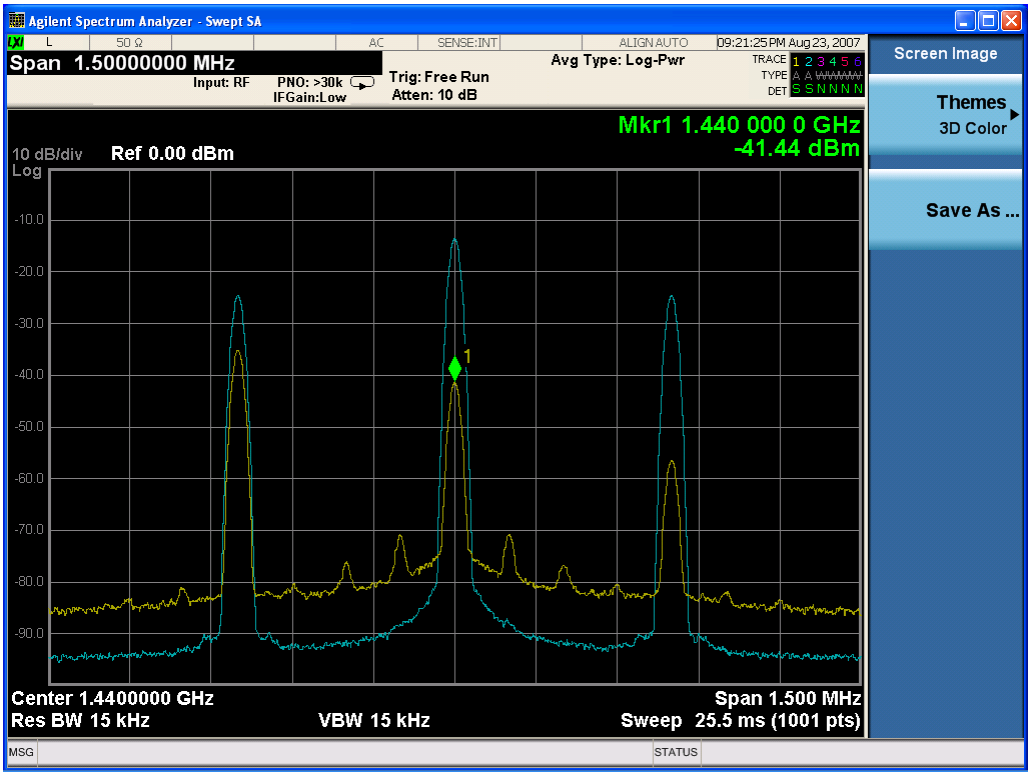


Figure 47: AM interferer suppression plot shows better than 20dB cancellation without degrading desired signal (not shown).

5.3 GAIN AND NF

A simple broadband match using an off chip balun with and without a 200 Ω external resistor was employed. Similar gain performance was obtained between the two cases while the NF improved without the resistor as explained earlier in Chapter 4.

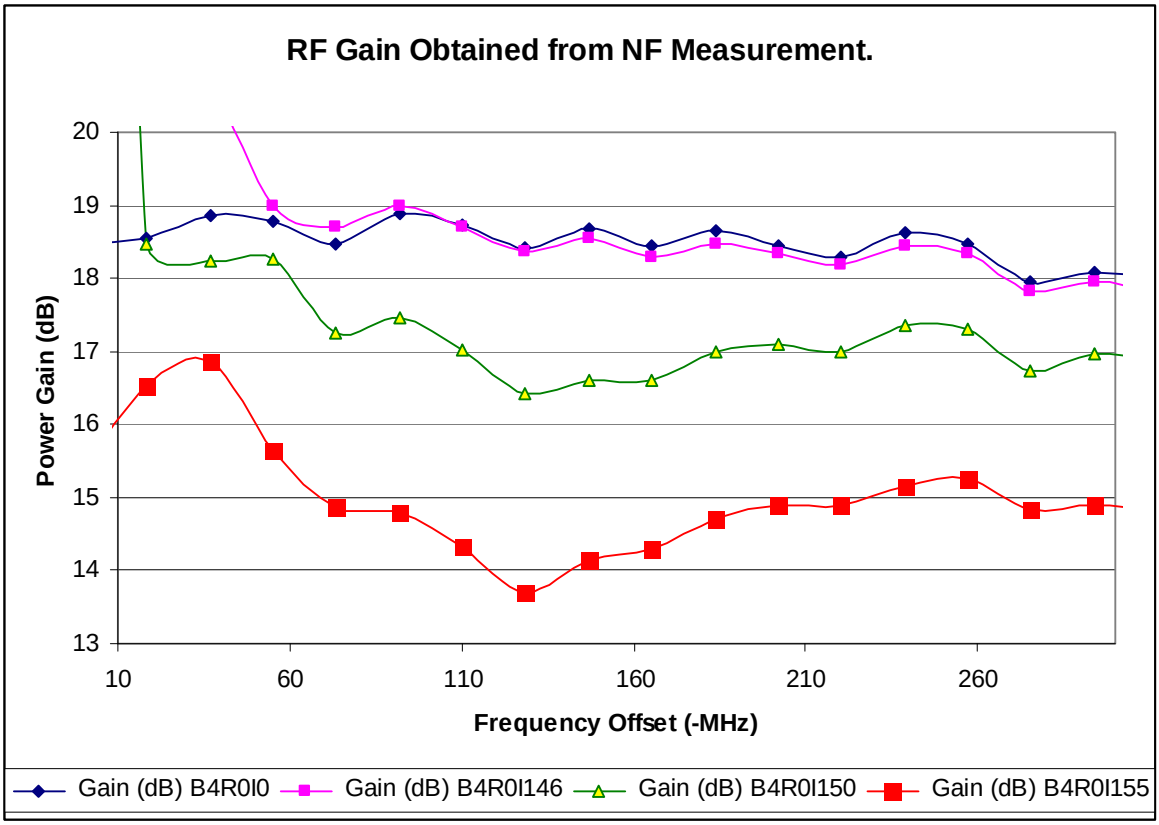


Figure 48: Power gain performance with different oscillation amplitude versus no oscillation (B4R0I0 curve).

The RF small signal gain plot shown in Figure 48 was obtained during the NF measurement. A power gain around 18dB was achieved. As plotted in Figure 48, gain compression is observed when the oscillator turns on with self oscillation at three different bias levels. External interference is not applied, and the free-running oscillator in effect acts like a large amplitude jammer. This is consistent with the change in the output level of the desired signal with the interferer cancellation on or off as discussed

earlier. Detailed statistical measurements were not performed. However, Figure 45 through Figure 48 is representative of measurements across multiple boards.

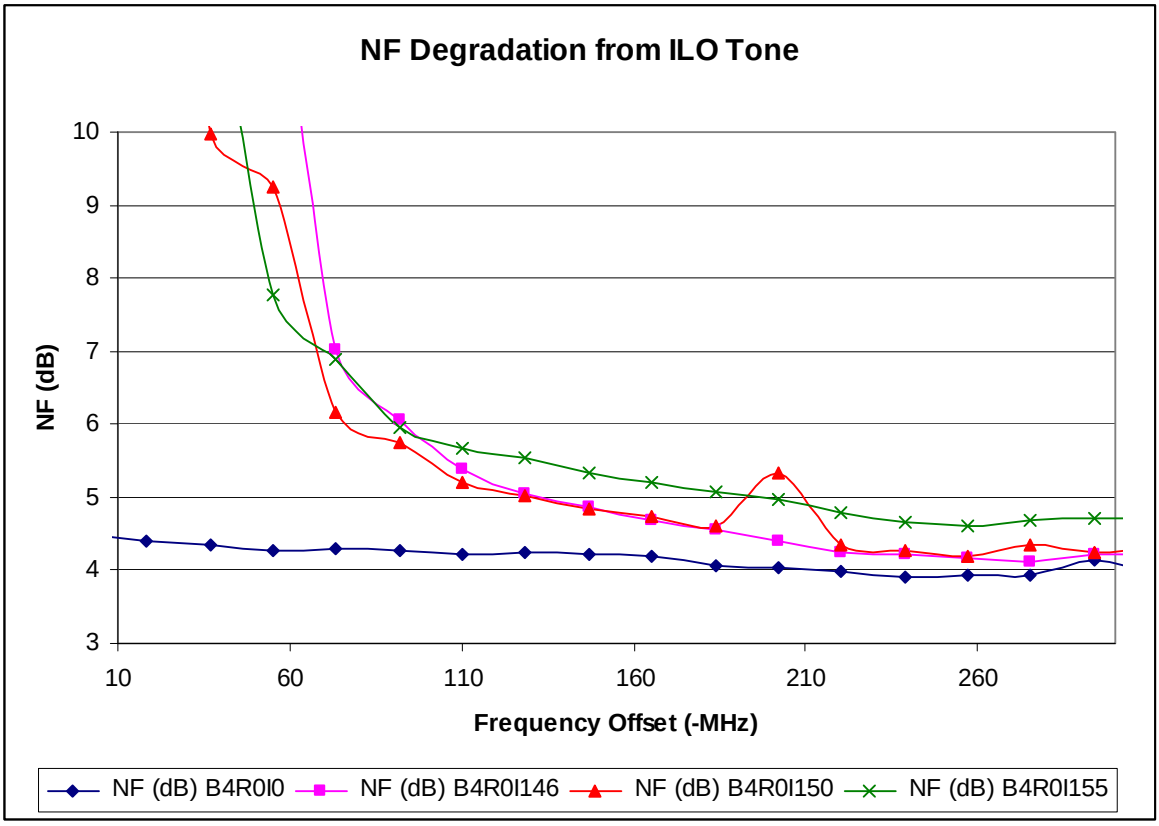


Figure 49: NF performance with different oscillator amplitude versus no oscillation (B4R0I0 curve).

A NF ranging between 3.9 and 4.5 was measured without the auxiliary path using a noise figure meter. This includes an off chip broadband balun that had approximately 1dB insertion loss. The noise figure measurement set up did not allow the application of an external interferer. To model the effect of the phase noise of the ILO, the auxiliary

path was enabled with the oscillator in self-oscillating mode. In this case, as shown in Figure 49, the NF degradation of less than 0.5dB was achieved when the desired signal was sufficiently far from the oscillation tone (>160MHz), which is beyond the frequency where the oscillator phase noise reaches its floor. The center of all curves includes the effect of the strong oscillation tone and does not represent valid noise data points.

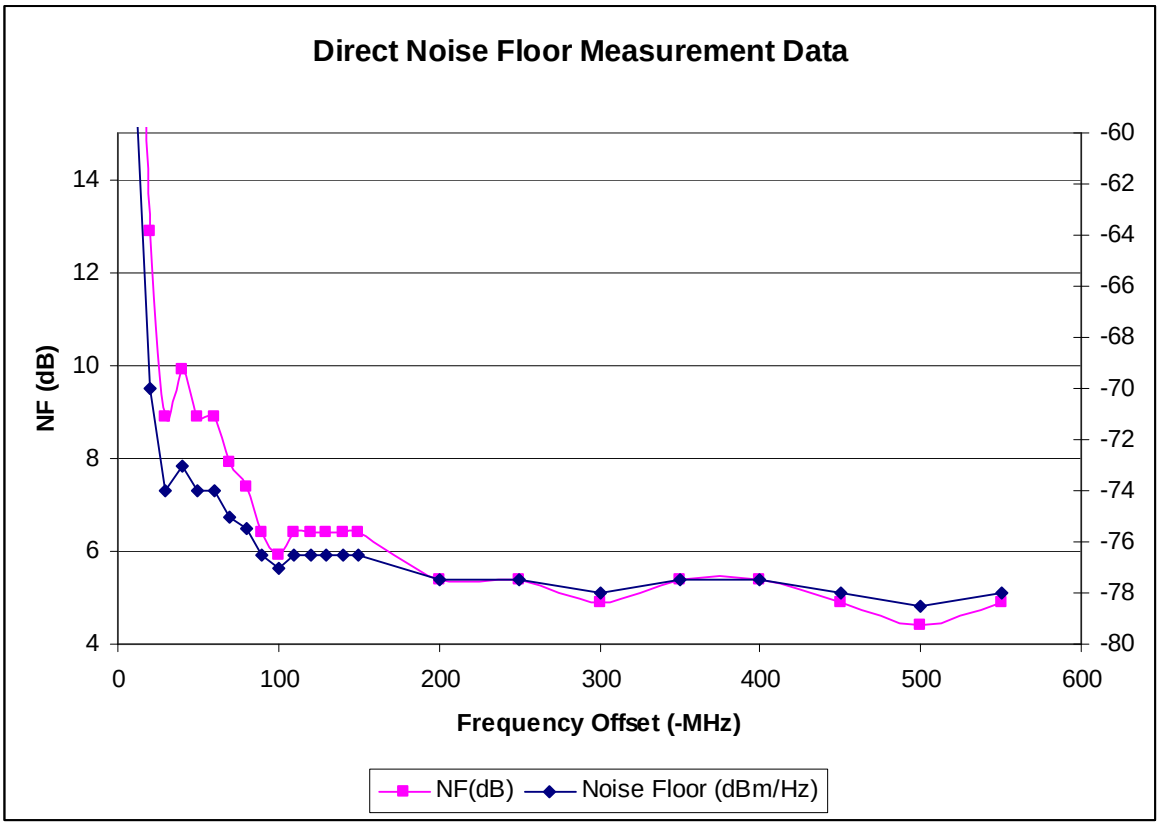


Figure 50: NF performance when the interferer is cancelled with the auxiliary path active. NF is 3.9dB without interferer and ILO.

To measure NF degradation with cancellation of an externally applied interferer in the auxiliary path a different measurement set up was employed. A wideband amplifier

with 35dB gain was used to raise the circuit noise above equipment noise floor, which is about -145 dBm/Hz in this case. Figure 50 shows the NF obtained with this method. In this approach we observed the degradation in the noise floor with and without the cancellation.

Figure 50 shows the NF degradation when the CW interferer is canceled by the loop. The calculated NF from noise floor measurement is approximately 3.9dB in absence of interferer and ILO action. The amount of degradation and the trend remained similar to noise meter measurement data shown in Figure 49 with a free-running oscillation and thus the two plots validate each other. The acceptable level of noise degradation is set by system requirement, and is often of the order of 3dB. This margin determines how close the interferer frequency can be brought towards the desired signal frequency, in order for this technique to be useful.

The die photo of the implementation is shown in Figure 51. As can be seen in the photo, spiral inductors have been used for LNA1, LNA2, and ILO. While high Q inductor is necessary for good ILO performance, LNA stages can potentially use lower quality factor inductors to save die area.

A quad flat no-leads (QFN) package (wire bonding shown in Figure 51) has been used that is adequate for the frequency of operation in this design. For future designs at higher frequency, more advanced packaging technologies such as ball grid array (BGA) or chip scale packaging (CSP) can be adopted to reduce high frequency parasitic effects. Another alternative approach is to use direct chip mounting techniques such as die on board (DOB).

It should also be noted that die area can further decrease with a more advanced process technology for higher frequency design.

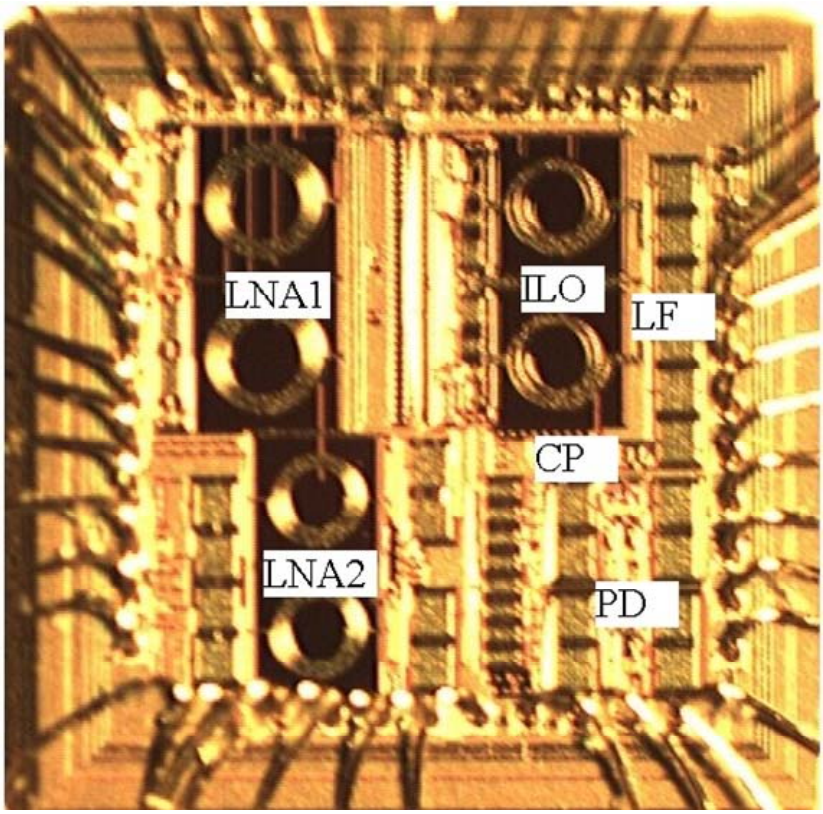


Figure 51: Die photo of the implementation.

Chapter 6: Summary

We have demonstrated a feed-forward interferer cancellation scheme in the context of wide band receivers for the scenario where the out of band interferer is much stronger than the desired signal. The approach can potentially find application in systems such as UWB or emerging cognitive radio systems. The interferer is attenuated within the LNA stage. This is significant as this relaxes the linearity requirement of the down-conversion mixer, which is typically the bottleneck for front end linearity. Fabricated in 0.18μm CMOS process, over 20dB attenuation of FM/PM and CW type interferers was obtained with minimal impact on the strength of the desired signal and in-band noise. AM type interferer rejection was also demonstrated with off chip envelope signal processing and feedback. The scheme can be expanded to cover wider bands using a faster process, as shown in the Appendix. Finally, although mainly designed for off-channel interferer rejection, on-channel interferer rejection is possible in the context of UWB system where the interferer lies inside the bandwidth of interest. In such a case, there may be loss of information within certain sub-channels due to increase in the noise level close to the original location of the narrow-band interferer. However as long as the integrated noise level stays below the margin allowed by the system in the presence of the interferer, this may be an acceptable trade-off, given that the receiver may otherwise get compressed or saturated, with catastrophic performance degradation.

Several potential extensions of this research are possible, some of which are listed below.

1. Design of an integrated ILO bias control to realize both the automatic gain control and the capability to handle AM interferers.

2. Implementation of full UWB multiband coverage using a more advanced process technology.

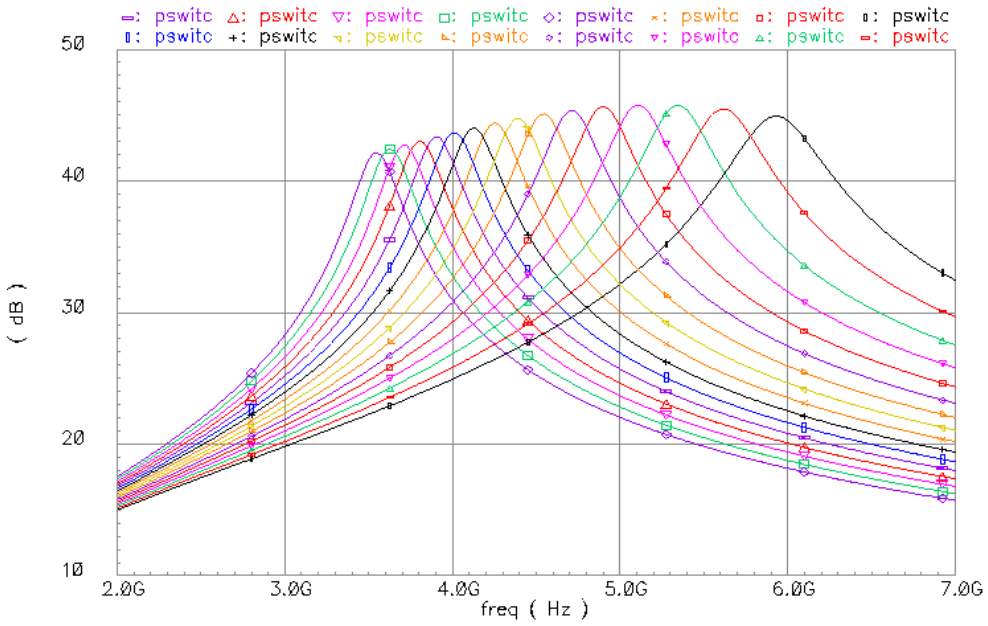
3. Realizing multiple band interference rejection using parallel auxiliary paths with further exploration.

Appendix

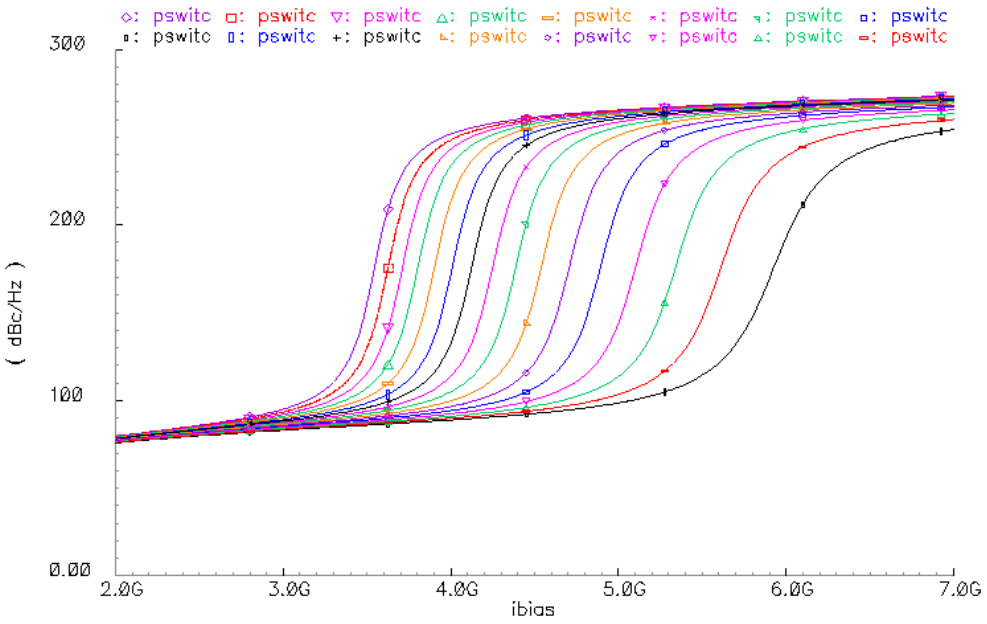
The proposed design was implemented at a lower frequency band around 1.5GHz with about 200MHz tuning range with the available process in 0.18µm. To demonstrate scope for improvement, simulation results with a more advanced RFCMOS process with 0.13µm minimum channel length are shown in this section.

A.1 ILO DIGITAL TUNING RANGE IN A FASTER PROCESS

As shown in Figure 52(a), the 16 digital capacitor programming settings provide over 2.5GHz (between 3.5GHz and 6.0GHz) frequency range using the 0.13µm RFCMOS process, compared with the 200MHz range with 0.18µm process shown in Figure 28(a). The phase response is also shown in Figure 52(b) to confirm the digital tuning range as well as the net negative impedance.



(a)



(b)

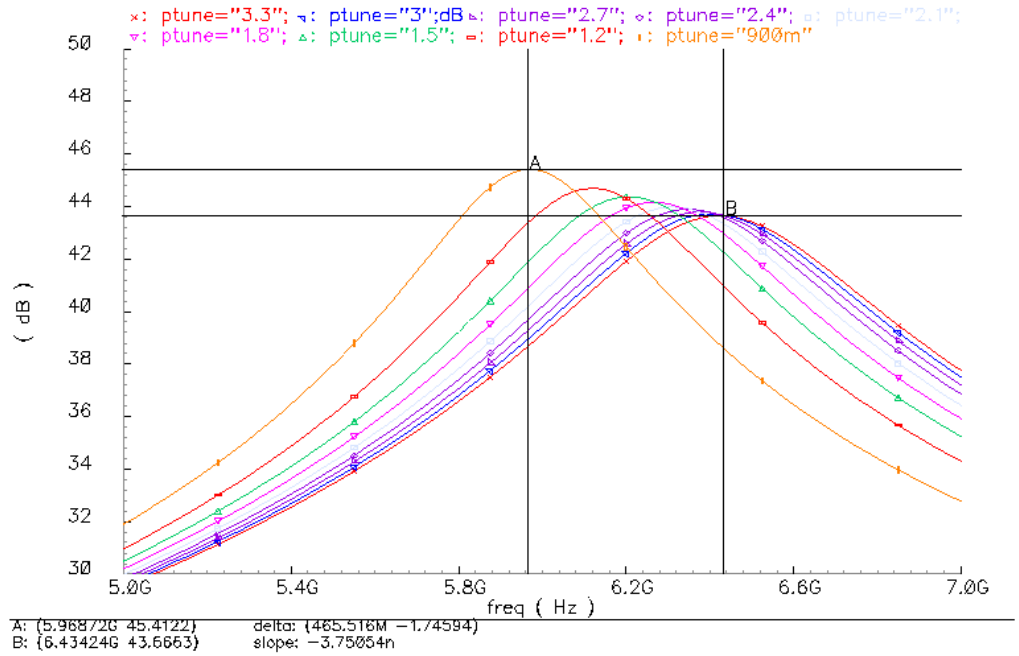
Figure 52: ILO digital capacitor tuning range simulation AC response with 0.13µm RFCMOS process. (a) Magnitude response. (b) Phase response.

As shown in Figure 52(b), the polarity of all impedance values is negative, that is 180^{o} in the plot. The strength of the negative impedance is regulated to be at similar levels, as shown in both Figure 52(a) and Figure 52(b).

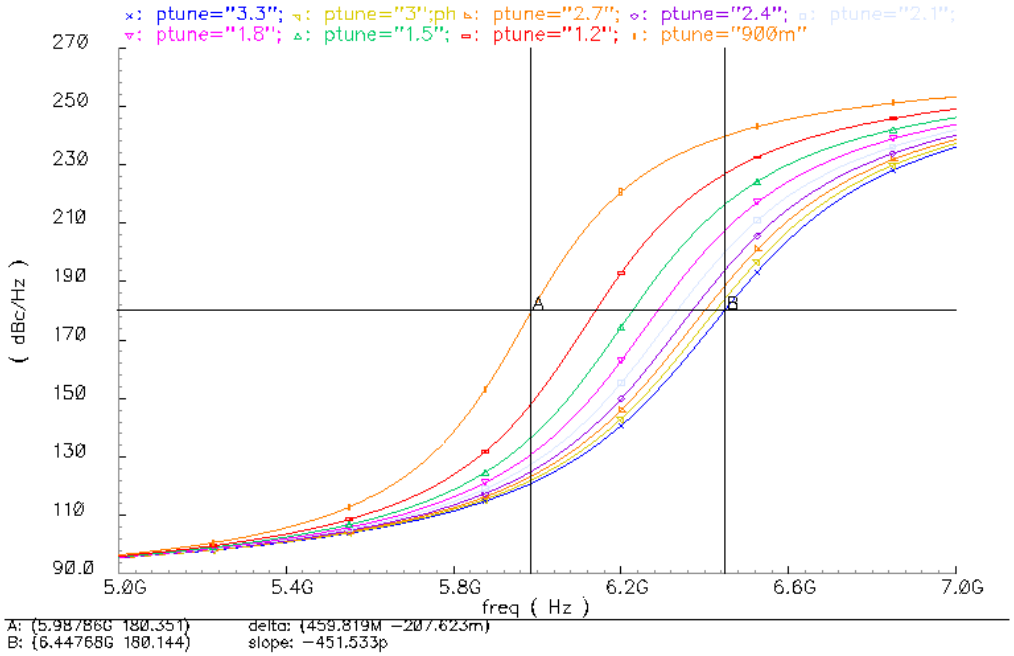
A.2 ILO ANALOG VARACTOR TUNING RANGE IN A FASTER PROCESS

To ensure that analog tuning range is wide enough to cover the frequency gaps due to coarse digital setting, varactor control voltage was swept between 0.9V and 3.3V with the highest digital setting for the same AC simulation.

As shown in Figure 53, the analog tuning range is about 450MHz, which is wider than the gap between adjacent digital settings shown in Figure 52. Therefore the coarse-fine tuning combination for the 0.13µm simulation is adequate for spanning the entire frequency range.



(a)



(b)

Figure 53: ILO analog varactor tuning range simulation AC response with 0.13µm RFCMOS process. (a) Magnitude response. (b) Phase response.

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Vita

Xin Wang was born on July 14, 1971 in Beijing, China. He is the first son of Guangji Wang and Zhaohua Hu. He obtained his Bachelor's degree in physics in 1994 from Peking University in Beijing, China and Master's degree in electrical engineering in 1996 from the University of Michigan in Ann Arbor, Michigan. After advancing to his Ph.D. candidacy in electrical engineering in 1997 at the University of Michigan, he started working for the industry on various analog/mixed-signal/RF integrated circuit (IC) designs. In 2005 he transferred to the University of Texas at Austin with Dr. Ranjit Gharpurey to continue his Ph.D. research work on a part time basis. He currently works at Maxlinear, Inc. as an IC design manager.

Permanent address: 27 Dinuba, Irvine, CA 92602

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