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Planar Ge Photodetectors on Si Substrates for Si/Ge-based Optical Receivers

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Dedicated to

my parents

and

my wife, Kwang-Joo,

for their unconditional love

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Planar Ge Photodetectors on Si Substrates for Si/Ge-based Optical Receivers

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Operation of photodetectors at a wavelength of 1.3 μm has extensive application in the rapidly growing field of optical transmission systems. As optical networks spread deeper into the consumer market, it will become important to have low-cost, manufacturable optical components that can be integrated on a chip with other electrical components. Enhanced performance of many of these systems can be achieved by monolithically integrating the discrete optical devices in existing Si integrated circuits (ICs). The use of Ge is advantageous in terms of lower cost of fabrication and compatibility with Si integrated circuit technology. The high electron mobility and high optical absorption coefficient at 1.3 μm make Ge attractive for some telecommunication applications. In addition, Ge is promising for other applications such as

microwave and millimeterwave photonic systems that require high photocurrent and high linearity. To this end, interdigitated Ge PIN photodetectors were fabricated on Si substrate using 10-μm-thick graded SiGe buffer layers. Their operation at 1.3 μm was successfully demonstrated. A 3-dB bandwidth of 3.8 GHz was obtained at low bias of -5 V and the external quantum efficiency at 1.3 μm was 49 % without external bias. The SiGe buffer layers effectively relieved strain and resulted in high quality Ge epitaxial layers with a low threading dislocation density of ~ 10^5 cm^{-2} and smooth surface morphology. A more practical approach was to directly deposit thin epitaxial layers of Ge on Si substrate. The challenge to this approach was to accommodate the lattice mismatch of 4 % without significant degradation in the material quality. Our approach to overcome island formation was to grow the Ge layers at low temperature. Metal-Ge-metal photodetectors were fabricated on a Ge epitaxial layer directly grown on Si (100) substrate. Amorphous Ge was used to increase the Schottky barrier height, which resulted in a reduction of the dark current by more than two orders of magnitude.

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Chapter 1

Introduction

1.1 Motivation

As optical networks spread deeper into the consumer market, it will become important to have low-cost, manufacturable optical components that can be integrated on a chip with other electrical components. Many of these systems have been demonstrated by monolithically integrating the discrete optical devices in existing Si integrated circuits (ICs) [1-1]-[1-13]. Integration of photonic devices into Si integrated circuits (ICs) has the potential to impact low-cost optical communications applications and optical interconnects. The primary advantages of a Si-based approach to optoelectronic devices are low-cost manufacturable optical components and easily mass-produced optoelectronic integrated circuits (OEICs).

1.2 All Si Optical Receivers

Previously, our group at the Microelectronic Research Center at the University of Texas at Austin developed monolithically-integrated all Si optical receivers consisting of a silicon p-i-n photodiode and a MOSFET transimpedance preamplifier circuit [1-14]-[1-24]. This optical receiver operated

at the telecommunication wavelength of 850 nm. However, the long absorption-length, 15 μm-20 μm, of 850 nm light in silicon made it extremely challenging to achieve a high-frequency performance comparable to traditional GaAs monolithic optical receivers. To improve the speed and lower the operating voltage of the photodiode, optical receivers were fabricated using silicon-on-insulator substrate [1-19]-[1-22]. Another method used to accomplish high-speed and low-operating voltage was resonant-cavity-enhanced (RCE) photodiodes [1-14]-[1-16]. The fabrication of RCE photodiodes involved placing a thin absorption region between two mirrors to form a resonant cavity. The incident light made multiple passes through the active region, enhancing the effective absorption length. This technique was also used to fabricate photodiodes using selective epitaxial growth (SEG). [1-17,18]

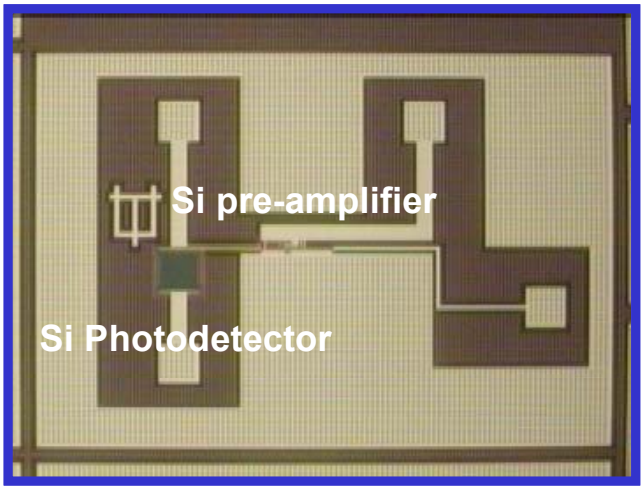


Figure 1.1 Schematic of completed Si-based optical receiver

Recently, in collaboration with Motorola, we built all-Si optical receivers using Motorola's 130 nm CMOS process technology [1-23]-[1-24]. We integrated a Si PIN photodetector with a Si preamplifier on silicon-on-insulator (SOI). The processing was carried out in one of Motorola's 8-inch pilot lines and was totally compatible with their CMOS process. Figure 1.1 shows a schematic diagram of monolithically integrated Si-optical receiver.

1.3 Si and Ge-based Integrated Optical Receivers

Following this project, we began to develop Si/Ge-based optical receivers and integration of a Ge photodetector with a Si preamplifier for use in 1.3 μm telecommunications. Operation of photodetectors at a wavelength of 1.3 μm has extensive application in the rapidly growing field of optical transmission systems. Figure 1.2 shows a schematic cross-section of the integrated Ge/Si-based optical receivers.

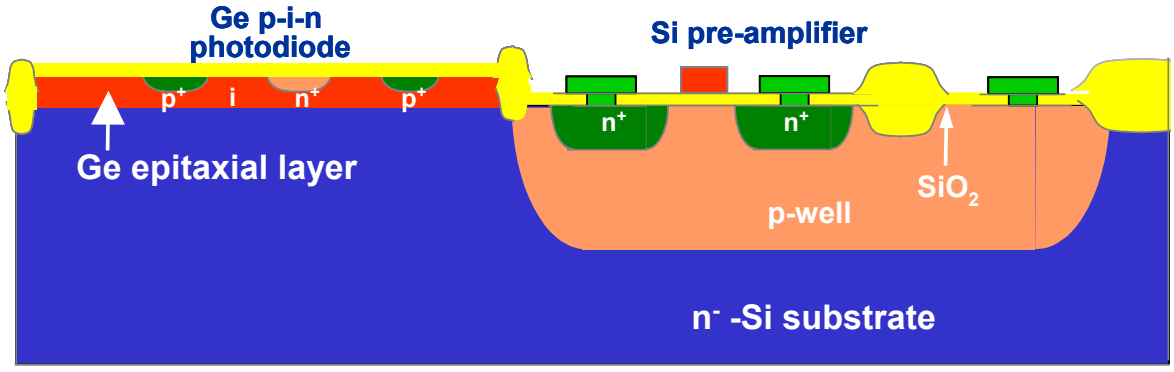


Figure 1.2 Schematic cross-section of integrated Ge/Si-based optical receiver

Germanium was used as a photodetector material. It is advantageous to use Ge photodetectors instead of Si photodetectors when a longer wavelength, a thinner absorbing layer, a higher quantum efficiency and/or a higher speed of the photodetector is needed. Although high-speed photodetectors have been built in a variety of III-V compound semiconductors for long-haul optical transmission, the use of Ge is beneficial in terms of lower cost of fabrication and compatibility with Si complementary metal oxide semiconductor (CMOS) processes using existing silicon manufacturing infrastructure. In addition, Ge is promising for other applications such as microwave and millimeterwave photonic systems that require high photocurrent and high linearity [1-30].

1.4 Advantages of Ge Technology

There are several more reasons that Ge is an attractive material for advanced photonic and electronic devices. Figure 1.3 shows the mobility of Ge, Si, and GaAs at 300 K versus impurity concentration. Germanium has higher carrier mobility than silicon for both electrons (3x) and holes (4x). The hole mobility of germanium is even higher than that of GaAs.

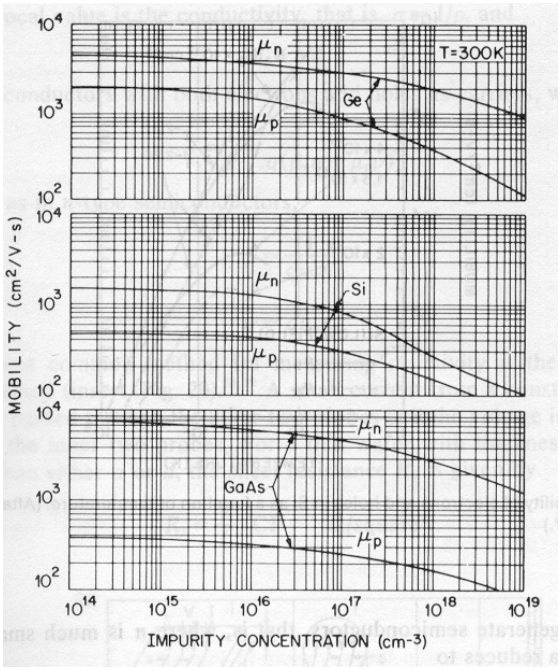


Figure 1.3 Drift mobility of Ge, Si, and GaAs at 300 K versus impurity concentration [1-34]

Figure 1.4 shows the optical absorption coefficient of germanium as a function of wavelength. The high optical absorption coefficient at 1.3 μm and the narrow band gap energy make Ge attractive for these optical communication applications. To this end, Ge PIN photodetectors were fabricated on Si substrate and their operation at 1.3 μm was successfully demonstrated [1-25]-[1-29].

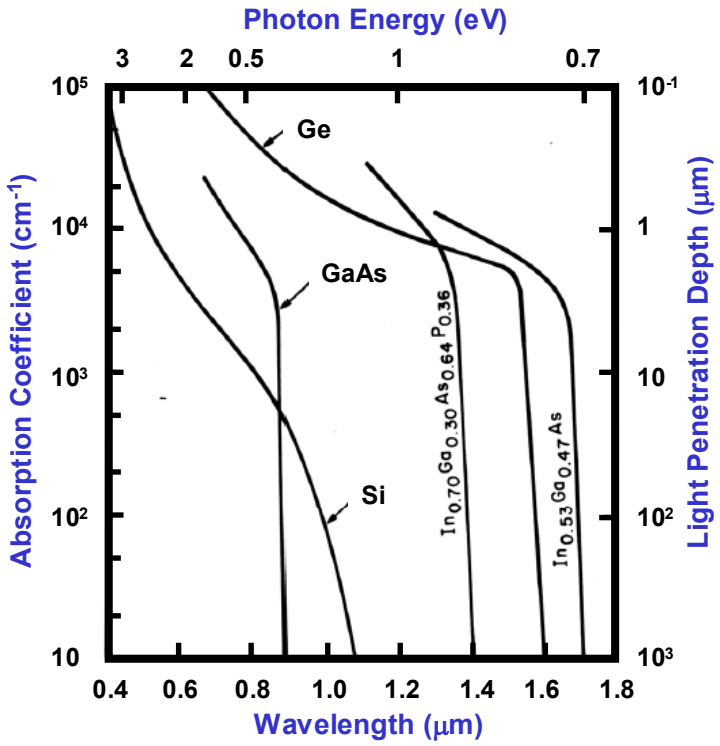


Figure 1.4 Optical absorption coefficient of germanium as a function of wavelength [1-35]

In electronic applications, SiGe technology has already entered high-volume and large-scale manufacturing of heterojunction bipolar transistors (HBTs) and SiGe-HBT-BiCMOS circuits. The dopant thermal activation

energies are much lower than those in silicon, which is advantageous for the formation of shallow junctions. Recently, to overcome the scaling challenges present in scaled silicon devices, alternative concepts such as the combination of high-κ dielectrics with Ge have been investigated [1-31,32].

In optoelectronic applications, Ge and SiGe alloys allow the integration of infrared Ge photodetectors with Si ICs. The addition of Ge to Si increases the absorption coefficient in the infrared spectral range, which allows a reduction in the detector thickness, and, therefore, enables faster detectors than with pure Si. Furthermore the band gap energy decreases with increasing Ge concentration and wavelengths that are longer than 1100 nm can be detected. Figure 1.5 shows the absorption coefficient for Ge fractions of 0, 20, 50, 75, and 100 % in SiGe [1-33].

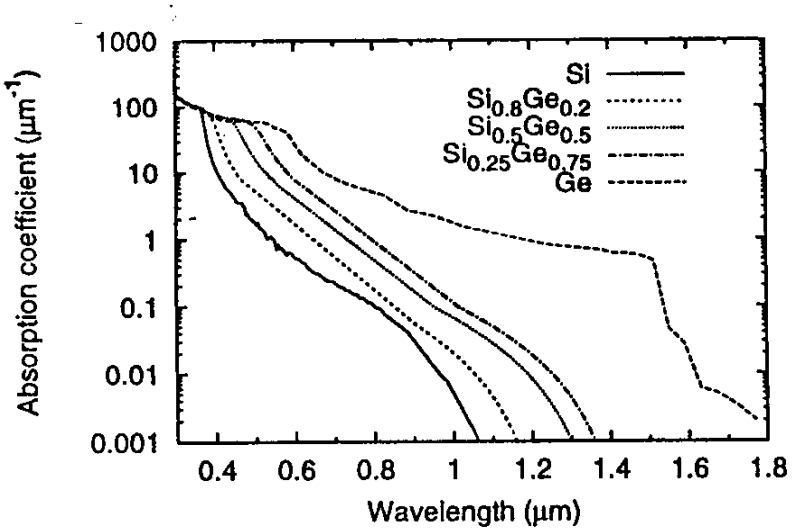


Figure 1.5 Absorption coefficient for SiGe with different compositions [1-33]

1.5 Planar Interdigitated Photodiode Design

The photodiode used in this work was a planar structure consisting of alternating interdigitated p^+- and n^+-fingers separated by intrinsic regions. This planar interdigitated p-i-n structure was designed to achieve high responsivity in addition to high speed. Figure 1.5 shows the schematic of the planar interdigitated p-i-n photodiode structure fabricated on slightly doped Ge substrate so that a large depletion width would be produced with a small-applied bias. This eliminated any diffusion effects arising from carrier generation in the undepleted region. A wide depletion region also yielded high quantum efficiency. The interdigitated p^+- and n^+-fingers were formed by ion implantation, which is a conventional process in CMOS technology.

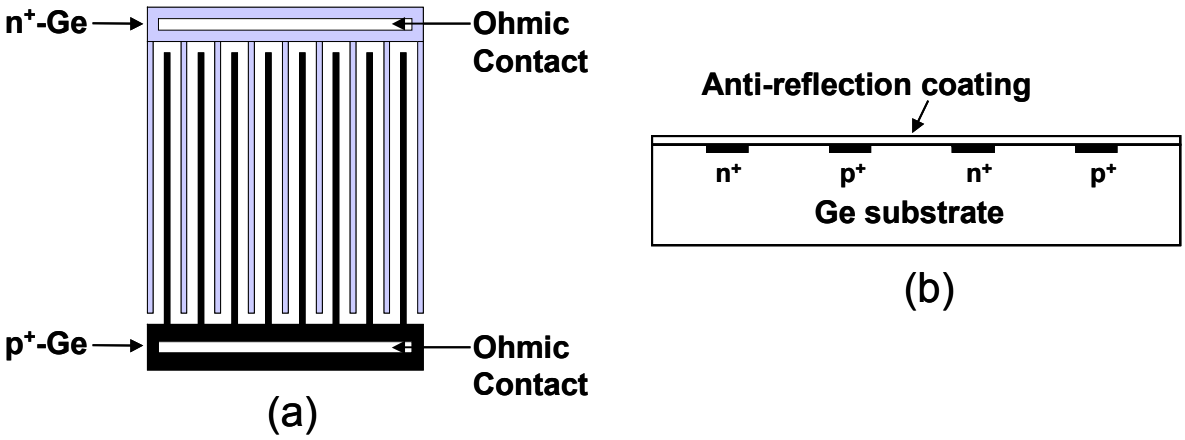


Figure 1.5 The planar interdigitated p-i-n photodiode structure: (a) top view, (b) cross-sectional view

Typical commercial p-i-n photodiodes employ a vertical structure using thermal diffusion or epitaxial growth. The thickness of the intrinsic absorption region is tailored to provide the desired balance between speed and efficiency. However, this type of device is not compatible with planar integration because both device contacts are not available from the top surface. One planar structure, the MSM photodiode, has been widely used owing to its relative ease of fabrication and low capacitance. The MSMs, however, tend to exhibit low quantum efficiency due to contact shadowing and high dark current when compared to PIN photodiodes. In addition, the MSMs require a Schottky metallization process, which is not compatible with Si CMOS process.

1.6 Challenges in the Integration of Ge with Si

Despite the potential advantages afforded by Ge devices, the growth techniques and material quality of Ge on Si have limited the performance and potential for integration with Si ICs. The lattice constant of Ge has a mismatch of 4 % relative to Si. The misfit-related strain of the pseudomorphic Ge film is relaxed by formation of a micro-rough surface up to a thickness of 8 MLs (MonoLayers). A partial relaxation of the Ge towards its bulk lattice constant occurs, which is not possible for a flat and continuous film. For thicker Ge films the misfit is relieved by a periodic dislocation network, which is confined to the Si-Ge interface.

For the integration of Ge photodetectors with acceptable responsivities, the thickness of a Ge epitaxial layer has to greatly exceed the psuedomorphic critical thickness, while maintaining low threading dislocation density. Various techniques have been pursued to achieve a relaxed Ge layer on Si with low defect density. Ge layers, grown by ultrahigh vacuum chemical vapor deposition (UHV-CVD) or molecular beam epitaxy (MBE), have demonstrated significant reduction in the threading dislocation density by incorporating thick graded $Si_{1-x}Ge_x$ buffer layers. Chapter 2 reviews the progress of Ge epitaxy on Si substrates over the past few decades.

Chapter 2

Review of Progress in Si/Ge-based Photodetectors

The growth of Ge and SiGe heteroepitaxial layers on Si substrate has been investigated for more than 20 years. The integration of Ge photodetectors on Si substrates has been an interesting area of research because the lower bandgap of Ge enables SiGe-based photodetectors to be used for 1.3 μm applications. However, the large lattice mismatch between Si and Ge of about 4 % has limited the performance and potential for integration with Si ICs. Thermal mismatch between the Si and Ge expansion coefficients (α_{Si} = 3.55 x 10^{-6} K^{-1} and α_{Ge} = 7.66 x 10^{-6} K^{-1} at 750 ^{o}C) has also led to undesirable tensile stresses during cool-down from the growth temperature that have resulted in micro-cracks or residual tensile strain and dislocations. To exploit the advantages of Ge and SiGe alloys for Si/Ge-based photodetectors, the problems associated with the heteroepitaxy have to be understood. This chapter gives an overview of these issues and describes several examples of Ge and SiGe epitaxy.

2.1 Ge Epitaxy on Si Substrates

The most effective way to overcome the lattice mismatch and to grow high-quality SiGe and Ge layers on Si substrates is to use a compositionally

graded SiGe buffer. Typical graded buffer layers consist of 10 % Ge per 1 μm, which results in a thick 10 μm buffer for Ge content varying from 0 % to 100 %. In the monolithic integration of optical receivers, direct growth of Ge epitaxial layers on Si substrates is more advantageous. The following reports of SiGe and Ge epitaxy on Si substrate describe the various techniques that have been used.

In 1983, Y Ohmachi et al., of NTT Japan, reported Ge epitaxial growth on Si substrate using vacuum evaporation at relatively low temperatures, 350 ^{o}C and 440 ^{o}C [2-3]. The Ge epitaxial layers were p-type with acceptor concentration of 1.6 x 10^{16} cm^{-3}. The mobility was measured to be 1040 cm^{2}/V sec. The acceptor concentration and mobility depended on the layer thickness. The acceptor concentration decreased rapidly and the hole mobility increased at a point larger than 0.7 μm from the interface.

In 1991, B. Cunningham et al. of IBM, reported for the first time the heteroepitaxial growth technique of pure Ge films on Si (100) substrate by an ultrahigh vacuum chemical vapor deposition (UHV-CVD) technique [2-4]. The growth mode was found to be critically dependent on the substrate temperature during deposition. Between 300 ^{o}C and 375 ^{o}C, growth occurred in a two-dimensional, layer-by-layer mode. However, the growth proceeded by island formation above 375 ^{o}C. The authors explained that in the low-temperature regime the growth rate was controlled by a surface decomposition reaction,

whereas in the high-temperature regime the growth rate was controlled by diffusion and adsorption from the gas phase.

E. A. Fitzgerald et al., of AT & T Bell Laboratories, reported totally relaxed compositionally graded Ge_xSi_{1-x} layers grown on Si substrate at 900 ^oC using molecular beam epitaxy (MBE) and rapid thermal chemical vapor deposition (RTCVD) techniques [2-5]. X-ray diffraction revealed that for $0.10 < x < 0.53$, the Ge_xSi_{1-x} layers were totally relaxed. $Si_{1-x}Ge_x$ layers grown on these graded layers showed low density of threading-dislocations, 4×10^5 cm^{-2} and 3×10^6 cm^{-2} for $x = 0.23$ and $x = 0.50$, respectively.

In 1994, A. Sakai et al., of NEC Corporation, reported the effect of adsorbed atomic hydrogen on the evolution of Ge films on Si substrates at 300 ^oC in solid-source MBE [2-6]. The hydrogen flux was supplied separately from the Ge flux. A hot tungsten filament was used to dissociate molecular hydrogen. The authors observed that hydrogen acted as a surfactant, suppressing island formation of Ge on the substrate. This was explained by a kinetic effect of the hydrogen surfactant, which reduced the diffusion length of Ge adatoms during growth.

Extensive studies on surfactant-mediated epitaxy have been done for Ge-on-Si using As, Sb, Te, and Bi [2-7]-[2-12]. The use of these surfactants was very effective in suppressing island formation, which resulted in the layer-by-layer mode throughout the growth. It was reported that introduction of a

monolayer of a surfactant completely changed the growth mode from an island growth to a 2-D layer growth (Frank van der Merwe) with a continuous and smooth Ge film on Si (111) [2-16]. The surfactant was not incorporated but segregated and floated on the growing Ge film. The saturation of the dangling bonds of the semiconductor reduced the surface free energy and drove the strong segregation. This effect on the growth process was the selective change of activation energies, which were important for the diffusion and the mobility of Ge. It was also suggested that hydrogen acted as a surfactant. Hydrogen coverage of the growth front during epitaxy was reported to have a considerable effect on growth kinetics of the films [2-13]-[2-15].

In 1998, M. T. Currie et al., reported high-quality Ge layers on optimized relaxed buffers by introducing an intermediated chemical mechanical polishing (CMP) step at $Si_{0.5}Ge_{0.5}$ in the graded structure [2-17]. The CMP step liberated dislocations and created the necessity to nucleate new dislocations. An optimized relaxation of the graded buffer resulted in such a way, where existing threading dislocations were more effectively used to relieve stress.

In 1999, H. C. Luan and L. C. Kimerling et al., from MIT, reported high-quality Ge epitaxial layers on Si substrates with low threading-dislocation densities using two-step UHV-CVD process followed by cyclic thermal annealing [2-18]. The growth proceeded in two steps. In the first step, 30 nm of Ge was deposited on Si substrate at 350 ^{o}C, then the temperature was raised to

600 ^{o}C and 1 μm of Ge was deposited. Finally, the wafers were cyclic annealed between a high annealing temperature (900 ^{o}C) and a low annealing temperature (780 ^{o}C). The threading dislocation density was measured to be 2.3 x 10^{7} cm^{-2}. Combining selective area growth with cyclic thermal annealing produced an average threading dislocation density as low as 2.3 x 10^{6} cm^{-2}.

In 2000, T. Langdo and E. A. Fitzgerald et al., of MIT, demonstrated selective epitaxial growth of high quality Ge on Si substrate [2-19]. Pure Ge layers were selectively grown on SiO_2/Si substrate using UHV-CVD. "Epitaxial necking," in which threading dislocations were blocked at oxide sidewalls, showed promise for dislocation filtering and for low-defect Ge-on-Si.

In 2001, J. L. Liu et al., from the University of California at Los Angeles, reported high-quality Ge-on-Si using solid-source molecular beam epitaxy [2-20]. They used a Sb surfactant-mediation technique and a SiGe graded buffer. A relaxed Ge film was grown on a 4-μm-thick Sb-mediated graded SiGe buffer. The threading dislocation density was measured to be 5.4 x 10^{5} cm^{-2}.

Recently, G. Luo et al., of National Chiao Tung University, Taiwan, reported the growth of Ge epitaxial layers on Si substrates using two SiGe buffer layers [2-21]. In this method, a 0.8 μm $Si_{0.1}Ge_{0.9}$ layer was first grown, then 0.8 μm $Si_{0.05}Ge_{0.95}$ layer, finally 1.0 μm top Ge layer was subsequently grown. The interfaces between $Si_{0.1}Ge_{0.9}$/ $Si_{0.05}Ge_{0.95}$ and Ge/$Si_{0.05}Ge_{0.95}$ were used to

terminate the upward-propagated dislocations effectively. The threading dislocation density was 3 x 10^6 cm^{-2}. The total thickness of all epitaxial layers was only 2.6 μm.

2.2 Ge Photodetector on Si Substrate

In 1984, S. Luryi et al., from AT & T Bell Laboratories, demonstrated the feasibility of fabricating infrared photodetectors for long-wavelength fiber-optics communications on a silicon chip for the first time [2-22]. Ge-on-Si structure was grown by molecular beam epitaxy (MBE) and consisted of Si substrate, SiGe alloy, n^+-Ge, undoped-Ge, and p^+-Ge. The Ge p-i-n photodiodes showed an external quantum efficiency of 40 %, which was measured in a short-circuit configuration.

In 1996, F. Huang and K. Wang of the University of California at Los Angeles, reported SiGeC photodetectors grown on Si substrates [2-23]. The active absorption layer of the SiGeC/Si p-i-n photodiode consisted of a strained SiGeC alloy with a Ge content of 60 % and a thickness of 80 nm. The device exhibited a peak response at 850 nm with the response extending to 1.3 μm. The external quantum efficiencies were 20 % at 850 nm and less than 1 % at 1.3 μm. This low quantum efficiency at 1.3 μm was due to the low content of Ge in a SiGeC layer and thickness of absorption layer was not thick enough to enable a

reasonable absorption. The leakage current density at the saturation voltage was 70 pA/μm^2.

In 1998, X. Shao and P. Berger et al., of The University of Delaware, reported $Ge_{1-x}C_x$/Si heterostructure photodiodes with nominal carbon percentages (0~0.02 %) [2-24], which exceeds the solubility limit. A 0.6 μm-thick p-GeC epitaxial layer was grown on n-Si substrate using MBE. The p-$Ge_{1-x}C_x$/n-Si photodiodes showed external quantum efficiency of 2.2 %. The leakage current was 10~20 pA/μm^2. A significant reduction in diode reverse leakage current was observed by adding C to Ge, but these effects saturated with more C. Incorporation of C into SiGe makes it possible to reduce the compressive strain between the SiGe and Si substrate.

In 1998, L. Colace et al., of Terza University of Rome, Italy, reported metal-germanium-metal photodetectors fabricated on thick relaxed Ge layers [2-25]. Ge layers (~1 μm) were epitaxially grown directly on silicon substrate using a low-temperature-grown Ge buffer layer (~50 nm). The detector showed a good responsivity at normal incidence at both 1.3 μm and 1.55 μm, with a maximum responsivity of 0.24 A/W at 1.3 μm under a 1 V bias. A response time of about 2 ns was measured. Interdigitated Ag electrodes spaced 10 μm apart were used as Schottky contacts to the Ge films on a 100 x 500 μm region. The dark current exhibited a superlinear dependence on applied bias.

In 2000, L. Colace et al, and H. Luan and L. Kimerling at MIT, demonstrated Ge/Si mesa heterojunction photodetectors with responsivities of 550 mA/W at 1.32 μm and 250 mA/W at 1.55 μm and time responses shorter than 850 ps [2-26]. The devices exhibited well-pronounced rectifying current-voltage characteristics with a saturated reverse current density about 30 mA/cm^2. High quality 1 μm-thick Ge epitaxial layers were grown on Si substrate using a UHV-CVD system followed by cyclic thermal annealing.

In 2002, D. Buca et al, of Forshungszentrum Julich, Germany, reported metal-germanium-metal photodetectors. MSMs were fabricated on 270 nm thick Ge epitaxial layers, which were grown on Si substrate using MBE [2-27]. Interdigitated Cr metal top electrodes were used as Schottky contacts to the Ge films. They showed a response time of 12.5 ps full width at half maximum at both 1300 and 1500 nm wavelength. The overall external quantum efficiency was 13 % at 1320 nm and 7.5 % at 1500 nm.

Chapter 3

Thermal Behavior of Native Ge Oxides

The advantages of Ge technology include high carrier mobility, low thermal activation energies, a high absorption coefficient at the telecommunication wavelength, and potential compatibility with the Si CMOS process. Despite these advantages, Ge technology has not been as widely deployed as Si technology. This is primarily because of a lack of a high-quality Ge insulating oxide that is comparable to SiO_2 in Si technology. While silicon has an extremely high-quality dielectric (SiO_2) that can be used for isolation, passivation, and gate oxide, Ge surfaces are not effectively passivated with Ge oxides.

The oxidation process of several semiconductor surfaces has been extensively studied over the past decade [3-1]-[3-5] but there are relatively few studies of Ge oxidation. Most of these studies have been carried out on the Ge oxides formed by wet chemical or in situ oxygen exposure [3-6]-[3-10]. The thermal characteristics of these oxides were investigated in a UHV system. This chapter describes a study of the annealing behavior of Ge native oxides, which were formed by exposure to air. The annealing behavior of Ge native oxides has been studied with X-ray photoemission spectroscopy (XPS), reflective-high-

energy-electron-diffraction (RHEED) patterns, and secondary ion mass spectroscopy (SIMS).

3.1 XPS Study on the Thermal Desorption of Ge Oxides

The chemical bonding states at the Ge surface were characterized by X-ray photoemission spectroscopy (XPS) as an aid to understanding the thermal characteristics of Ge oxides. The samples used in this experiment were Sb-doped n-type Ge (100) substrates with resistivity in the range 1~5 Ω-cm. Annealing was performed using a rapid thermal processor (RTP) with a N_2 purge at atmospheric pressure for 60 s. This annealing technique is a typical semiconductor process in microelectronics technology.

The XPS measurements were performed using a Physical Electronics (Department of Chemistry, The University of Texas at Austin) PHI 5700 ESCA spectrometer with monochromatic Al K_α (1486.7 eV) x-ray sources and an 11.7 eV path energy. Photoelectron spectra were measured at a take-off angle of 45^o. The vacuum level during the measurements was 10^{-10} Torr at room temperature. For a binding energy reference, Ag $3d_{5/2,}$ Cu $2p_{3/2}$, and Au $4f_{7/2}$ were used. Peak fits were performed as part of the analysis.

Figure 3.1 (a) shows the Ge 3d XPS spectrum of a native oxide before annealing. The $3d_{3/2}$ and $3d_{5/2}$ peaks are signatures of elemental Ge. A peak fit resolved spin-orbital splitting of 0.6 eV with an intensity ratio of 0.7. A binding

energy of 29 eV for the Ge $3d_{5/2}$ peak was used as a reference to correct for charging effects. An additional broad peak, shifted from the Ge $3d_{5/2}$ peak by 3.4 eV toward higher binding energy, was identified as GeO_2, a native oxide.

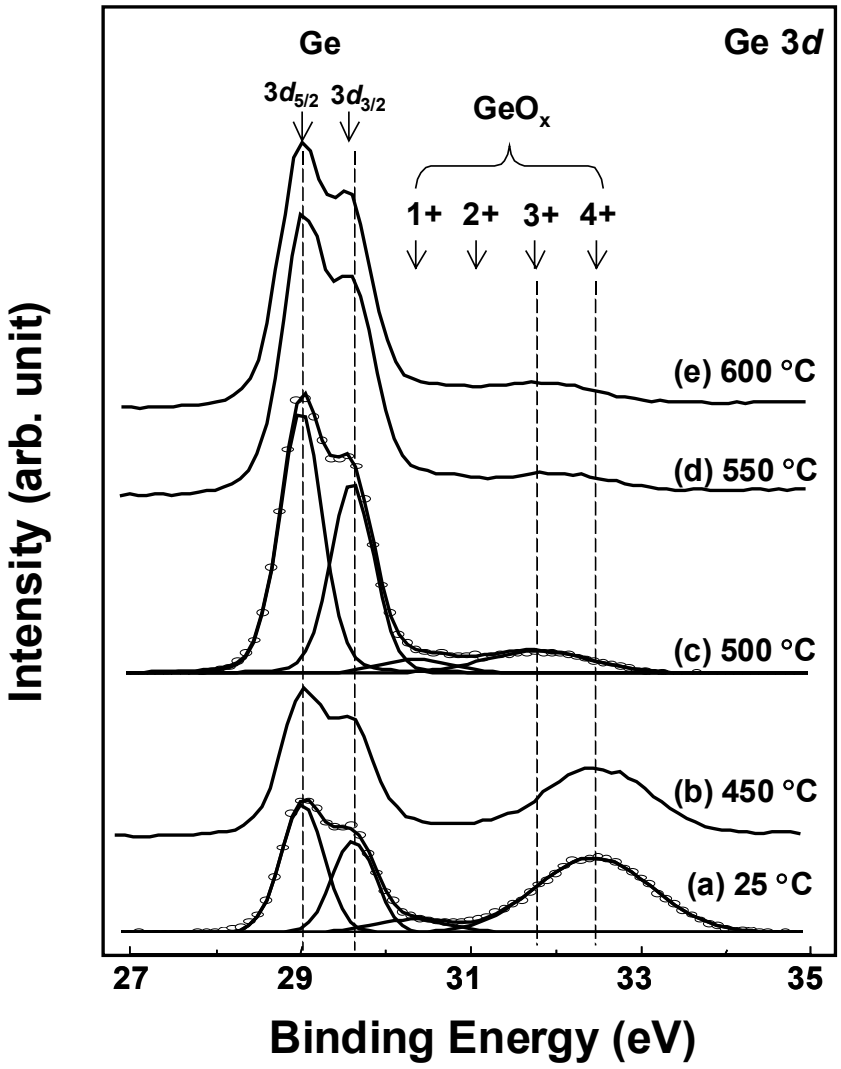


Figure 3.1 XPS Ge 3d core-level spectra from Ge (100) wafers with native oxides for different temperatures. (a) 25 ^{o}C, (b) 450 ^{o}C, (c) 500 ^{o}C, (d) 550 ^{o}C, and (e) 600 ^{o}C

The Ge 2*p* XPS spectrum of the native oxide before annealing (Fig. 3.2 (a)) shows the oxide component more clearly. The higher surface sensitivity of the Ge 2*p* electrons is due to the reduction of the mean free path for electrons of low kinetic energy compared to that of Ge 3*d* electrons [3-14]. An elemental Ge peak with low intensity is centered at 1217.3 eV and a dominant oxide peak occurs at 1220.3 eV. This oxide is mainly attributable to GeO_2. As for the Ge 3*d* spectra, the other oxides states were not clearly resolved.

Figure 3.3 (a) shows an O 1*s* XPS spectrum measured before annealing. A main peak was positioned at 531.5 eV with a small shoulder toward lower binding energy. The peak with a high binding energy was assigned to GeO_2 and the low-energy shoulder to other oxide states. After annealing at 450 ^{o}C, the spectral features showed very little change as shown in Fig. 3.1 (b), 3.2 (b), and 3.3 (b). The Ge 3*d* spectrum after annealing at 500 ^{o}C is shown in Fig 3.1 (c). The intensity of the GeO_2 peak decreased significantly, which resulted in an intensity reduction for the total oxide by a factor of approximately 5. A peak fit showed a slight increase in GeO_x ($x<2$). This intensity change in the oxide states shifted the combined oxide peak toward lower binding energy at 31.8 eV, which corresponds to the binding energy of the Ge^{3+} oxide state. The intensity of the elemental Ge peak increased concurrently. This is more clearly seen in the Ge 2*p* spectrum in Fig. 3.2 (c).

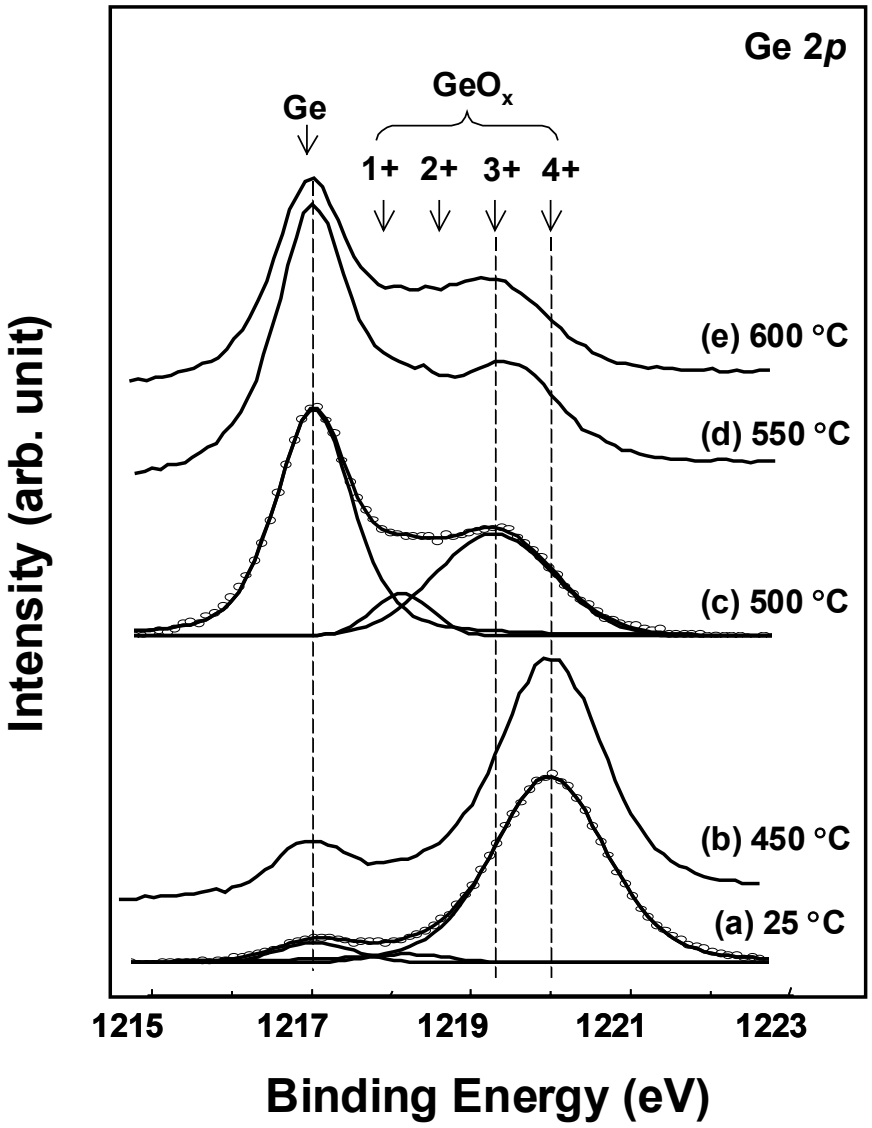


Figure 3.2 XPS Ge 2*p* core-level spectra from Ge (100) wafers with native oxides for different temperatures. (a) 25 ^{o}C, (b) 450 ^{o}C, (c) 500 ^{o}C, (d) 550 ^{o}C, and (e) 600 ^{o}C

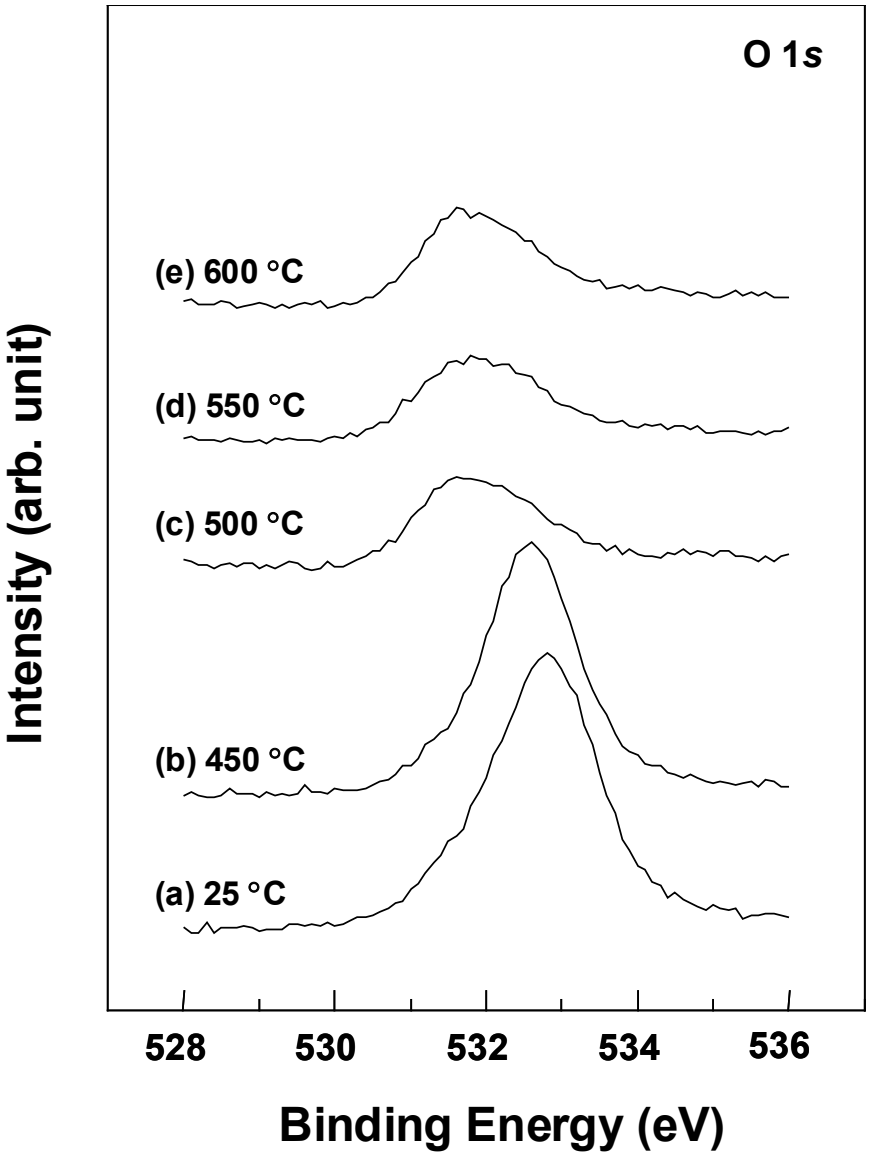


Figure 3.3 XPS O 1*s* core-level spectra from Ge (100) wafers with native oxides for different temperatures. (a) 25 ^{o}C, (b) 450 ^{o}C, (c) 500 ^{o}C, (d) 550 ^{o}C, and (e) 600 ^{o}C

The intensity of the predominant Ge oxide decreased and elemental Ge became the dominant peak. This decrease in Ge oxide resulted from a reduction of the Ge^{4+} state. The Ge^{3+} became the strongest peak with small amounts of Ge^{1+} and Ge^{2+} also present, which shifted the Ge oxide peak to the lower binding energy of the Ge^{3+} oxide state. The intensity of combined oxide spectra decreased. After annealing, the O 1*s* core-level peak intensity decreased by a factor of approximately 3 and shifted toward lower binding energy. This supported the result obtained from Ge core level spectra, namely, an intensity reduction from the combined oxide peaks and a shift of the oxide peak toward lower binding energy indicating a change in oxide states from Ge^{4+} to Ge^{3+}. Further annealing up to 600 ^{o}C produced little change in the spectra.

As shown in the Ge 3*d* and Ge 2*p* spectra, the native oxide state naturally formed in the air was found to be primarily GeO_2 with small amounts of GeO_x ($x < 2$). It has been reported that in situ or chemically prepared oxides consist mainly of GeO_x ($x<2$) [3-9,10]. At 500 ^{o}C, most of the Ge oxides were desorbed, which left the surface rich in elemental Ge instead of the Ge oxides. This thermal desorption of the Ge oxides was marked by a reduction in GeO_2. However, the possibility of desorption of GeO_2 from the Ge surface can be ruled out since GeO_2 is known to be stable up to 1170 ^{o}C [3-10]-[3-11]]. Instead, it appears that GeO_2 thermally decomposed to GeO through an interfacial reaction of $GeO_2 + Ge = 2GeO$ between the native oxide layer and the Ge substrate. This

was then followed by desorption of volatile GeO from the surface [3-9]. GeO is known to sublimate at low temperature [3-13]. At 500 ^{o}C, the Ge oxide peak was close to that of the Ge^{3+} (Ge_2O_3) oxide state.

3.2 RHEED Patterns from Ge Substrates

The reflective-high-energy-electron-diffraction (RHEED) patterns were measured from the Ge substrate at different temperatures in an MBE system. On one occasion, we conducted GaAs epitaxy on Ge substrate in order to increase the Schottky barrier height in metal-germanium-metal photodetectors. The RHEED patterns, as shown in Figure 3.4, were observed in preparation for deoxidation of the Ge substrate.

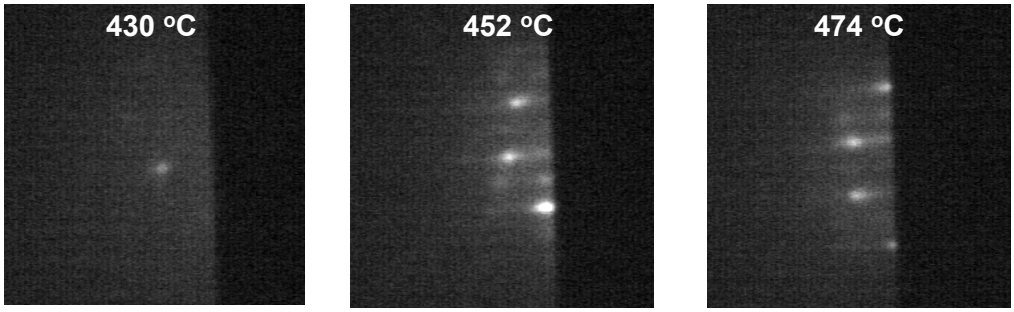


Figure 3.4 Reflective-high-energy-electron-diffraction (RHEED) patterns taken from Ge substrate for different temperature in MBE system

At 430 ^{o}C, essentially clear spots were not yet visible. That indicated that native oxide still existed on the Ge surface. At 452 ^{o}C, some spots started

appearing but they were not well aligned. This indicated deoxidation was underway but was not yet complete. Another possibility was that there were 3-dimensional features on the surface, which resulted in transmission-reflection diffraction. At 474 ^{o}C, spots were aligned in an arc pattern, which indicated deoxidation was almost complete and the surface was very smooth.

3.3 Oxidation of Ge and XPS Study

Another XPS analysis was conducted to study thermal oxidation of Ge. In this experiment, the Ge wafers were annealed using RTA at atmospheric pressure for 1 minute. The annealing ambient was modified to be an oxidizing ambient by intentionally adding a small amount of oxygen (0.5 slm) along with nitrogen (8.0 slm) during the annealing. After the Ge wafers were annealed in the oxidizing ambient, they were loaded into the XPS chamber. The Ge wafers were ex-situ annealed and then transferred into the XPS chamber.

As shown in Figure 3.5, the Ge *3d* spectrum showed little change up to the annealing temperature of 500 ^{o}C. However, significant intensity change was found at temperatures between 500 ^{o}C and 550 ^{o}C. The intensity of elemental Ge was decreased significantly, while the intensity of mixed Ge oxides was increased concurrently. The same trend was found in O *1s* spectra in Figure 3.6. This indicated that oxidation of Ge occurs at temperatures between 500 ^{o}C and

550 ^{o}C. This temperature range was found to be a little higher than the temperature that was required for desorption of Ge oxides in Section 3.1.

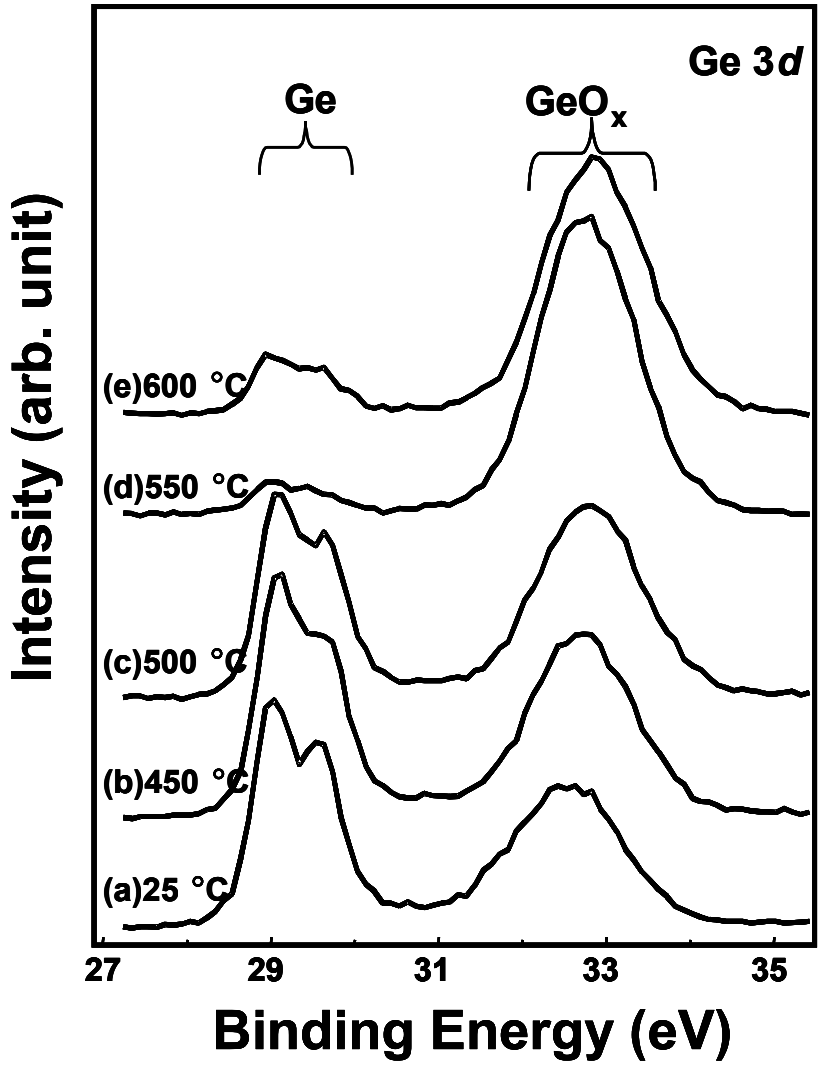


Figure 3.5 XPS Ge 3d (a) and O 1*s* (b) core-level spectra from Ge (100) wafers annealed in oxidizing ambient for different temperatures. (a) 25 ^{o}C, (b) 450 ^{o}C, (c) 500 ^{o}C, (d) 550 ^{o}C, and (e) 600 ^{o}C

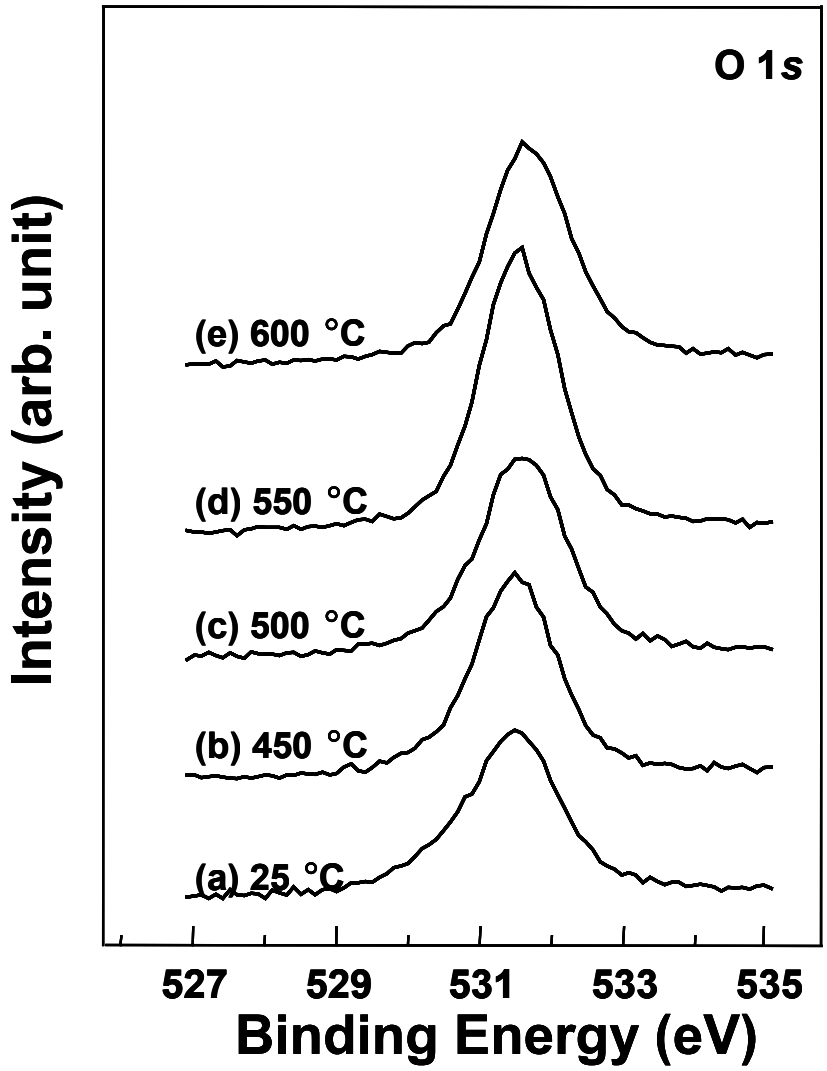


Figure 3.6 XPS O 1*s* core-level spectra from Ge (100) wafers annealed in oxidizing ambient for different temperatures. (a) 25 ^{o}C, (b) 450 ^{o}C, (c) 500 ^{o}C, (d) 550 ^{o}C, and (e) 600 ^{o}C

Figure 3.7 shows the percentage of Ge oxides in Ge *3d* spectra versus the annealing temperature. Two reactions, oxidation of Ge and desorption of Ge, are shown in this figure. As shown in XPS spectra, desorption of oxide took place in the temperature range of 450 ^{o}C ~ 500 ^{o}C, while the oxidation of Ge occurred at temperatures between 500 ^{o}C and 550 ^{o}C. The percentage of Ge oxides was obtained by calculating a relative area of Ge oxide across the entire spectrum.

$$\%\ \text{Ge oxides} = \frac{\text{area (Ge oxides)}}{\text{area (Ge oxides + elemental Ge)}} \qquad (3\text{-}1)$$

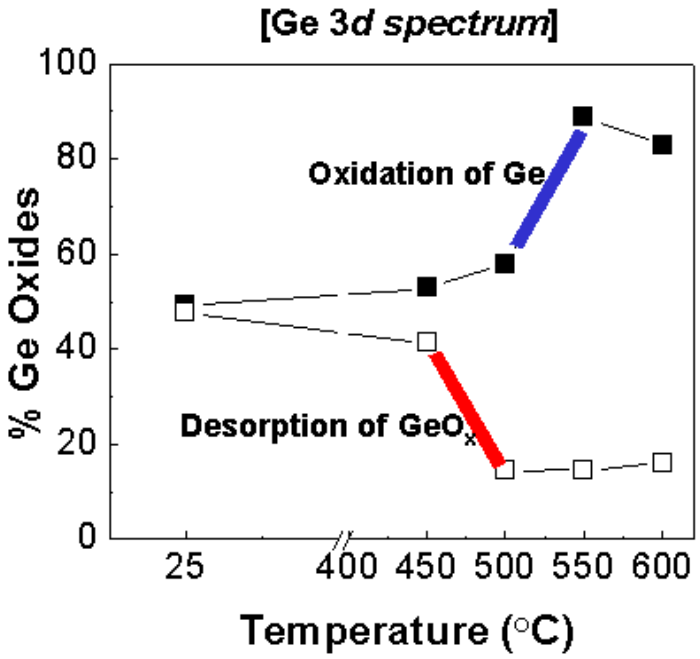


Figure 3.7 Percentage of Ge oxides for oxidation of Ge and desorption of Ge oxides over the annealing temperature

What we found is that if a Ge wafer is annealed at 600 ^{o}C in an oxidizing ambient, two reactions (desorption of Ge oxide and oxidation of Ge) are likely to occur simultaneously. These two successive reactions, oxidation and desorption (deoxidation), are basic mechanisms of an etching process. I believe that thermal desorption and oxidation of Ge resulted in the loss of Ge from the surface. I will discuss this issue in Section 3.4.

3.4 Loss of Ge from the Surface

Ion implanted Ge substrates were used to investigate the loss of Ge from the surface. The samples were ion-implanted with boron or arsenic with a dose of 2 x 10^{15} cm^{-2} at energies of 35 KeV and 60 KeV, respectively. Before annealing, two types of samples were prepared; one by capping the Ge surface with SiO_2 (100 nm) using plasma enhanced chemical vapor deposition (PECVD) at 285 ^{o}C. The other samples were uncapped. The annealing was performed at the temperature of 450 ^{o}C and 500 ^{o}C, so there were five samples including the sample as implanted. After annealing, dopant profiles were measured using secondary ion mass spectroscopy (SIMS) after removing the SiO_2 cap layer. Annealing was performed using a rapid thermal processor (RTP) with a N_2 purge at atmospheric pressure.

Figure 3.8 shows boron profiles from the samples of (a) as-implanted, (b) and (c) annealed at 450 ^{o}C, and (d) and (e) annealed at 600 ^{o}C. The samples

labeled (b) and (d) were capped with SiO_2 layers but (c) and (e) were not. The profiles (a), (b), (c), and (d) are almost identical indicating no boron diffusion in the Ge up to 600 ^oC. The profile (e) obtained at 600 ^oC without a SiO_2 cap layer moved toward the surface by 100 nm compared to the other samples. What this indicates is the loss of Ge from the surface. Approximately 100 nm of Ge was lost from the surface and the implanted B dose decreased by more than one order of magnitude. This shift of profile cannot be explained by outdiffusion of the implanted atoms because the SIMS profiles exhibited a parallel-shift relative to the as-implanted profiles.

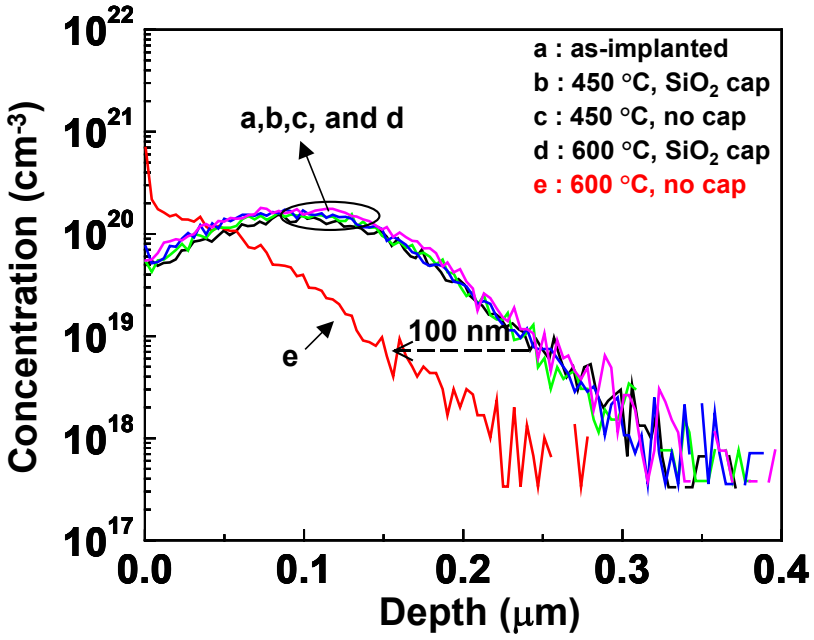


Figure 3.8 SIMS profiles of boron in the Ge wafer with/without SiO_2 cap layer as a function of temperature.

A similar trend was observed for As profiles as shown in Fig 3.9. The profiles showed no As diffusion in Ge up to 450 ^{o}C. Upon annealing at 600 ^{o}C, the profile was characteristic of As diffusion. The remaining As doses of samples annealed at 600 ^{o}C with and without a SiO_2 cap layer were 1.5 x 10^{15} cm^{-2} and 2.5 x 10^{14} cm^{-2}, respectively. The capped samples retained most of the initial As implant dose of 2.0 x 10^{15} cm^{-2}. The capless samples, however, experienced a one order of magnitude decrease. The profile obtained at 600 ^{o}C without a SiO_2 cap layer moved toward the surface by 350 nm, which reflected the loss of Ge from the surface. This surface loss resulted from the simultaneous reactions that happened to the surface during the annealing process, as discussed in the previous section. If a Ge wafer is annealed at 600 ^{o}C with some background oxygen present, these two reactions compete and result in the loss of Ge from the surface. This surface loss which is due to thermal desorption of Ge oxides can be avoided by depositing SiO_2 on the Ge wafer.

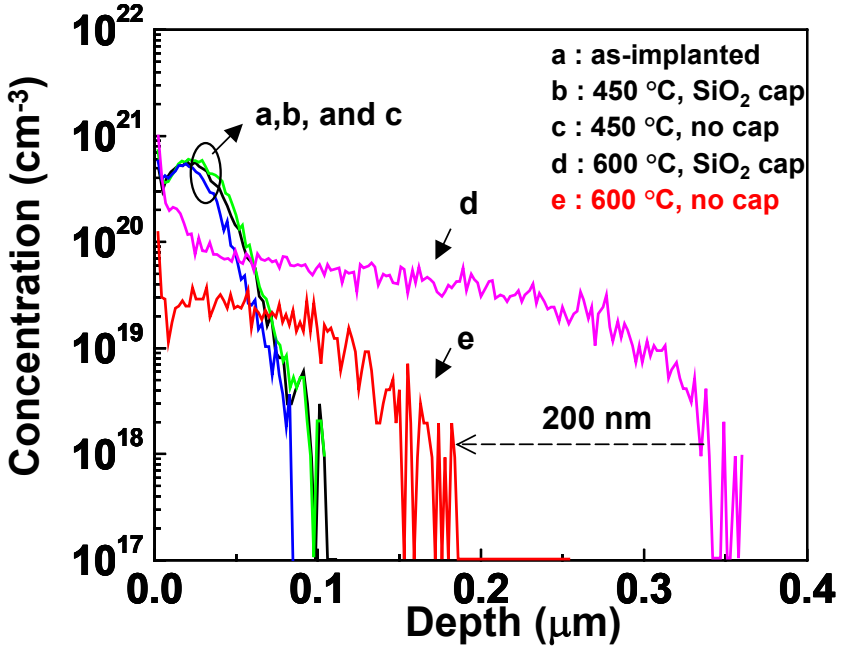


Figure 3.9 SIMS profiles of arsenic in the Ge wafer with/without SiO2 cap layer as a function of temperature.

3.3 Summary

We have investigated the thermal characteristics of Ge oxides using XPS and SIMS analyses. The native Ge oxide was found to consist primarily of GeO_2 with small amounts of GeO_x (x<2). The thermal desorption of Ge oxide occurred at the temperatures of 450 ^{o}C ~ 500 ^{o}C. Since GeO_2 is known to be stable up to 1000 ^{o}C, we believe that GeO is the oxide state that is desorbed. It

is likely that GeO was desorbed through an interfacial reaction between GeO_2 and Ge.

Dopant profiles were measured from ion-implanted samples. By examining the depth profiles, it was observed that the uncapped samples lost more than 100 nm of Ge from the surface after annealing at 600 ^{o}C but no surface loss was observed for the capped samples at the same temperature. It is likely that the SiO_2 cap layer blocked the absorption of oxygen and prevented further oxidation of the Ge.

In addition, it was found that thermal desorption of volatile Ge oxides and oxidization of Ge occurred successively, which resulted in the loss of Ge from the surface. The implantation profiles confirmed the loss of Ge from the surface and an XPS analysis indicated that this was preceded by oxidation and thermal desorption of the Ge oxides, which took place simultaneously.

Chapter 4

Growth and Characterization of Ge Epitaxial Layers

In crystal growth, both lattice strain and surface free energy determine the growth mode. A classification of the three basic modes of heteroepitaxial growth was first proposed by Bauer [4-1] as layer-by-layer growth (Frank-Van der Merwe), islanding growth (Volmer-Weber), and layer-by-layer growth followed by islanding growth (Stranski-Krastanov). A variety of researchers have reported that the growth of Ge on Si occurred as Stranski-Krastanov growth [4-2]-[4-10].

In the absence of any strain in the epitaxial layer, considering only thermodynamic free energies, theoretical models of epitaxial growth mode are determined by the free energy of the substrate surface (σ_s), the interface free energy (σ_i), and the surface free energy of the heteroepitaxial layer (σ_f). The inequality $\sigma_s > \sigma_f + \sigma_i$ sets the condition for the epitaxial film to wet the substrate [4-8]. Ge has a lower surface free energy than Si, and σ_i may be considered insignificant. The growth of Ge on Si is therefore predicted to be layer-by-layer growth (Frank-Van der Merwe), not taking into account the strain energy of the film. However, since there is a lattice mismatch between Ge and Si, the accumulation of strain energy is expected to produce islanding growth

after a certain thickness of the epitaxial layer is exceeded, so the growth of Ge on Si, in fact, occurs as Stranski-Krastanov (SK) growth.

4.1 Ge Epitaxy on Si Substrates using SiGe Buffer

In collaboration with Motorola and Unaxis, Ge epitaxial layers were grown on a graded $Si_{1-x}Ge_x$ buffer layer on Si (100) substrate using Unaxis's low energy plasma enhanced chemical vapor deposition (LEPE-CVD). The advantage of the Unaxis LEPE-CVD system is its fast growth rates in the range of 45 Å/s to 60 Å/s. The growth rates of conventional UHV-CVD or MBE are typically on the order of a few angstroms per second. For practical purposes, a short growth time for a thick SiGe buffer is advantageous.

To relieve strain induced from the lattice mismatch, a 10 μm-thick compositionally graded SiGe buffer was used. The buffer layers were effective in relieving the strain and blocking the propagation of threading dislocations. As a result, high quality Ge epitaxial layers with a low threading dislocation density of ~ 10^5 cm^{-2} were obtained, and surface morphology was smooth. Figure 4.1.1 shows a schematic cross-sectional view of a 1 μm-thick Ge layer grown on a 10 μm-thick SiGe buffer layer on Si (100) substrate.

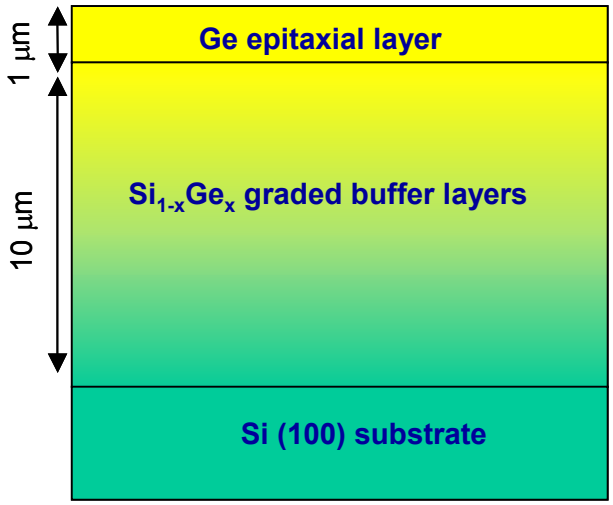


Figure 4.1 Schematic cross sectional view of a 1 μm-thick Ge layer grown on a 10 μm-thick SiGe buffer layer on Si (100) substrate

4.1.1 LEPE-CVD (Low Energy Plasma Enhanced Chemical Vapor Deposition)

In a LEPE-CVD reactor, compositionally-graded thick SiGe buffer with Ge concentrations up to 100% can be grown on Si substrate with high growth rates but at low substrate temperatures below 600 °C [4-9,10]. The utilization of plasma enhancement allows higher deposition rates at even lower temperatures. However, for epitaxial layers, the energy of the particles in this plasma must be controlled to prevent damage to the single crystal structure. In a LEPE-CVD, the ion energies can be controlled below the sputtering threshold. Thanks to the low energy characteristics of plasma, the wafer can be directly exposed to the plasma. In addition, the high electron density in the discharge helps to

efficiently dissociate the precursors (SiH_4, GeH_4, and PH_3) into more reactive radicals. An intense but low energy bombardment of the surface during growth enhances the surface reaction as well. This results in a high deposition rate and increases the utilization of the precursors, which is of particular importance for expensive gases like germane (GeH_4). Figure 4.2 shows a schematic of the LEPE-CVD system.

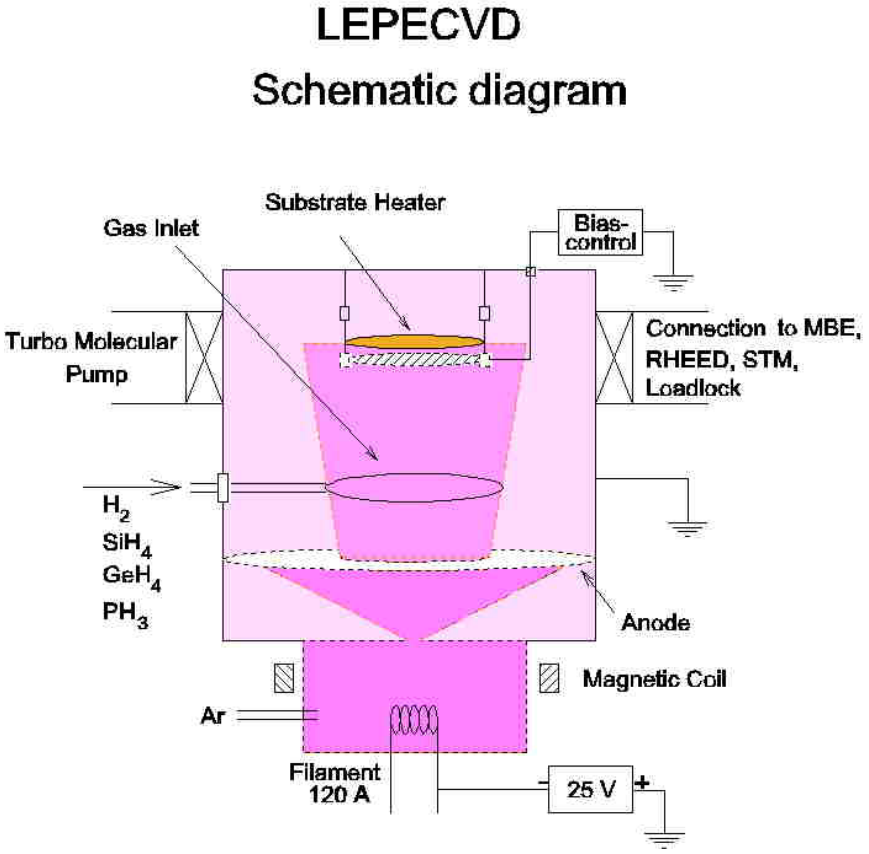


Figure 4.2 Schematic of the LEPECVD system. The growth chamber is connected to standard analysis tools as RHEED, XPS and UBS, and a UHV STM/BEEM

4.1.2 TEM Analysis

Cross-sectional and plan-view TEM images were measured for a relaxed 1 μm-thick Ge epitaxial layer grown on a 10 μm-thick compositionally graded SiGe buffer layer on Si (100) substrate. Figure 4.3 shows cross-sectional TEM images. Dislocations were mostly confined to the graded buffer layer, yielding high-quality threading dislocation free Ge layers. The fact that the top Ge exhibited a low dislocation density indicates that the buffer layers were effective in relieving the strain and blocking the propagation of threading dislocations. Figure 4.4 (a) shows a high-resolution TEM image measured from the defect-free region. The selected area diffraction pattern showed well-aligned bright spots, which are characteristic of a high quality single crystal.

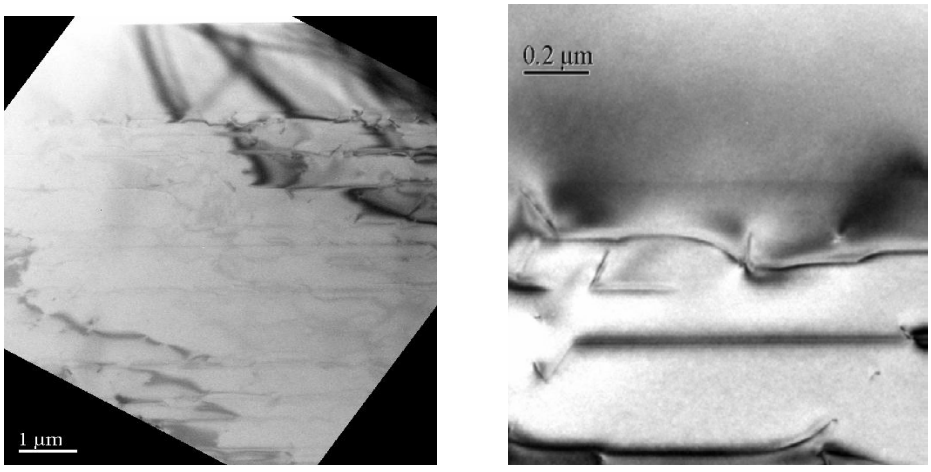
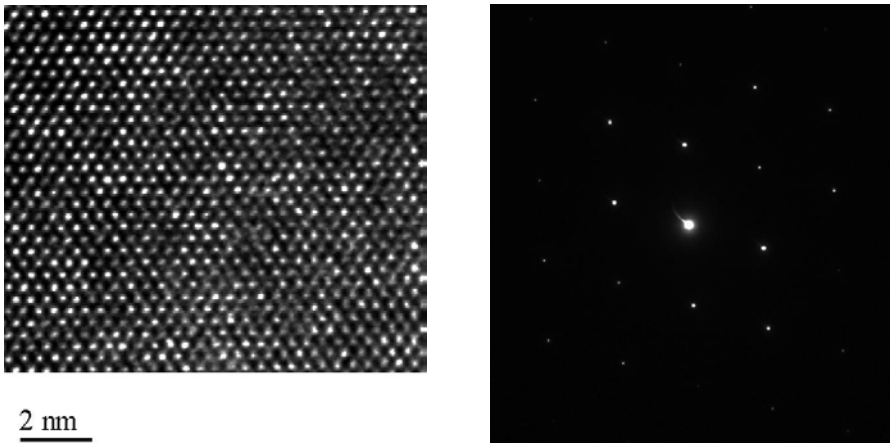


Figure 4.3 TEM cross-sectional images of Ge epitaxial layers grown on compositionally graded SiGe buffer layer on Si (100) substrates



(a) (b)

Figure 4.4 (a) TEM high-resolution image (b) Selected Area Diffraction (SAD) pattern

4.1.3 Etch Pit Density Measurements

The low threading dislocation density was difficult to determine by cross-sectional TEM, so etch pit density measurements were used. These measurements indicated that the threading dislocation density was as low as 1.5 x 10^5 cm^{-2}, which was an order of magnitude improvement over previously reported Ge-on-Si [4-11]-[4-14]. A mixture of CH_3COOH (67 ml), HNO_3 (20 ml), HF (10ml), and I_2 (30 mg) was used for etch pit density measurement [4-12]. An optical microscope was used to count the number of etch pits.

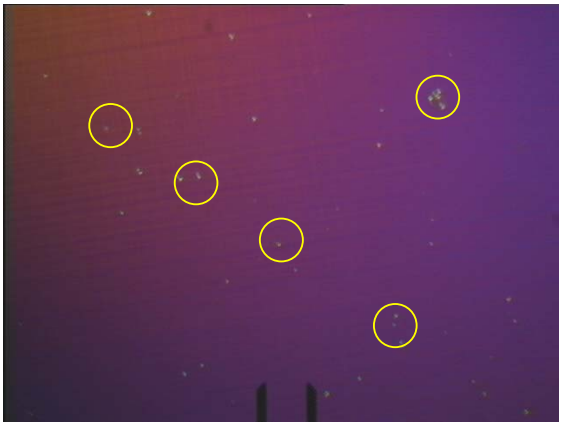


Figure 4.5 Etch pit density results of Ge on SiGe graded buffer on Si (100) substrate

4.1.4 AFM Measurements

Atomic force microscopy (AFM) is a technique that allows three-dimensional imaging of surfaces with sub-nanometer resolution. In this study, the tapping mode of a Digital Instrument Dimension 300 was used for AFM imaging.

Figure 4.6 shows AFM images of Ge-on-Si grown using an LEPE-CVD deposition system. AFM measurements of the surface morphology yielded a root-mean square (RMS) roughness of 3.3 nm. Clearly defined surface cross-hatch patterns were observed, which is consistent with effective strain relief through misfit dislocations. The surface roughness was mainly caused by the cross-hatch patterns. However, ordered and straight cross-hatch lines indicated

that strain relaxation was efficiently achieved by a periodic array of misfit dislocations in SiGe buffer layers.

The compressive strain in the Ge layer due to the lattice mismatch was mostly relaxed by creating threading dislocations in the graded SiGe buffer. Although these dislocations did not propagate into the top Ge layer, they caused the formation of cross-hatch patterns along the (110) and (1-10) directions. The AFM image clearly showed the cross-hatch patterns with a rms roughness of 3.3 nm that corresponds to about 12 atomic steps.

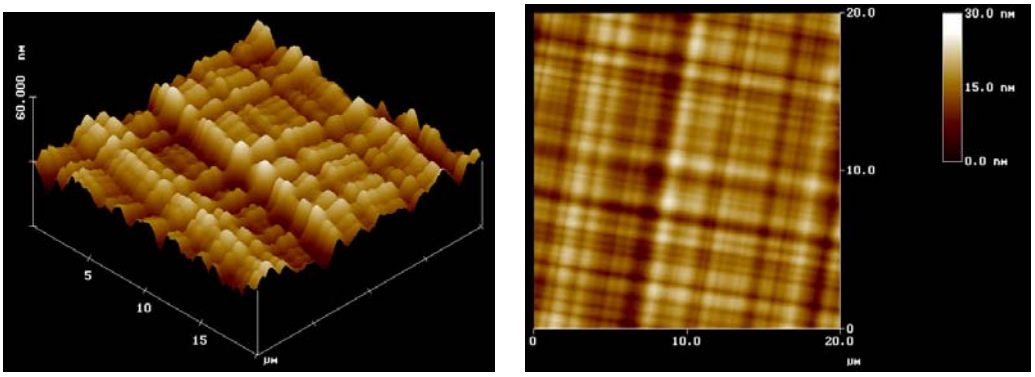


Figure 4.6 AFM images of Ge-on-Si deposited using an LEPECVD system. Root-mean square (RMS) roughness was 3.3 nm.

4.1.5 X-ray diffraction Measurements

The x-ray diffractions (XRD) were measured using a Philips X'Pert MRD (Material Research Diffractometer) high-resolution x-ray diffractometer at the Microelectronics Research Center at the University of Texas at Austin. A point focusing source of x-ray (characteristic Cu $K_{\alpha 1}$ and $K_{\alpha 2}$ radiation: λ=1.5405 Å and 1.5443 Å, respectively) was collimated and the energy was filtered by a four-crystal (i.e., four reflection) Ge (220) beam conditioner to achieve high angular resolution. The monochromatic and collimated primary x-ray beam was diffracted from a particular set of planes of the sample and then the diffracted beam was detected at either of the detector positions (a proportional detector filled with Xe gas), depending on secondary optic setting.

Figure 4.7 shows ω-2θ XRD measurements. Inhomogeneous broadening was due to the compositionally-graded SiGe buffer layer, which is apparent at intermediate 2θ values between the Ge (004) and Si (004) diffraction. The thickness of the Ge epitaxial layer greatly exceeded the critical thickness. Based on the diffraction angles and lattice constants, the Ge epitaxial layers were found to be fully relaxed and oriented in the (004) direction. The full width at half maximum (FWHM) was measured to be 466 arcsec and 59 arcsec for the Ge and Si peaks, respectively. X-ray diffraction measurements provided evidence that Ge epitaxial layers were high-quality single crystals.

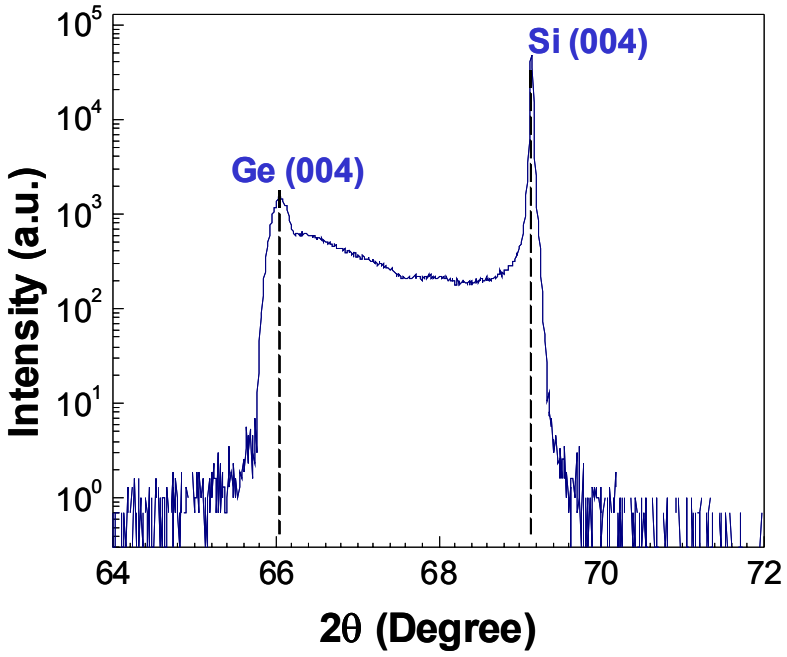


Figure 4.7 X-ray diffraction measured from a 1μm-thick Ge epitaxial layer grown on a 10 μm-thick SiGe buffer on Si substrates (θ = angle of incidence)

Figure 4.8 shows another ω-2θ diffraction wide scan obtained from the same sample using Motorola's Rigaku RU200-BH rotating anode x-ray generator (50 kV, 200 mA, 1° divergence slit) and a D-MAXB 2θ goniometer.

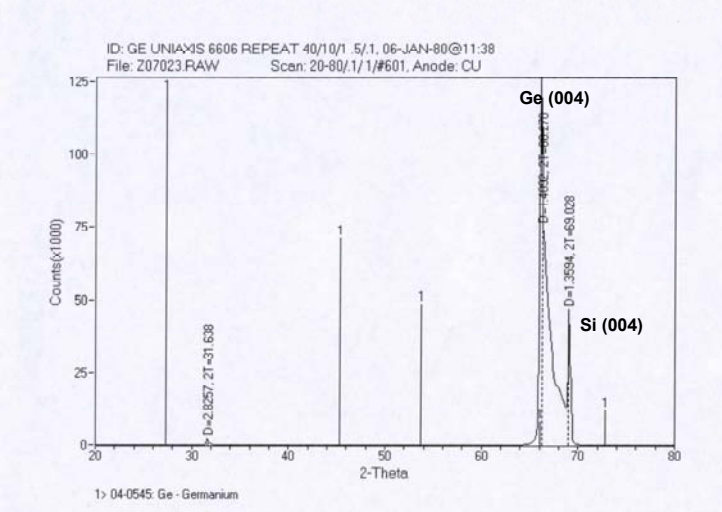


Figure 4.8 X-ray diffraction measured from a 1μm-thick Ge epitaxial layer grown on a 10 μm-thick SiGe buffer on Si substrates (θ = angle of incidence)

4.1.6 Spectroscopic Ellipsometry

The sample was also submitted for Spectroscopic Ellipsometry and for Raman analysis. Ginger Edward and Ran Liu in the *Process & Materials Characterization Laboratory* at Motorola conducted these measurements and summarized the crystal quality. Results and discussion are provided below.

The ellipsometric angles ψ and Δ were obtained on the sample using a J.A. Woollam vertical VASE ellipsometer from 2.0 to 6.0 eV at angles of incidence of 65°, 70°, and 75°. The identity of the heterostructure layers was determined via the standard three-phase model calculation provided in the

WVASE32 data analysis software. Results showed that the crystal quality was almost comparable to bulk Ge wafer.

Figure 4.9 shows pseudodielectric functions ε1 and ε2 obtained on the Ge epitaxial layer for three angles of incidence. The model and experimental fits are shown in solid and dashed lines, respectively. The best fit to the data was obtained by creating a multi-layer stack composed of ~15 Å GeO_2 on top of an optically opaque layer of Ge. The quality of the fit indicated that Ge epitaxial layer was nearly as good as bulk Ge. However, there was a small discrepancy in the circled fit region. This indicates that though the sample was very promising, there is room for further improvements in crystal quality.

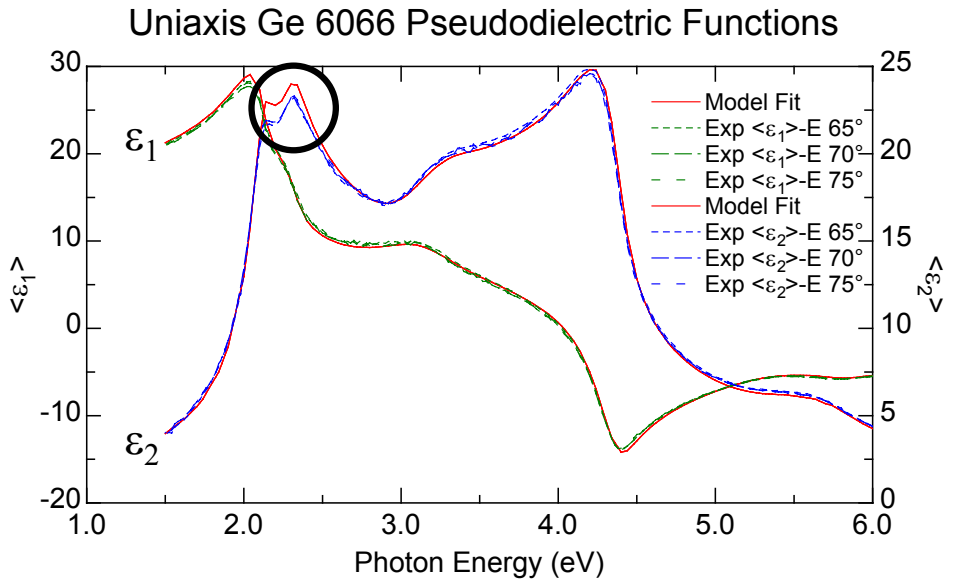


Figure 4.9 Spectroscopic Ellipsometry (SE) results on a Ge epitaxial layer grown on Si substrates

4.1.7 Raman Measurement

Figure 4.10 shows the polarized Raman spectra of the epitaxial Ge layers as well as of the bulk Ge wafer from Union Minere. The phonon peak was strongest when both incident and scattered light were polarized along the (110) direction and almost vanished when polarized along the (100) axis. The residue peak intensity in the forbidden geometry was caused mostly by imperfect polarization and sample angle alignment. It can be seen that the ratios of the allowed and forbidden intensities were almost the same between a Ge epitaxial layer and a bulk Ge wafer. This suggests that the Ge was epitaxially grown with crystal axes coinciding with that of the Si substrate.

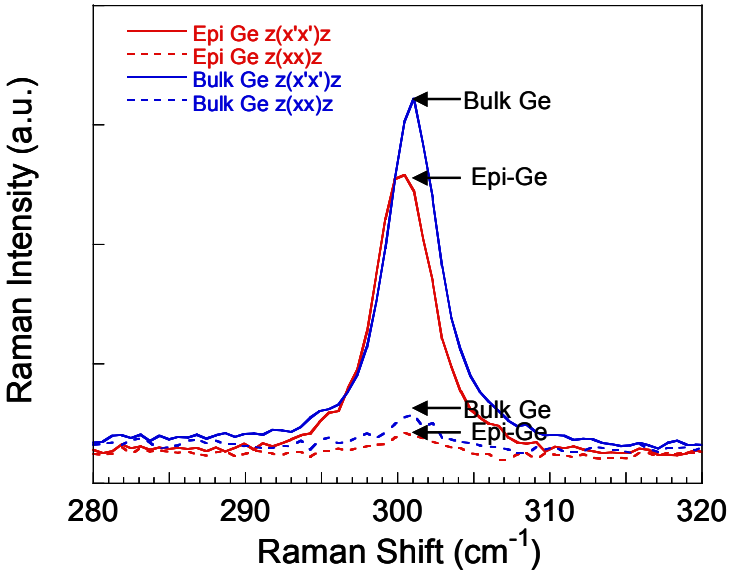


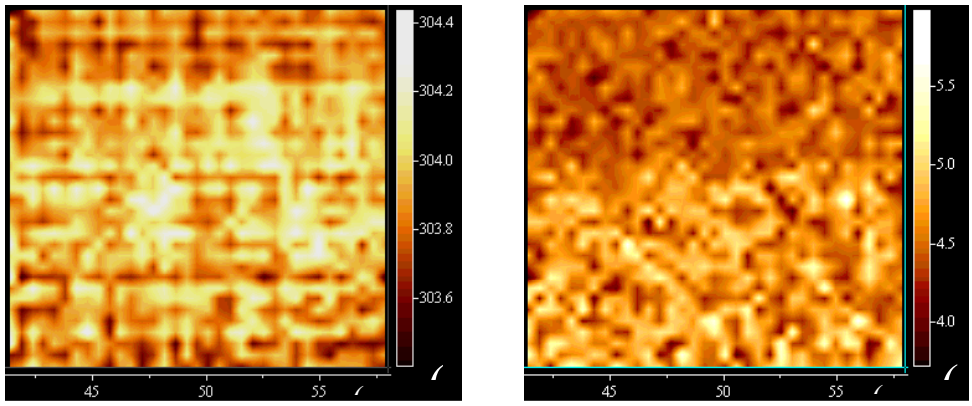
Figure 4.10 Polarized Raman spectra of the epitaxial Ge and of a bulk single crystal Ge wafer in both allowed (solid lines) and forbidden (dashed lines) scattering geometry

The peak width of the epitaxial Ge film was slightly larger than that of the Ge reference (4.2 cm^{-1} vs. 4.0 cm^{-1}). This indicates very low defect density in Ge epitaxial layers, which is in agreement with the TEM results. As the peak position occurred at almost the same frequency for the epitaxial Ge layer and bulk Ge, the Ge epitaxial layer was nearly completely relaxed.

A question that arises regarding this measurement is why the phonon frequency in the epitaxial Ge film, 300.4 cm^{-1}, was slightly lower than that of the bulk Ge reference, 301.0 cm^{-1}. This mode-softening in the Ge film seems to indicate a minor tensile strain of ~ 100 MPa, which contradicts the fact that the larger Ge lattice constant should lead to a compressive strain due to lattice constant mismatch between Ge and Si. It is not yet clear if this residue strain was caused by a difference in the thermal expansion coefficients of the Ge epitaxial layer, the SiGe buffer, and Si substrate.

To characterize the distribution of the residue strain across the cross-hatch, we performed Raman mapping on a 15 μm x 15 μm area with a scanning step of 0.5 μm. Figure 4.11 (a) shows an image of the phonon frequency. Since there were no other factors such as composition or poor crystallinity affecting the phonon frequency in this case, this image reflected the residual strain field near the surface. It was shown that the strain field correlated well with the surface cross-hatch patterns with a strain variation of about 0.001 or stress variation of about 130 MPa. Figure 4.11 (b) shows an image of the phonon peak.

The change in the width was mostly caused by convolution of peaks due to the strain gradient within the laser spot (~0.4 μm). No significant peak broadening due to defects was observed.



(a) (b)

Figure 4.11 Raman 2-D mapping of the Ge phonon frequency (a) and width (b) for the epitaxial Ge. The frequency image correlates very well with the surface cross-hatch structures seen in AFM and micro-optical images

4.2 Ge Epitaxy Directly on Si Substrates

For a more practical approach to the fabrication of monolithically integrated Si-Ge optical receivers, thin epitaxial layers of Ge were directly deposited on Si substrates. The challenge to this direct deposition was how to accommodate the lattice mismatch of 4 % without significant degradation in the material quality. In the absence of strain-relaxation layers, the strain induced from the lattice mismatch was relieved by forming islands after 3-4 MLs of

growth, which resulted in rough surface morphology and poor carrier transport characteristics due to high density of defects.

Many techniques have been used to improve Ge epitaxy. It was reported that the incorporation of carbon, a small lattice constant element, in the Ge layers compensated for the lattice mismatch with Si substrate [4-15,16]. However, the low solid solubility of C in Ge (10^8 atoms/cm^3) limited the carbon fraction in the Ge substitutional sites to as low as 2% ~ 3% under metastable conditions. Another approach to the island formation problem was to use a group V element as a surfactant [4-17]-[4.21]. Surfactant-mediated epitaxy (SME), however, resulted in an undesirable doping of the Ge layer.

Our approach to overcome island formation was to grow the Ge layers at low temperatures. The growth kinetics of Ge at low temperatures has not been well studied. However, it was reported that in a low temperature regime, where the growth rate was surface reaction limited, the heteroepitaxial growth mode was layer-by-layer [4.22]. Above the transition temperature, the growth rate was controlled by diffusion and adsorption of GeH_4 from the gas phases, and the growth mode changed to Stranski-Krastanov (SK). It appeared that the layer-by-layer growth in the low temperature region was due to the control of the growth kinetics by a surface reaction mechanism, for example, the H_2 desorption step prior to lattice incorporation of the Ge. The GeH_x surface species were likely to be less mobile (and less reactive) than Ge adatoms due to hydrogen termination

at the growth interface, which thereby reduced the overall surface mobility and prevented island formation.

4.2.1 UHV-CVD System

Figure 4.12 shows a cold-wall UHV-CVD deposition system at the Microelectronics Research Center at the University of Texas at Austin. A load-lock chamber was used to prevent the main chamber from being exposed to atmosphere during wafer loading. A turbo pump and a mechanical pump were used to bring the load lock chamber to a pressure of below $1x10^{-7}$ Torr. Then, the wafers were transferred into the main chamber. A sorption pump was connected in parallel with the turbo pump to allow quick pump-down of the load lock chamber after wafers had been loaded. The main chamber was pumped to a base pressure of 5×10^{-10} Torr using a Balzers turbomolecular pump with a pumping speed of 330 l/s. It was backed by a dual-stage Alcatel mechanical pump with a rated foreline pressure of 10^{-4} Torr.

The substrate heater was attached to the top of the main chamber. The heater consisted of five quartz-halogen lamps enclosed in a molybdenum box. The lamps were powered by a single-phase 120 V SCR, which was manipulated by a temperature controller. The substrate was held with its backside facing the lamps and was supported by three quartz pins. For this heater design, feedback was not used for temperature control. Instead, a Sensarray sensor wafer was

used to determine a reference temperature. Periodic modification of the heater power was needed to account for aging and coating of the lamps. This heater arrangement did not allow rapid variation in deposition temperature. However, the growth rates were not always reproducible because of the open-loop control. The temperature was pyrometrically measured at the center and the edge of the wafer.

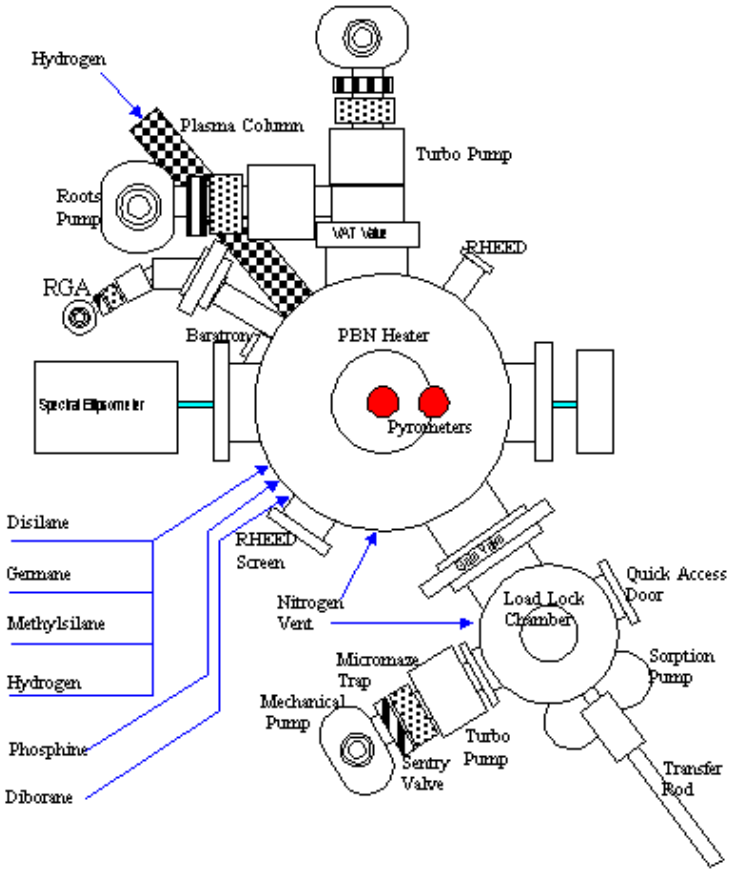


Figure 4.12 UHV-CVD growth system used for this work

4.2.2 Material Characterization

As stated above the Ge epitaxial layers were grown using UHV-CVD system at base pressures of low 10^{-9} Torr. The Si substrates were p-Si (100) wafers with resistivity in the range of 5-25 Ω-cm. The Si substrates were Piranha-cleaned with H_2O_2+H_2SO_4 (1:2) solution and rinsed in de-ionized water. Native oxides were etched in diluted HF solution for 10 seconds, spin-dried in nitrogen, and then loaded into the load-lock chamber. Quartz-halogen lamps heated the substrates and the temperature was measured pyrometrically. A mixture of 20 % GeH_4 in a carrier gas of helium was used as the Ge source and its flow was set at 10 sccm with a GeH_4 partial pressure of 2-3 mTorr. Typical depositions were carried out at nominal temperature of 380 ^oC.

Figure 4.13 shows X-ray diffraction (XRD) measured from a 700 nm-thick Ge epitaxial layer grown on Si substrates. Two peaks due to Bragg reflection from Ge (004) and Si (004) planes are clearly visible. Since the thickness of the Ge epitaxial layer greatly exceeded the critical thickness, the Ge epitaxial layer was fully relaxed and oriented in the (004) direction. The full width at half maximum (FWHM) was measured to be 402 arcsec and 21 arcsec for the Ge and Si peaks, respectively.

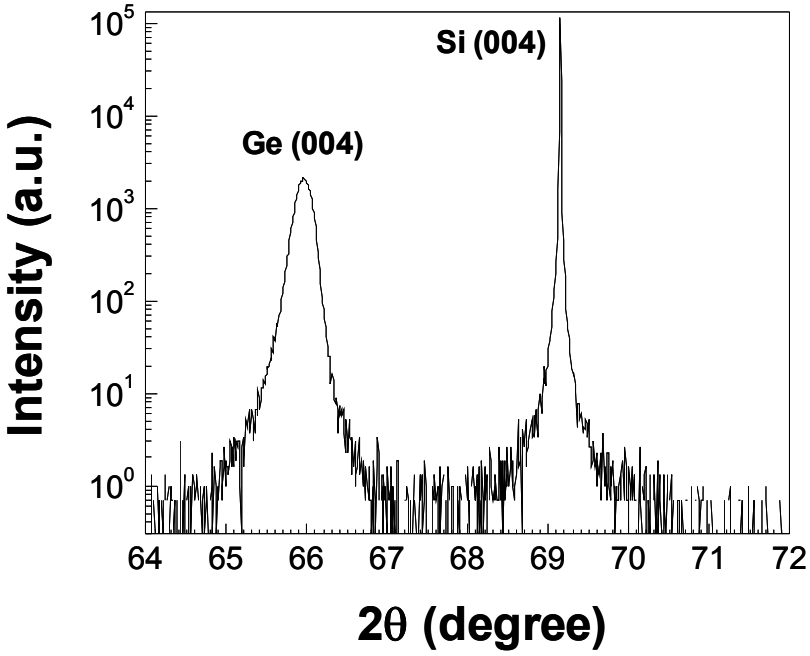


Figure 4.13 X-ray diffraction measured from a 700 nm-thick Ge epitaxial layer grown on Si substrates (θ = angle of incidence)

Figure 4.14 shows a cross-sectional TEM image taken for a relaxed Ge epitaxial layer directly grown on Si (100) substrate. Due to direct growth without using buffer layers, there were many defects including threading dislocations in the Ge epitaxial layer. However, the growth proceeded layer-by-layer in a two-dimensional mode, which resulted in a smooth surface. More defects were found near the heteroepitaxial interface and fewer defects toward the surface. Selected area diffraction measurements confirmed that the layer was a single crystal.

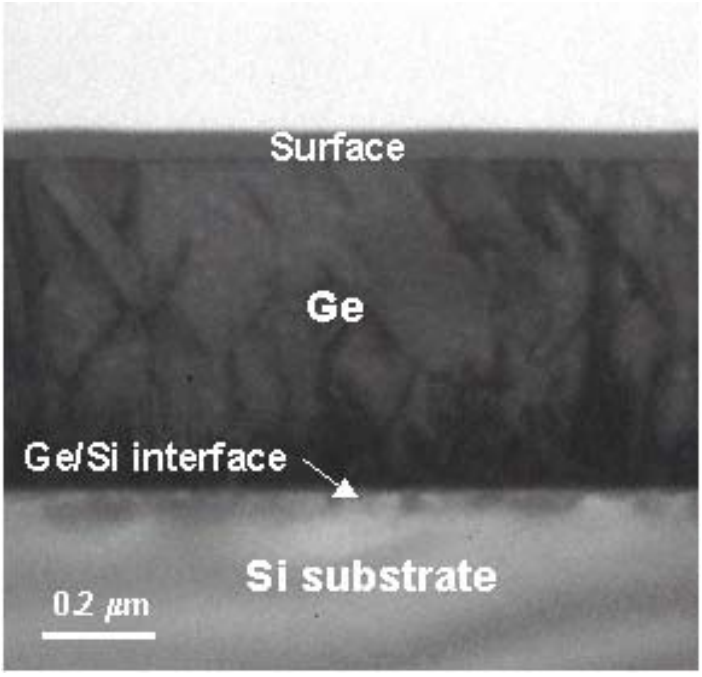


Figure 4.14 TEM cross-sectional image of Ge epitaxial layer grown directly on Si substrates

Hall effect measurements showed the Ge epitaxial layers to be p-type with acceptor concentration of ~10^{17} cm^{-3}. This was closely associated with the structural imperfection of the Ge films, which resulted mainly from the Ge-Si lattice mismatch. It has been reported that structural defects in Ge lead to acceptor states near the valence band edge [4.23]. Figure 4.15 shows the localized energy states caused by these structural defects.

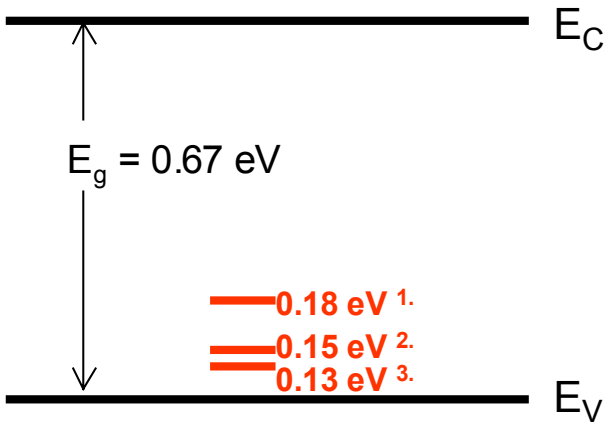


Figure 4.15 Localized energy levels due to structural defects

The samples were submitted for secondary ion mass spectroscopy (SIMS) analysis to identify any possible dopants that might have been introduced during the deposition. Figure 4.16 shows the SIMS analysis. The boron concentration in Ge layers was measured to be as low as 6 x 10^{15} atoms/cm^3, which was the detection limit for the analysis. The phosphorous concentration in the samples was at the instrumental background. What this indicated was that the background doping was not the cause of the acceptor concentration of ~10^{17} cm^{-3}. Instead, the p-type Ge was attributable to structural imperfection.

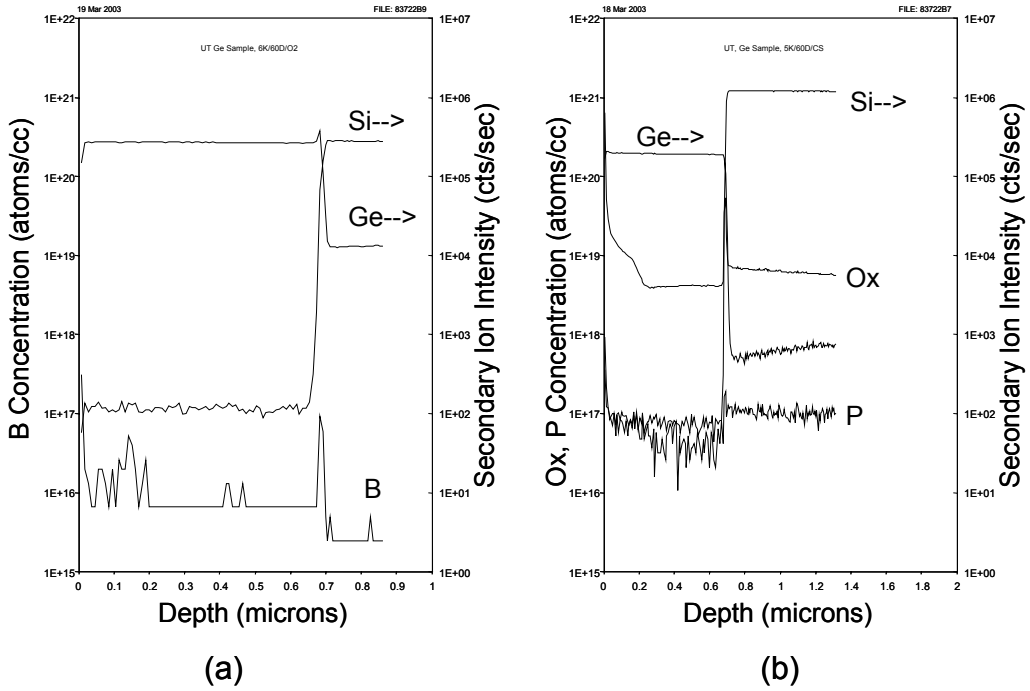


Figure 4.16 SIMS profiles of boron (a) and phosphorous (b) in the Ge epitaxial layer grown on Si substrates using a UHV-CVD system

Figure 4.17 shows AFM measurements of the surface morphology. The root-mean square (RMS) roughness was measured to be 2.5 nm. The rms roughness of previously reported Ge epitaxial layers grown on Si substrate using SiGe buffer layers was 3.2 nm [4-24]. The surface roughness was mainly caused by the cross-hatch patterns. Ordered and straight cross-hatch lines indicated that strain relaxation was efficiently achieved by a periodic array of misfit dislocations in SiGe buffer layers. For direct deposition of Ge epitaxial layers on Si substrates, the cross-hatch patterns were not observed on the surfaces of Ge.

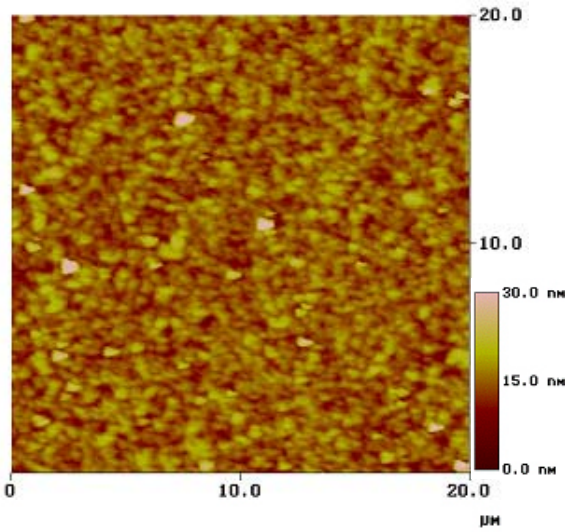


Figure 4.17 AFM image of Ge epitaxial layers grown directly on Si substrates, Root-mean square (RMS) roughness was 2.5 nm

4.3 Summary

Ge epitaxial layers were grown on Si substrate using 10 μm-thick compositionally graded SiGe buffer layers. A fast growth rate of 45 Å/s ~ 60 Å/s was achieved using Unaxis's low energy plasma enhanced chemical vapor deposition. The use of thick SiGe buffer was effective in relieving the strain and blocking the propagation of threading dislocations, which resulted in high-quality Ge epitaxial layers. The threading dislocation density was ~10^5 cm^{-2} and RMS surface roughness was 3.2 nm. XRD clearly showed the diffractions of Ge (004) and Si (004). Based on the calculation of diffraction angles and lattice

constant, the Ge layer was found to be fully relaxed and oriented in (004) direction. For a more practical approach, Ge epitaxial layers were grown directly on Si substrates. The Ge epitaxial layer was found to be very defective with threading dislocation density of $10^8 \sim 10^9$ cm^{-2}. Also, this layer was p-type with acceptor concentration of $\sim 10^{17}$ cm^{-3}. This was closely associated with the structural imperfection of the Ge films, which resulted mainly from the Ge-Si lattice mismatch. By using a low temperature growth technique, however, the growth proceeded layer-by-layer in 2-dimensional mode, which resulted in a smooth surface. A root-mean square (RMS) roughness was measured to be 2.5 nm.

Chapter 5

Photodetector Fabrication

This chapter will provide an overview of the fabrication process and a discussion of the process/integration techniques. The major processes in the fabrication of interdigitated PIN Ge photodetectors include ion implantation, metallization, and surface passivation. In the beginning of this project, I worked on the development of optimum conditions for these processes using bulk Ge wafers. The wafers were Sb-doped n-type and the resistivity was 1-5 Ω-cm. The thickness was approximately 170 μm. The sheet resistance was determined to be 178 Ω/□ by a four probe technique.

Subsequently, I conducted research on Ge epitaxy on Si substrate. Two types of Ge-on-Si wafers were grown for the fabrication of the Ge photodetectors on Si substrates. One was Ge (1μm)/GeSi (10μm)/Si-substrate, which was used for the fabrication of interdigitated PIN Ge photodetectors. The other layer structure was Ge (700nm)/Si-substrate, which was used for MSM photodetectors.

5.1 Interdigitated PIN photodetector Fabrication Process

Schematic top and cross-sectional views of the interdigitated photodetector fabricated on Ge (1μm)/GeSi (10μm)/Si-substrate are shown in Figure 5.1. The planar interdigitated Ge PINs were fabricated starting with the formation of p^+-and n^+-fingers using ion implantation. Interdigitated patterns of 1 μm width and 2 μm spacing were defined by photoresist. The wafer was implanted with boron at an energy of 35 KeV and a dose of 2 x 10^{15} cm^{-2} to form the p^+-fingers. Subsequently, the n^+-fingers were patterned and implanted with phosphorous at an energy of 60 KeV and a dose of 2 x 10^{15} cm^{-2}. After implantation, the photoresist was removed using oxygen plasma and then the activation annealing was performed.

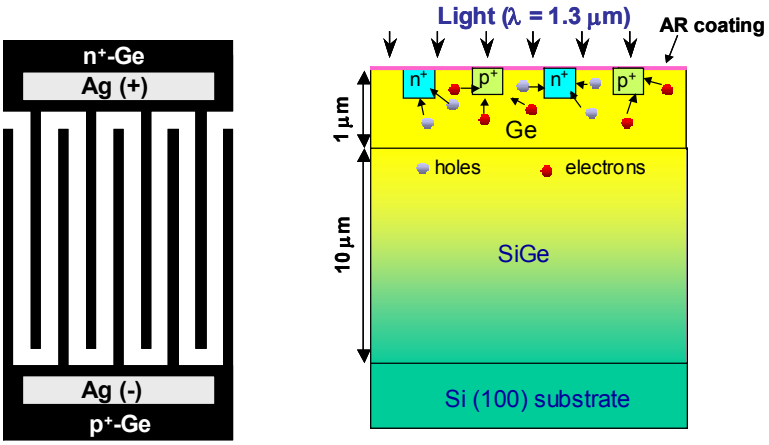


Figure.5.1 Ge photodetector with interdigitated p^+- and n^+-fingers fabricated on Ge-on-Si substrate (a) Top view (b) Cross-sectional view

The rapid thermal annealing used in this work was not a vacuum system. Some background oxygen existed in the annealing ambient. To minimize any undesirable oxidation during the annealing, the annealing tube was purged with ultra-high purity nitrogen gas for at least 5 min. As discussed in Chapter 3, oxidation of Ge and desorption of Ge oxides resulted in an undesirable loss of Ge from the surface. Following the activation annealing, a SiO_2 layer (1000 Å) was deposited on top of the active area for passivation. Additionally, this SiO_2 layer can serve as an anti-reflection coating. The third mask layer was used for the formation of ohmic contacts to p^+- and n^+-Ge. Two micrometer wide contact bars were patterned at the ends of the fingers and the SiO_2 layer was etched. This was followed by the pad photolithography step using the final mask layer. Silver was deposited on the p^+- and n^+-Ge and on the metal pads using an electron beam evaporator. Then, a lift-off process was performed. Prior to evaporation, native oxide was removed using a $HCl:H_2O$ (1:1) solution and a de-ionizing rinse. The contact was annealed at 400 °C for 1min by rapid thermal annealing. Figure 5.2 shows the complete interdigitated PIN photodetector having 1 μm finger width and 2 μm spacing with 50 x 50 μm^2 active area.

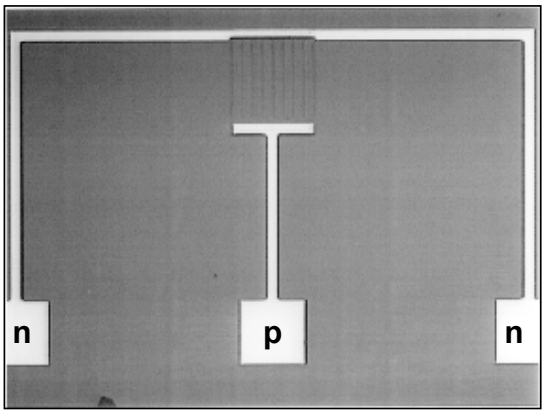


Figure 5.2 Completed interdigitated PIN photodetector. Ion-implanted fingers are not visible clearly, especially after activation annealing.

Figure 5.3 shows the I-V characteristic measured for annealing temperature in the range of 200 °C - 400 °C. Ohmic behavior was observed even in the as-deposited state, and the contact resistivity decreased very slightly with increasing annealing temperature. Sometimes, the metallization was not annealed because ohmic contacts were achieved as deposited. The fact that an ohmic contact was achieved at room temperature is attributed to the high surface concentration and low bandgap energy of Ge, which result in increased tunneling of carriers and thermionic emission.

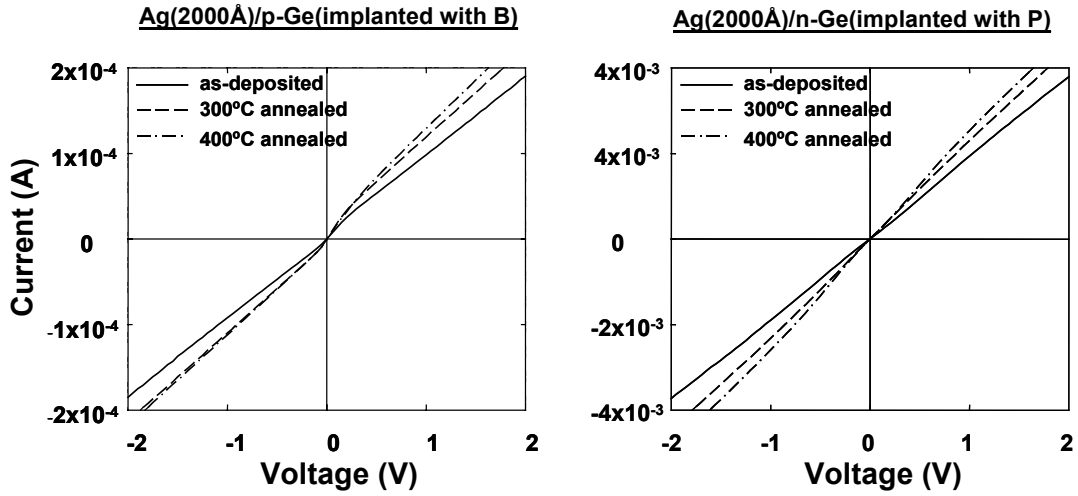


Figure 5.3 Current and voltage characteristics to evaluate Ohmic contact resistivity

5.1.1 Ion Implantation

In the fabrication of interdigitated Ge PIN photodetectors, ion implantation was used to form the p^+- and n^+-electrodes. One of the advantages of Ge technology is low thermal activation energy. Sheet resistivity was measured as a function of the annealing temperatures. The resistivity decreased significantly beginning at the temperature of 400 °C. This temperature is very low compared with Si technology. A low activation temperature is advantageous for the formation of a shallow junction in the scaled devices. In addition, we can minimize the formation of undesirable interfacial oxide, for example, in the gate stack of MOSFETs.

Figure 5.4 shows the sheet resistivity as a function of annealing temperature. Two types of ions were implanted into the Ge wafer, boron and phosphorous. Ion implantation energies and doses are shown in the figure. It is clear that there is a significant decrease in the sheet resistivity at temperatures above 400 °C. The resistivity showed little change as annealing temperature was increased.

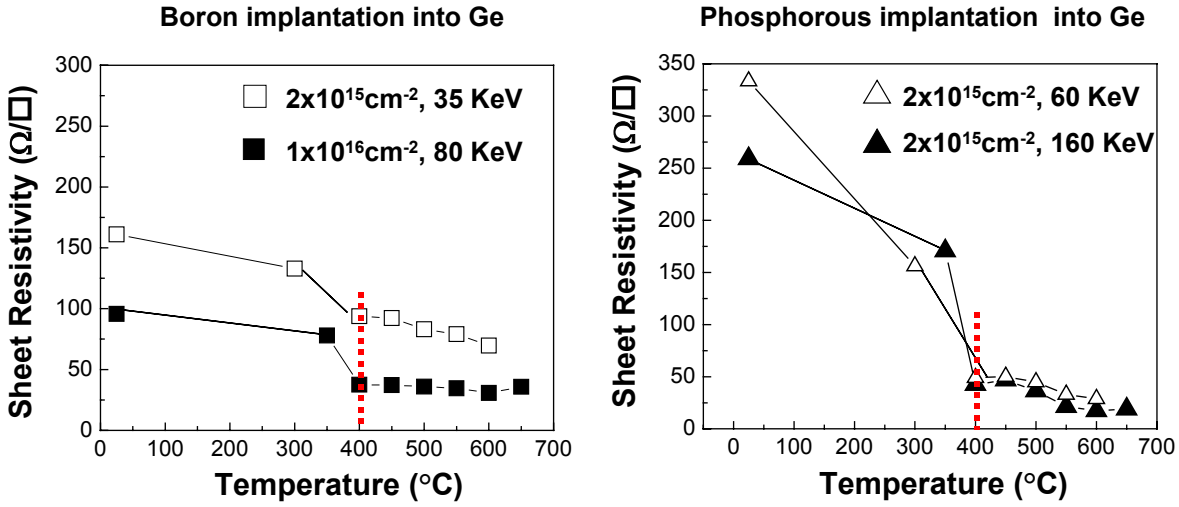


Figure 5.4 Sheet resistivity as a function of annealing temperature for boron and phosphorous implanted Ge as different implantation conditions

The as-implanted resistances were 168 Ω/□ and 326 Ω/□ for boron and phosphorous implants, respectively. To activate the implanted ions, rapid thermal annealing was performed at 450 °C for 1min in N_2 ambient. Sheet resistivity measurements were used to determine an optimum activation temperature. For boron implants, the electrical activation increased slowly with

temperature while phosphorous exhibited a steep increase in conductivity near 400 °C. After annealing at 450 °C, the sheet resistance was 93 Ω/□ and 42 Ω/□ for boron and phosphorous implants, respectively.

5.2 Metal-Germanium-Metal Photodetectors

The metal-semiconductor-metal photodiode (MSMs) structure has been widely used owing to its relative ease of fabrication and low capacitance. For long wavelength operation, MSMs have shown relatively high dark current since the Schottky barrier height scales with band gap energy. Germanium is a narrow band gap material with indirect and direct band gap energies of 0.67 eV and 0.81 eV, respectively. Low dark current is essential for the photodiodes to have high signal to noise ratio. To enhance the Schottky barrier height, we introduced higher bandgap amorphous Ge layers between the Schottky contact and the Ge epitaxial layer.

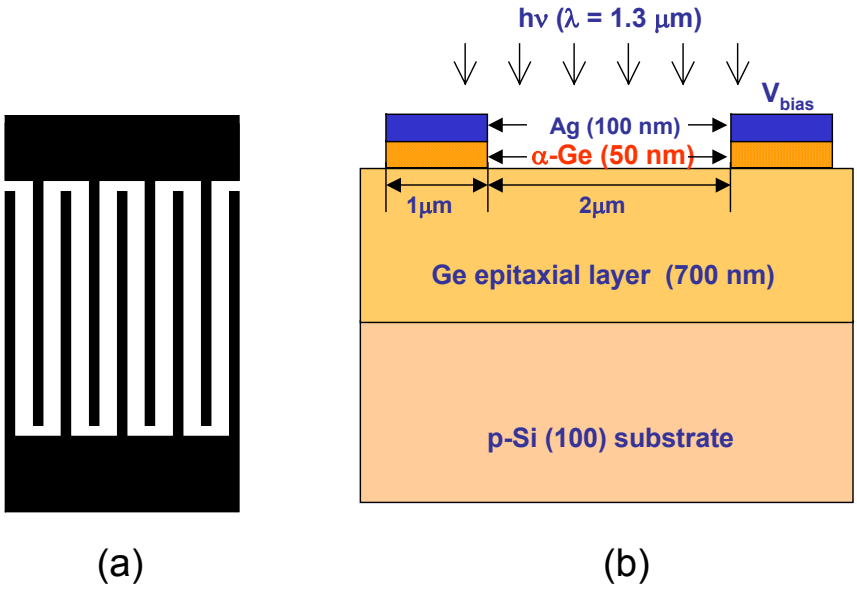


Figure 5.5 Metal-Ge-Metal photodetector with amorphous Ge interfacial layer (a) Top view (b) Cross-sectional view

The metal-Ge-metal photodetector was fabricated on 700 nm-thick epitaxial Ge layers directly grown on Si substrate. Figure 5.5 shows schematic top and cross-sectional views of MSMs with an amorphous Ge layer between the Ag Schottky contact and the Ge epitaxial layer. A SiO_2 layer (1000 Å) was deposited using plasma enhanced chemical vapor deposition (PECVD) to isolate the metal pads from the Ge epitaxial layer. Then, interdigitated fingers were patterned in the active area and SiO_2 was removed. The α-Ge (500 Å) was electron-beam evaporated and followed by Ag (1000 Å) deposition at a base pressure of 2×10^{-6} Torr. The substrate was held at room temperature during electron-beam evaporation to prevent solid-phase epitaxy, and the Ge layer remained amorphous. Finally, a lift-off process was performed. Prior to evaporation, native oxide was removed using dilute HF solution and a de-ionizing rinse.

5.3 Summary

In this chapter the photodetector fabrication has been described. In the fabrication of interdigitated planar p-i-n photodiode, ion implantations were used for the formation of p-i-n junctions. To activate the implanted ions, RTA was performed for 1 min in N_2 ambient. Sheet resistivity measurement showed low thermal activation energy, where we found a significant decrease in the sheet resistivity at temperature above 400 ^{o}C. Following the activation

annealing, a SiO_2 layer was deposited using PECVD for passivation, and this layer also served as an anti-reflection coating. In the fabrication of MSM photodetectors, amorphous Ge interfacial layer was used to increase the hole barrier height between Ag Schottky contact and Ge epitaxial layer. Due to the stretched separation between the mobility edges in amorphous Ge, the dark current decreased by more than two orders of magnitude.

Chapter 6

Measurement Results

6.1 Photodetector Measurements

This chapter presents the measurement results obtained in characterizing the performance of Ge PIN and metal-Ge-metal photodetectors. The performance of Ge photodetectors was characterized in terms of the dark current, quantum efficiency, and 3-dB bandwidth. In this Chapter, I present three types of Ge photodetectors that are differentiated by their structure: (1) interdigitated bulk Ge PIN photodetectors, (2) interdigitated Ge PIN photodetectors fabricated on Ge-on-Si using a thick SiGe buffer, and (3) metal-germanium-metal photodetectors fabricated on Ge epitaxial layers directly grown on Si substrates.

6.1.1 Current-Voltage Characteristics

Usually, photodetectors are operated in reverse bias. A small generation current flows without light incident, which is commonly called the dark current or reverse-bias leakage current. This background leakage current contributes to noise in the output electrical signal. The magnitude of this generation current depends on the rate of generation of electron and hole pairs. Once carriers

(electron and hole pairs) are created, a current will flow until they are collected or recombined. This generation current can be increased greatly by optical excitation of e-h pairs. On the other hand, surface recombination current and deep traps within the semiconductors cause the photo-generated current to recombine before reaching the electrodes. [6-1,2]

In this work, the current-voltage characteristics of the photodetectors were measured using an HP 4145B semiconductor parameter analyzer. The dark current and breakdown voltage were measured by applying sufficiently high electric field to the photodiodes. Figure 6.1 shows a typical I-V characteristic of the Ge interdigitated PIN photodiodes having different finger spacings. The leakage current (log scale) measured at the reverse bias condition is shown at lower row. The breakdown voltages vary according to the finger spacings. The breakdown voltages were reached at larger reverse voltages (V_R) as the result of increasing the finger spacing (S). An approximated expression for the electric field (E) is $E = V_R / S$. When the field approaches 10^4 V/cm in Ge, the electron and hole velocities saturate at 6 x 10^6 cm/s and a significant current begins to flow by means of the band-to-band tunneling process [6-1].

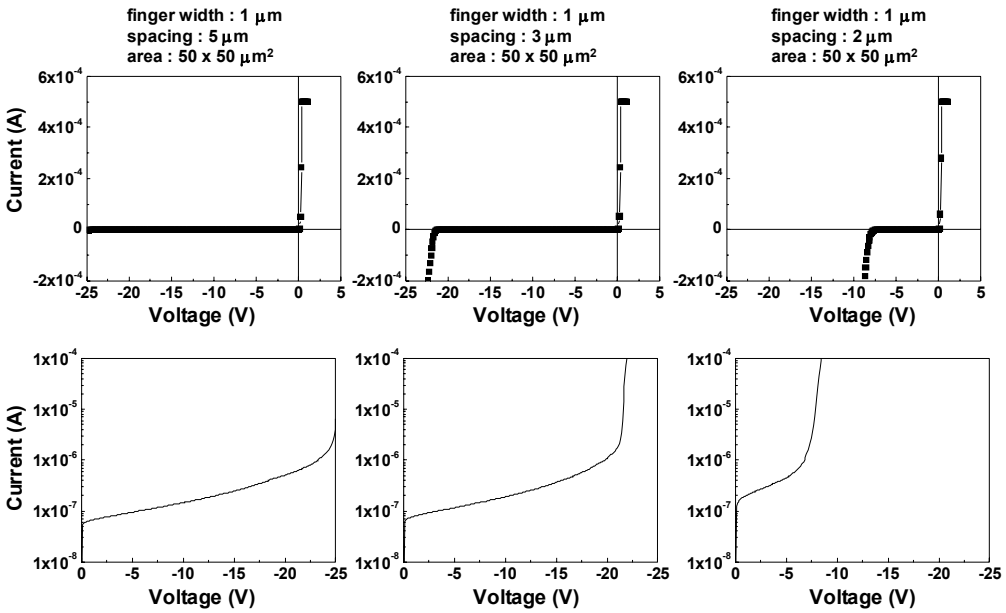


Figure 6.1 Typical I-V characteristics of Ge interdigitated PIN photodetectors with different finger spacing

6.1.2 Quantum Efficiency

The quantum efficiency for photodiodes is a measure of how many e-h pairs are created per incident photon and then collected by the electrodes to the external circuit. Quantum efficiency here is measured in terms of percentages (less than 100% without gain). Internal quantum efficiency (η_{int}) relates the photocurrent to the number of absorbed photons being collected by the contacts, whereas external quantum efficiency (η_{ext}) compares the number of incident photons to the collected photocurrent. The external quantum efficiency includes the effects of surface reflections. The external quantum efficiency is defined as

$$\eta_{ext} = \frac{I_{ph}/q}{P_o/h\nu} = (1-R)(1-e^{-\alpha d}) \qquad (6.1.1)$$

In this equation, I_{ph} is the measured photocurrent, P_o is the incident optical power, R is the reflectance, α is the absorption coefficient, and d is the thickness of the absorbing region.

Internal quantum efficiency generally exceeds 90%. However, without a proper anti-reflection (AR) coating of the photodetector surface, approximately 30% (Si and GaAs) and 39% (Ge) of the incident light is reflected off the semiconductor surface due to differences in indices of refraction of the semiconductor and air. This limits the external quantum efficiency to less than 70% [6-2].

Figure 6.2 shows a simulated reflectance as a function of wavelength. At 1.3 μm, the reflection loss between air and Ge is about 39% without anti-reflecting coating. This can be reduced to 12% by using a SiO_2 anti-reflecting coating (224 nm).

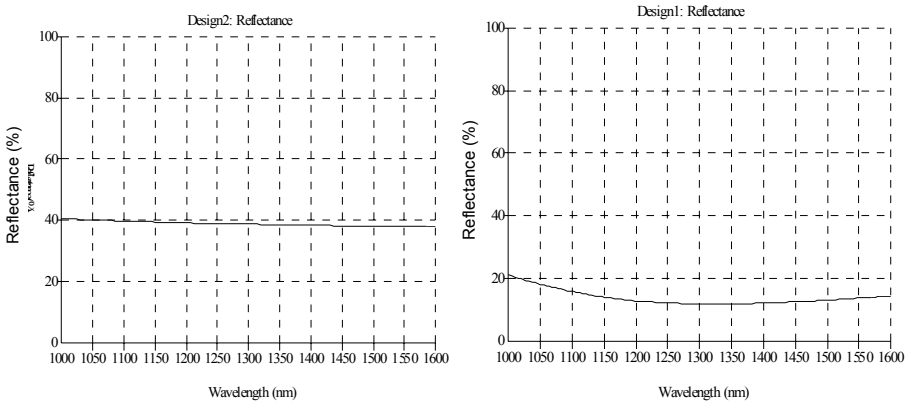


Figure 6.2 Simulated reflectance as a function of wavelength (a) without AR coating (b) with SiO_2 (224 nm) AR coating

In this work, the external quantum efficiency was measured using a tunable monochromatic light source (Spex 500M Grating Spectrometer), a lock-in amplifier (Stanford Research model 510), and a calibrated Ge photodetector. A tungsten-halogen lamp filtered by a grating spectrometer provided a tunable optical input. The optical input was transmitted through a chopper to introduce a frequency-dependence to the signal and then focused onto the photodiode using a microscope objective. The electrical output of the device was measured using a lock-in amplifier tuned to the frequency of the chopper. The entire measurement process was then repeated with a calibrated photodiode. A schematic of the experimental setup that was used to measure the photodiode efficiency is depicted in Figure 6.3.

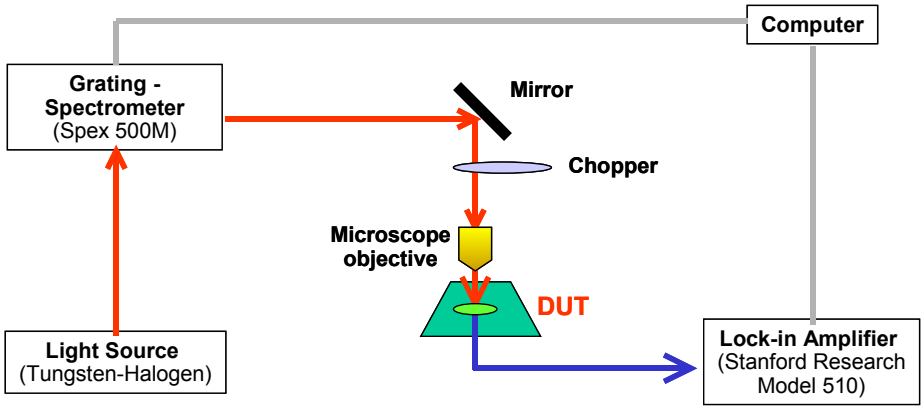


Figure 6.3 Experimental apparatus used to measure photodiode quantum efficiency, DUT (Device Under Test)

The quantum efficiency of the photodetector under test was determined by comparing its photocurrent with the photocurrent of the calibrated photodetector at each incident wavelength, according to the following relationship [6-3]:

$$\eta_{ext}^{test} = \eta_{ext}^{calibrated} \cdot \frac{I_{ph}^{test}}{I_{ph}^{calibrated}} \qquad (6.1.2)$$

In this expression, $\eta_{ext}^{calibrated}$ is the known external quantum efficiency of the calibrated photodiode, and I_{ph}^{test} and $I_{ph}^{calibrated}$ are the measured photocurrents of the photodiode being tested and the calibrated photodiode, respectively. The incident light was focused to a spot whose area was smaller than the active area of the photodiode.

6.1.3 Bandwidth

The 3-dB bandwidth of a photodetector is a measure of how fast the photodetector can respond to a series of light pulses. The 3-dB bandwidth is found by measuring the ratio of output electrical modulation current to input optical modulation power of a device. When plotted, a flat region should occur at low frequencies, indicating a stable response. However, as the frequency increases, the photodetector response degrades. It cannot respond to the signal as quickly as the light beam is modulated. As a result, the response photocurrent falls. When the response falls to 3-dB below the flat region, 50% of the power is lost. The frequency at this point is referred to as the 3-dB frequency or the bandwidth of the device under test [6-2].

There are two time constants, that limit the speed of a photodiode. One is the transit time. This is simply the time a carrier, created by a photon, takes to travel through the active region and get collected by the contacts. Photons are absorbed in the semiconductor by raising the potential energy of an electron from the valence band to the conduction band. The missing electron in the valence band is transported very much like a positive particle and is referred to as a "hole". Electrons and holes can have different mobilities, and the disparity can be ten-fold or more for direct band gap semiconductors, like GaAs, which collects and emits photons more efficiently than indirect semiconductors, such

as Si and Ge. Thus, holes take longer to traverse the photodiode active region than electrons, and therefore can limit the photodiode speed [6-2].

$$t_{tr} = d / v_{sat} \qquad (6.1.3)$$

$$f_{3dB} = \frac{\Gamma_d}{2\pi \cdot t_r} \qquad (6.1.4)$$

where t_{tr} is the transit time, v_{sat} is the saturated carrier velocity, and d is the distance the carriers travel.

The RC time constant is the other limiting factor. The product of the photodiode junction capacitance (C_j) and the equivalent resistance in parallel with C_j (usually 50 Ω governed by the measuring instrument and cabling) yields the RC time constant, measured in seconds.

$$C_j = \frac{\varepsilon_s \varepsilon_o \cdot A}{d} \qquad (6.1.5)$$

where ε_s is the permitivity of the semiconductor in an intrinsic layer, ε_o is the permitivity of free space (8.854 x 10^{-14} F/cm), A is the photodiode area, and d is the photodiode absorption layer thickness.

In this work, the frequency response of Ge photodetectors was determined using an HP 8703A Lightwave Component Analyzer (LCA). The LCA provided a combination of calibrated 20 GHz lightwave and microwave measurement capabilities, which performed the optical, electrical, and electro-optical measurements. The bandwidth was measured in the frequency domain.

The optical source in the LCA is a 1.3 μm distributed feedback laser with a typical spectral width of less than 50 MHz and a peak-to-peak modulated optical output power of 130 μW. The frequency of modulation was swept over a bandwidth range of 130 MHz ~ 10 GHz and the photodetectors were biased on-wafer using microwave probes. Figure 6.4 shows the experimental setup used to measure the frequency response of the photodiodes in the frequency domain using Lightwave Component Analyzer.

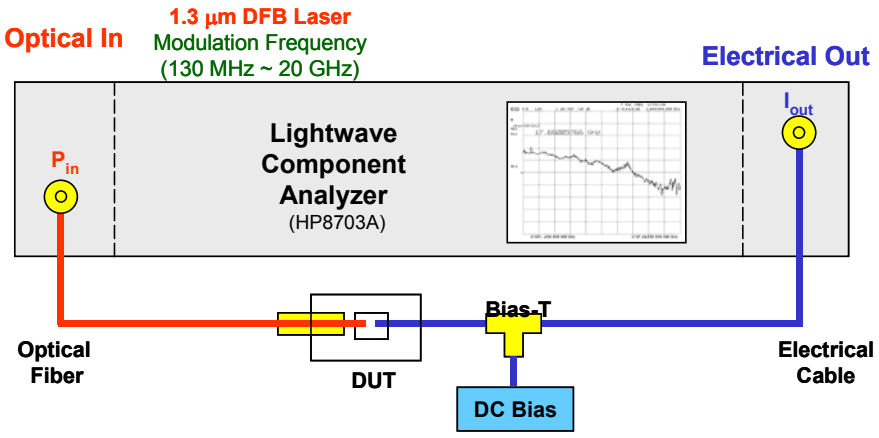


Figure 6.4 Experimental setup used to measure the frequency response of the photodiodes in the frequency domain

The measurement consists of the ratio of output electrical modulation current to input optical modulation power. Slope responsivity describes how a change in optical power produces a change in electrical current. Graphically, this is shown in Figure 6.5. The LCA measures the input optical modulation

power and output modulation current and displays the ratio of the two in Amps/Watt.

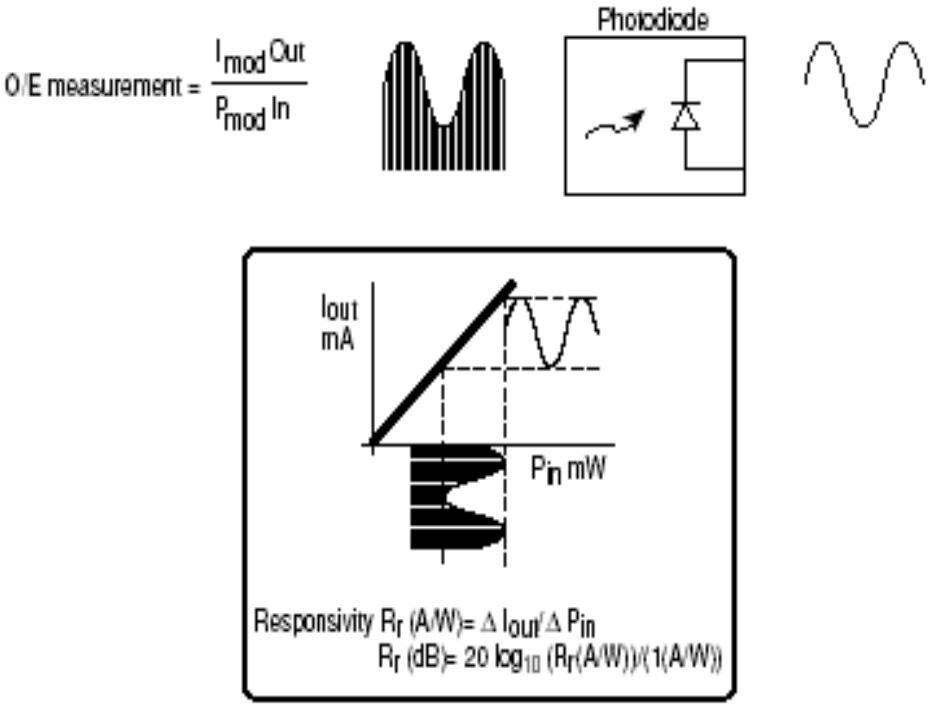


Figure 6.5 Measurement consists of the ratio of output electrical modulation current to input optical modulation power

6.2 Bulk Ge Photodetectors

A high-speed PIN photodetector was fabricated on n-type bulk Ge substrate with a resistivity of 1-5 Ω-cm. Planar interdigitated p^+- and n^+-fingers were formed by ion implantation. This section reports on the dark current, the quantum efficiency, and the bandwidth of the photodetector having 1 μm finger width and 2 μm spacing with a 50 x 50 μm^2 active area. The external quantum efficiency was measured in the spectral range of 1.0 μm to 1.5 μm, without external bias. The frequency response was measured at reverse bias levels of 5 V, 10 V, and 15 V at a wavelength of 1.3 μm using a lightwave component analyzer.

6.2.1 DC Measurements

The I-V characteristics of photodetectors with 1 μm finger width and 2 μm spacing and 50 x 50 μm^2 active area are shown in Figure 6.6. Dark currents of 0.9 μA and 10 μA were observed at room temperature at biases of –5 V and –15 V, respectively. The relatively high dark current was due primarily to the low bandgap energy, the high surface field in this structure, and the absence of a good passivation material for Ge. For the interdigitated structure described in this work, the electric field intensity at the surface was very high. Ge surfaces,

however, were not effectively passivated with Ge oxides. In fact, the unstable Ge oxides could induce point defects at the surface. These surface states acted as recombination and generation centers of carriers, leading to surface leakage current. The breakdown voltage of devices was near 17 V.

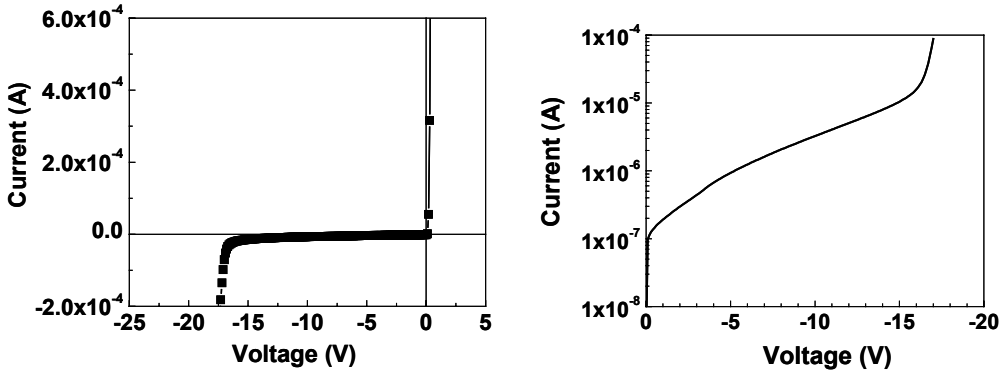


Figure 6.6 Measured I-V characteristics and the dark current in reverse bias of a photodetector having 1 μm finger width and 2 μm spacing and 50 x 50 μm^2 active area

6.2.2 Photodiode Quantum efficiency

Figure 6.7 shows the external quantum efficiency of a photodetector with 1 μm finger width and 2 μm spacing and 50 x 50 μm^2 active area. The external quantum efficiency was > 60 % in the wavelength range 1.0 μm < λ < 1.5 μm. At a wavelength of 1.3 μm, the external quantum efficiency was 67 % (responsivity = 0.7 A/W). The decrease in the quantum efficiency for wavelengths ≥ 1.55 μm resulted from a lower absorption coefficient. Since

interdigitated p^+- and n^+-fingers were formed using ion implantation with much smaller junction depth than the absorption depth, there was no effective contact shadowing, which can reduce the efficiency of MSMs. A further increase of the quantum efficiency is expected by incorporating an anti-reflecting coating. In this work, the reflection loss for the photodiode passivated with SiO_2 (1000 Å) was calculated to be 29 % at the wavelength of 1.3 μm.

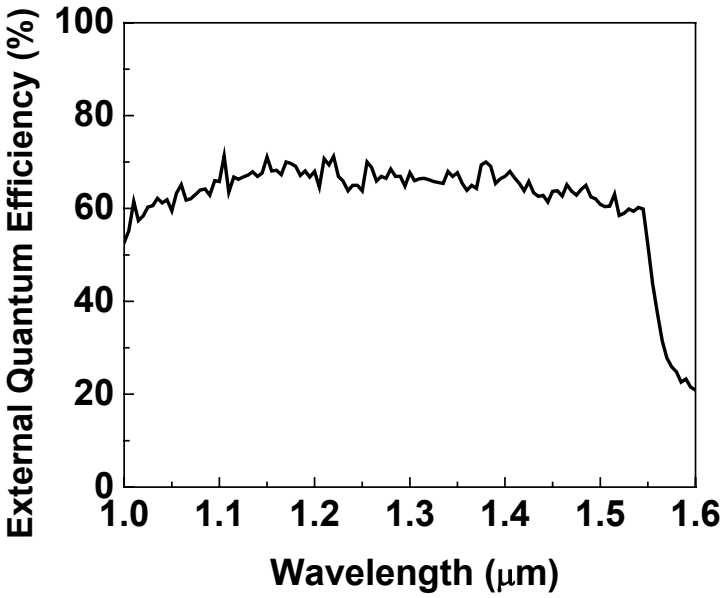


Figure 6.7 Measured photodiode external quantum efficiency versus wavelength in the spectral range of 1.0 μm to 1.5 μm with no external bias

6.2.3 Photodiode Frequency Response

The frequency response of a photodetector with 1 μm finger width and 2 μm finger spacing and 50 x 50 μm^2 active area is shown in Figure 6.8 at three bias levels. At a reverse bias of 5 V, the 3 dB bandwidth was found to be 1.8 GHz. At biases –10 V and –15 V, the bandwidths increased to 2.6 GHz and 3 GHz, respectively. It is anticipated that narrowing the spacing between fingers to reduce the transit time can further increase the bandwidth, however, it should be noted that the capacitance increases rapidly as the finger spacing is reduced. Owing to the high absorption coefficient of Ge, the frequency responses of the photodetectors were flat and did not exhibit a low-frequency tail, which can be caused by slow transport of carriers generated in low-field regions. At $\lambda \sim 1.3$ μm, the absorption depth was about 1.0 μm, which was less than the depletion width.

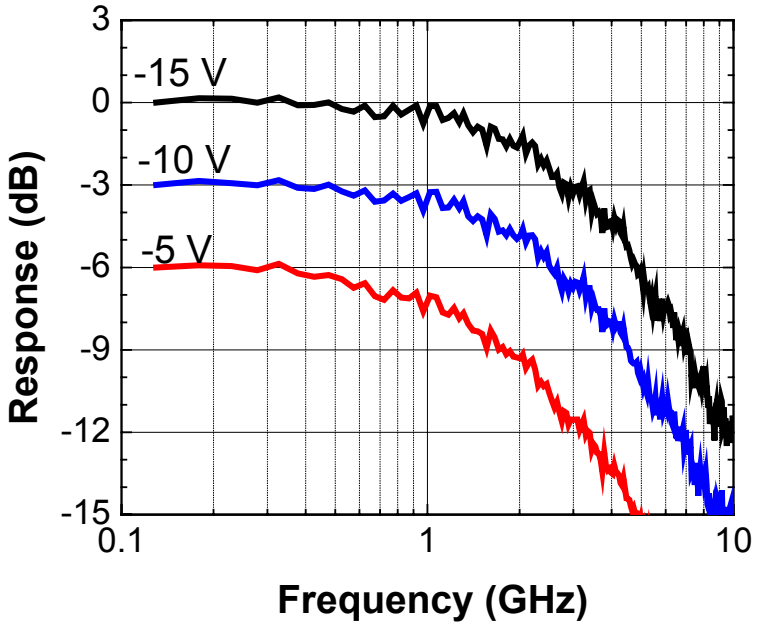


Figure 6.8 Measured frequency response of a 1 μm x 2 μm device with a 50 x 50 μm^2 active area at reverse bias of 5 V, 10 V, and 15 V. The curves have been shifted vertically with respect to each other for clarity

Figure 6.9 shows the frequency response of a photodetector having 1 μm finger width and 5 μm spacing and a 50 x 50 μm^2 active area. This photodetector had wider finger spacing compared to the photodetector presented above. The bandwidths were measured at different bias voltages. The 3-dB bandwidths were measured to be 800 MHz, 1 GHz, and 2 GHz at -5 V, -10 V, and -15 V, respectively. At higher voltages of -24 V and -30 V, the 3-dB

bandwidths were 3.2 GHz and 3.3 GHz, respectively. Compared to the photodetectors with narrower finger spacing of 2 μm, the frequency response degraded faster at the same bias voltage, which resulted in a lower 3-dB bandwidth. The longer the distance and the greater the time the photo-generated carriers had to travel, the lower the 3-dB bandwidths. What this indicated was that the bandwidth of this photodetector was limited by the transit time.

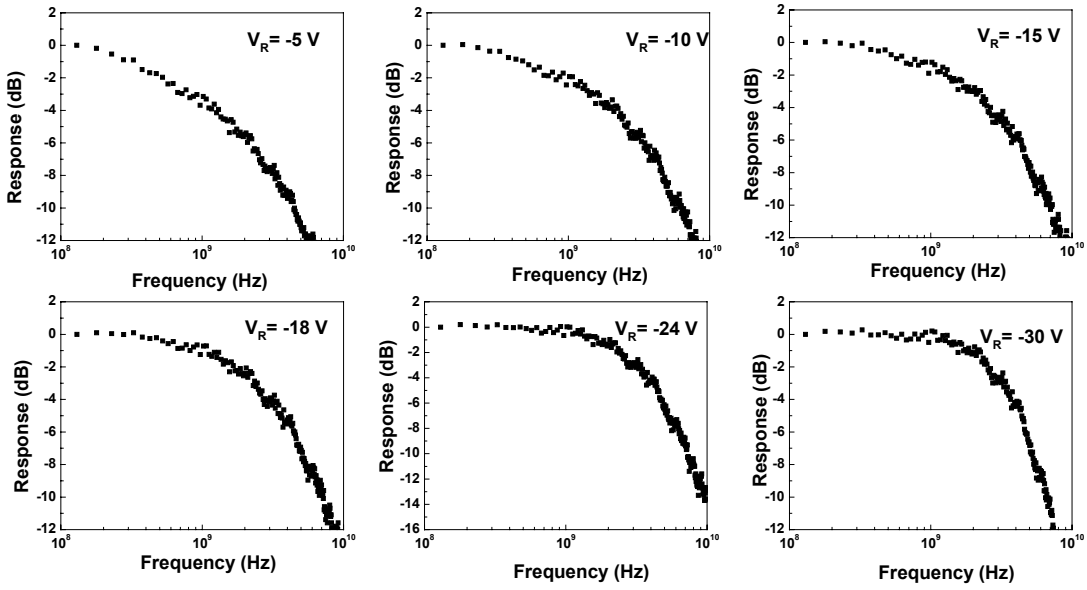


Figure 6.9 Measured frequency response of a photodetector having wider finger spacing of 5 μm, 1 μm finger width, and a 50 x 50 μm^2 active area at reverse biases of 5, 10, 15, 18, 24, and 30 V. The curves have been normalized for clarity.

6.3 Ge-on-Si Photodetectors with SiGe Buffer

Interdigitated PIN photodetectors were fabricated on a 1 μm-thick Ge epitaxial layer grown on Si substrate using a 10 μm-thick graded SiGe buffer layer. The Ge epitaxial layer had a threading dislocation density of 10^5 cm^{-2} and rms surface roughness of 3.28 nm. The 3-dB bandwidth and the external quantum efficiency were measured on a photodetector having a 1 μm finger width and 2 μm spacing with a 25 x 28 μm^2 active area.

6.3.1 DC Measurement

The dark current of photodetectors with 1 μm finger width, 2 μm spacing, and 25 x 28 μm^2 active area is shown in Figure 6.10. Dark currents of 3.2 μA and 5.0 μA were observed at biases of –3 V and –5 V, respectively. Those values were about 5 times greater than those obtained in interdigitated bulk Ge PINs [6-4]. This might be due to the fact that the epitaxial Ge layer has a higher defect density than the bulk Ge substrate. In comparison with previously reported mesa PINs [6-5]-[6-8] on epitaxial Ge layers grown on Si substrates, our interdigitated PINs had relatively high dark currents. The epitaxial Ge layers used in this work, however, showed the lowest threading dislocation density among those devices.

What this suggests is that one of the possible causes is related to the high surface field in the interdigitated structure and the absence of a good passivation material for Ge. For the interdigitated structure described in this work, the electric field intensity was highest near the surface. Ge surfaces, however, are not effectively passivated with Ge oxides. In fact, the unstable Ge oxides can induce point defects at the surface.

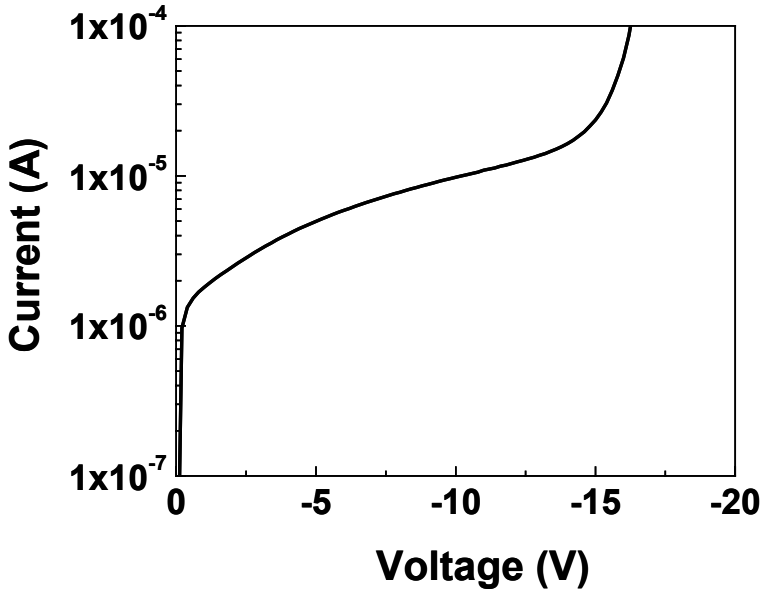


Figure 6.10 Measured dark current of photodiodes with 1 μm finger width, 2 μm spacing, and a 25 x 28 μm^2 active area

6.3.2 Photodiode Quantum Efficiency

Figure 6.11 shows the measured quantum efficiency versus wavelength with no external bias. The incident light was focused to a spot whose area was smaller than the active area of the photodiode. At a wavelength of 1.3 μm, the quantum efficiency was 49 % (responsivity = 0.51 A/W). For increasing wavelength the absorption coefficient decreased, which resulted in reduced quantum efficiency. Since interdigitated p^+- and n^+-fingers were formed using ion implantation with much smaller junction depth than the absorption depth, and since the p^+- and n^+-fingers do not have metal contacts on the top in the active region, there was no effective contact shadowing.

The reflection loss for the photodiode passivated with SiO_2 (1000 Å) was calculated to be 29 % at the wavelength of 1.3 μm. Higher quantum efficiencies, particularly at longer wavelengths could be achieved by using an improved anti-reflecting coating of SiO_2 (2250 Å), which would reduce the reflectance to 13 %, and by increasing the thickness of the Ge layer.

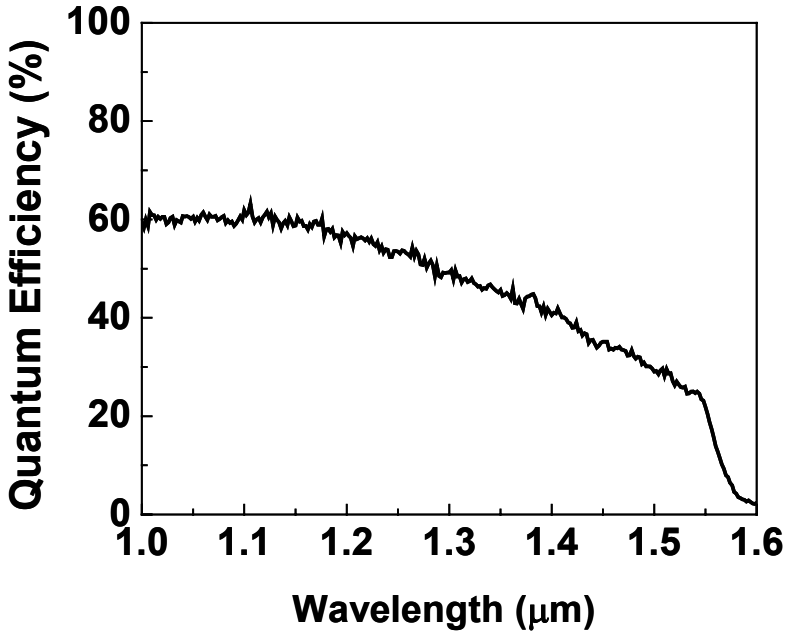


Figure. 6.11 Measured external quantum efficiency versus wavelength with no external bias

6.3.3 Photodiode Frequency Response

The photodiode frequency response, measured in the frequency domain using a 1.3 μm DFB laser at three bias levels, is shown in Figure 6.12. At a reverse bias of 1 V, the 3-dB bandwidth was found to be 2.2 GHz. At reverse biases of 3 V and 5 V, the 3-dB bandwidths increased to 3.5 GHz and 3.8 GHz, respectively. The fact that these photodetectors operate at low bias voltages is attractive for integration with Si ICs. In comparison to the Ge PINs that were

fabricated on bulk Ge substrates [6-4], the Ge PINs on Si substrate showed higher 3-dB bandwidths at lower biases.

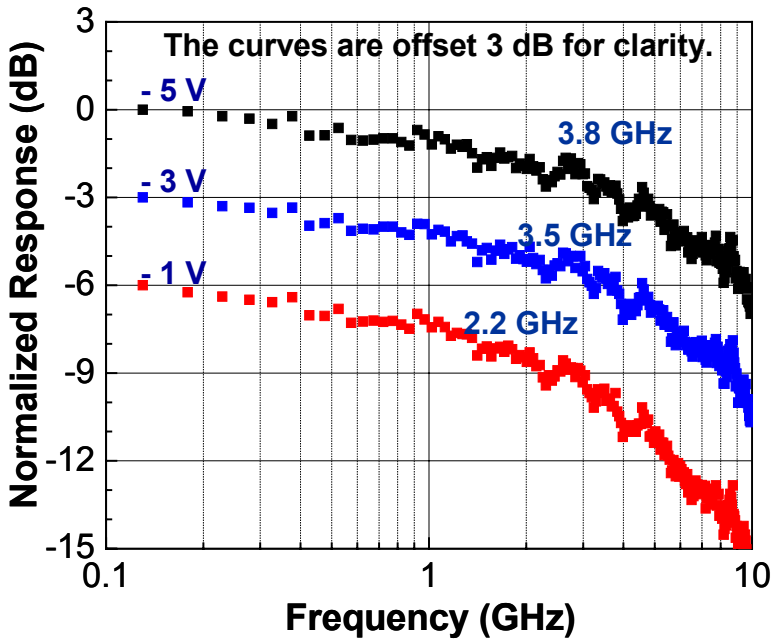


Figure 6.12 Frequency response of 1 μm x 2 μm (finger width x finger spacing) device with a 25 x 28 μm^2 active area at reverse biases of 1 V, 3 V, and 5 V. The curves have been shifted vertically with respect to each other for clarity.

The 3-dB bandwidth and the external quantum efficiency were highest among Ge photodetectors on Si substrate reported for operation at a wavelength of 1.3 μm. A comparison with previously reported results is summarized in Table I.

TABLE I. Previously reported Ge photodiodes fabricated on Si substrate for operation at a wavelength of 1.3 μm

Device	External quantum efficiency (Resposivity)	3dB bandwidth / Response time	Reference
MSMs	23 % (240 mA/W) at -1V	2 ns at -3V	4
Mesa PINs	12.6 % (133 mA/W) no external bias	$(2\pi R_L C_J)^{-1}$ = 2.35 GHz at -3V*	7
Mesa PINs	53 % (550 mA/W) at -1V	850 ps at -4V	6
Interdigitated PINs	49 % (510 mA/W) no external bias	3.5 GHz at -3 V	This work

* The theoretical bandwidth obtained using R_L (100 Ω) and C_J (0.676pF).

Figure 6.13 schematically illustrates the absorption (penetration) depth in bulk Ge and Ge-on-Si photodetectors when illuminated at a wavelength of 1.3 μm. In the bulk Ge photodetectors, incident photons are absorbed as light travels in the bulk Ge and the intensity decays exponentially with distance. Most of the photon absorption (63%) occurs over a distance of $1/\alpha$ (~ 1 μm) and the rest of the absorption takes place below $1/\alpha$ in the bulk Ge, where the electric field is relatively weak.

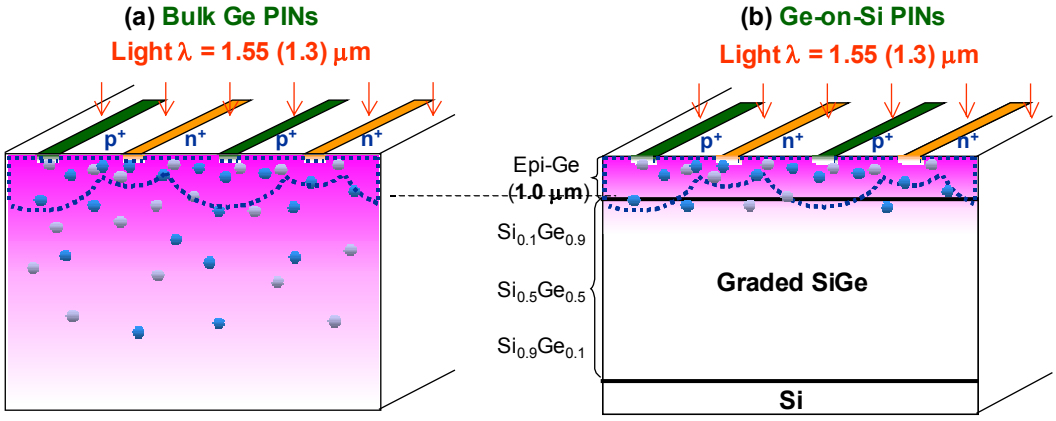


Figure 6.13 Schematic diagrams showing an absorption (penetration) depth at 1.3 μm in (a) bulk Ge PINs, (b) Ge-on-Si PINs

The absorption depth of the Ge-on-Si photodetectors, as shown in Figure 6.13, occurs in both the Ge layer and the SiGe graded buffer layer. With the greater depth of the SiGe buffer layer, the bandgap energy of SiGe increases and the absorption coefficient significantly decreases. One impact of this effect is the reduction in quantum efficiency at longer wavelengths as shown in Section 6.3.2. Additionally, as compared to bulk Ge photodetectors, there is a reduction in generated carriers in the low-field regions and, hence, a reduction in slowly transported carriers. This process offers a better control over the generated electron-hole pairs by confining these carriers in the strong electric field, which, in turn, enhances the carrier drift velocity and results in a higher bandwidth.

6.3.4 Frequency Response at 1.55 μm

The frequency responses of photodiodes were also measured at the wavelength of 1.55 μm. Figures 6.14 shows the frequency responses of the bulk Ge PINs and the Ge-on-Si PINs measured at 1.55 μm. As these figures demonstrate, the 3-dB bandwidth of bulk Ge PINs was as low as 800 MHz at –5 V. On the other hand, the 3-dB bandwidths of Ge-on-Si PINs were measured to be 2.4 GHz, 3.5 GHz, and 4 GHz at –1 V, -3 V, and –5 V, respectively. Photodetectors fabricated using Ge-on-Si substrates showed much higher frequency responses compared to the bulk Ge PINs when measured at 1.55 μm.

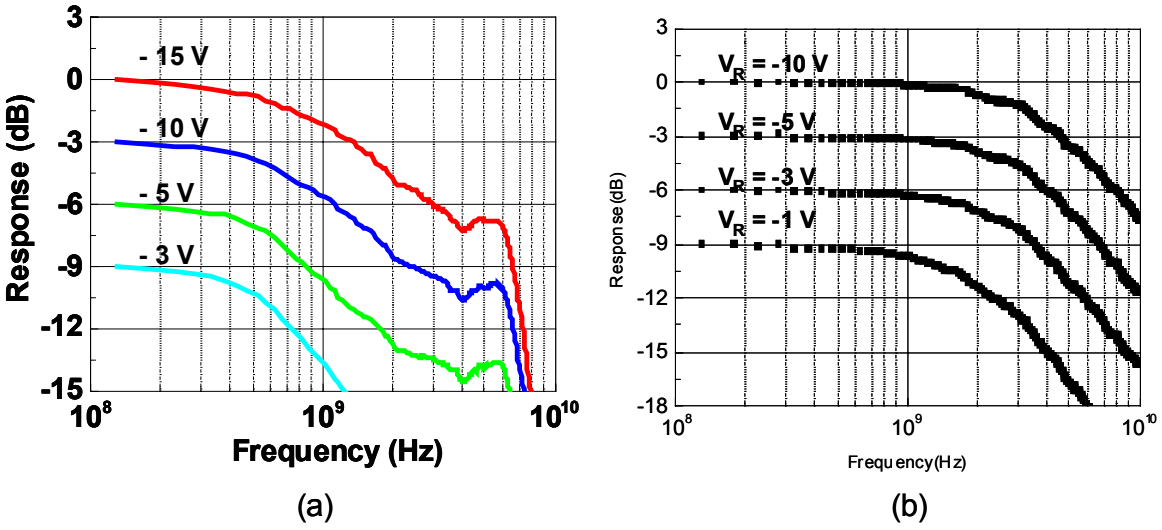


Figure 6.14 Frequency responses of (a) bulk Ge PIN photodiodes and (b) Ge-on-Si PIN photodiodes measured at 1.55 μm as a function of bias voltage

Figures 6.15 (a) and (b) schematically show photon absorption in the bulk Ge PINs and Ge-on-Si PINs, respectively. At the wavelength of 1.55 μm, the absorption coefficient of light within the Ge decreases dramatically. As the absorption coefficient decreases, more light is absorbed uniformly throughout the active region down to the substrate instead of close to the upper surface of the Ge. Charge carriers that are photogenerated at the deep substrate are swept under a relatively low electric field. As the effective absorption region becomes thicker, more photons are absorbed, which increases the quantum efficiency. However, this effect also slows down the transit time, thus lowering the bandwidth.

On the other hand, the absorption region in Ge-on-Si PINs at 1.55 μm is not as deep as in bulk Ge PINs. In Ge-on-Si PINs, the absorption diminishes significantly as light travels down to the SiGe buffer. This occurs because the photon at 1.5 μm does not have enough energy to move an electron from the valence band to the conduction band in the SiGe buffer as the Ge concentration increases. This results in photo-generated carriers being produced closer to the high electric field upper surface of the semiconductor, thus leading to high bandwidths at 1.55 μm in Ge-on-Si PINs.

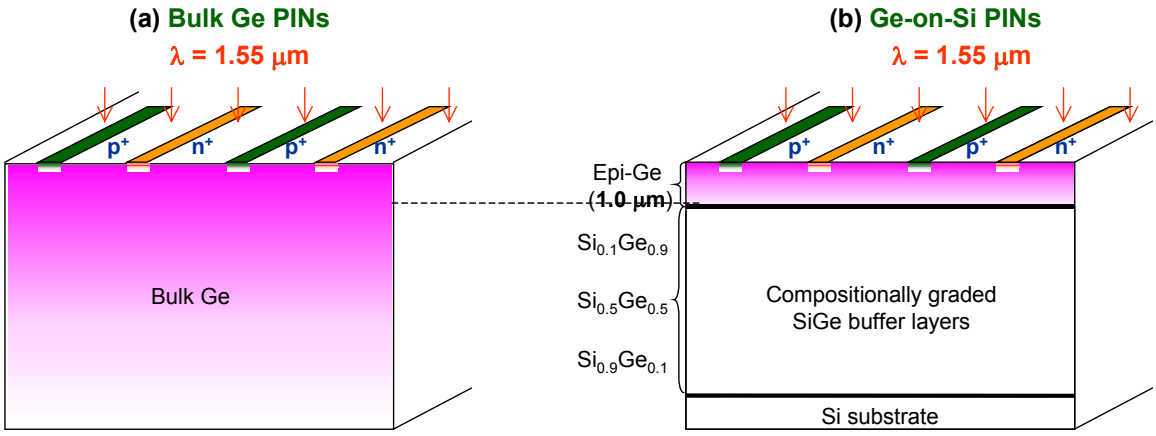


Figure 6.15 Schematic diagrams showing a photon absorption at 1.55 μm in (a) the bulk Ge PINs, (b) Ge-on-Si PINs

6.4 MSMs with Amorphous Ge Schottky Barrier Enhancement Layers

Figure 6.16 shows the energy band diagram of metal-Ge contacts. In an ideal situation when a metal comes into contact with a semiconductor, the hole barrier height is determined by bandgap energy, electron affinity, and metal work function. For example, the ideal hole barrier height of silver-germanium contacts is 0.54 eV.

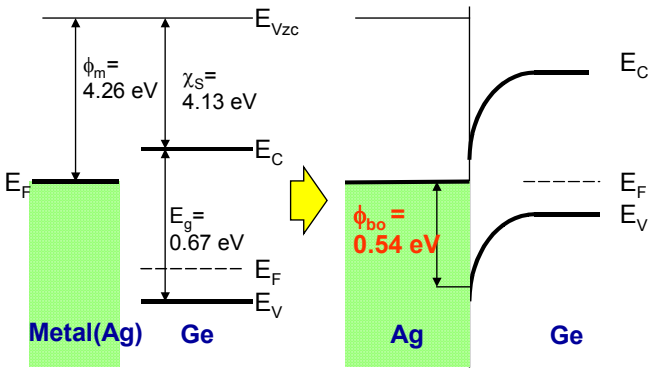


Figure 6.16 Energy band diagram of ideal metal-Germanium contacts

However, in most practical contacts, the ideal condition is never reached because of the effect of surface states. Thus, the barrier height becomes less or almost independent of the metal work function and the Fermi-level tends to be pinned. Figure 6.17 shows an energy band diagram of silver-germanium contacts. According to some reports, the Fermi-level is pinned at 0.54 ~ 0.61 eV

below the conduction band edge [6-9]. This results in the Schottky barrier height as low as 0.09 eV on p-type Ge, which is very low compared with the ideal barrier height of 0.54 eV.

In Chapter 5, the epitaxial Ge layers grown directly on Si substrates were found to be highly conductive p-type with an acceptor concentration of 10^{17} cm^{-3}. This background doping was due to the structural defects. The fact that the epitaxial layers are p-type with the Fermi level pinned slightly above the valence band edge indicates that Ge MSMs will be very leaky because of the low hole barrier and a high thermionic current flow. [6-10,11]

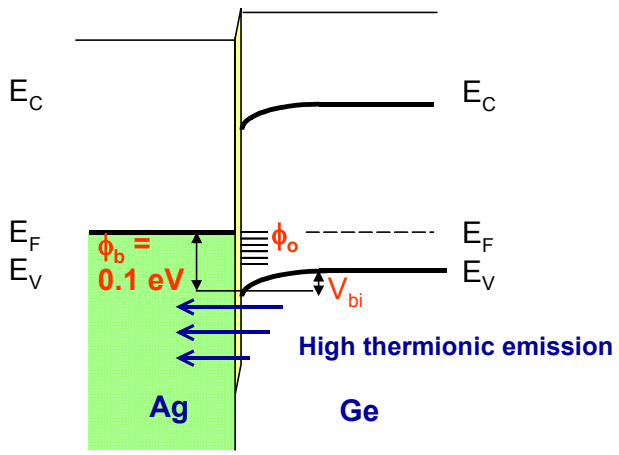


Figure 6.17 Energy band diagram of metal-germanium contacts

In this work, amorphous Ge was used to increase the Schottky barrier height, which was very low due to the small band-gap energy of Ge and Fermi

level pinning independent of the contacting metallization. Figure 6.18 shows an energy band diagram of silver-germanium contacts with amorphous Ge interfacial layers being introduced between the silver and the Ge epitaxial layer.

The separation between the mobility edges in amorphous Ge is assumed to be higher than the band gap energy of crystalline Ge. The mobility edges in amorphous material plays a role equivalent to the band-gap energy in crystalline semiconductors. The separation between the mobility edges in hydrogenated amorphous Si (α-Si:H) was reported to be 1.7 eV [6-12], which is higher than the band gap energy of crystalline Si (1.11 eV).

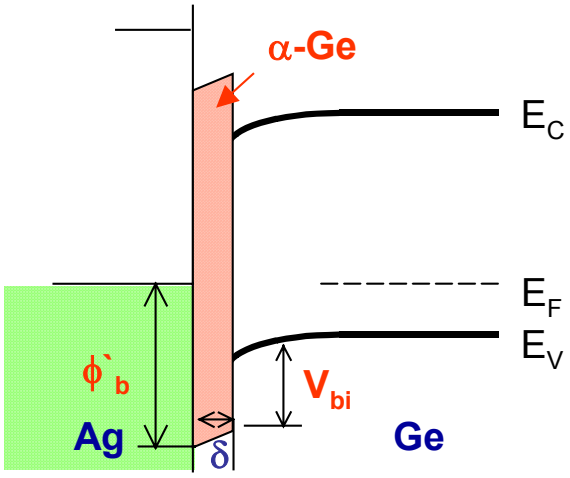


Figure 6.18 Energy band diagram of metal-Germanium contacts with amorphous Ge Schottky barrier height enhancement layers

6.4.1 DC Measurements

The I-V characteristics of metal-Ge-metal photodetectors with 1 μm finger width and 2 μm spacing and 25 x 50 μm^2 active area are shown in Figure 6.19. The increase in the barrier height affected by incorporating amorphous Ge resulted in a reduction of the dark current by more than two orders of magnitude to 7.5 μA at 3 V. The effectiveness of α-Ge at reducing the dark current is believed to be due to the enhanced barrier height by increasing the separation between the mobility edges in α-Ge. However, the dark current of these MSMs was relatively high compared other semiconductor photodetectors. This is due primarily to the high surface field in the MSM structure and the absence of effective surface passivation. Due to the high optical absorption coefficient of Ge at a wavelength of 1.3 μm, more light was absorbed closer to the upper surface of Ge, instead of being uniformly distributed throughout the substrate. This effect might have caused a high dark current since recombination currents were more prevalent at the surface.

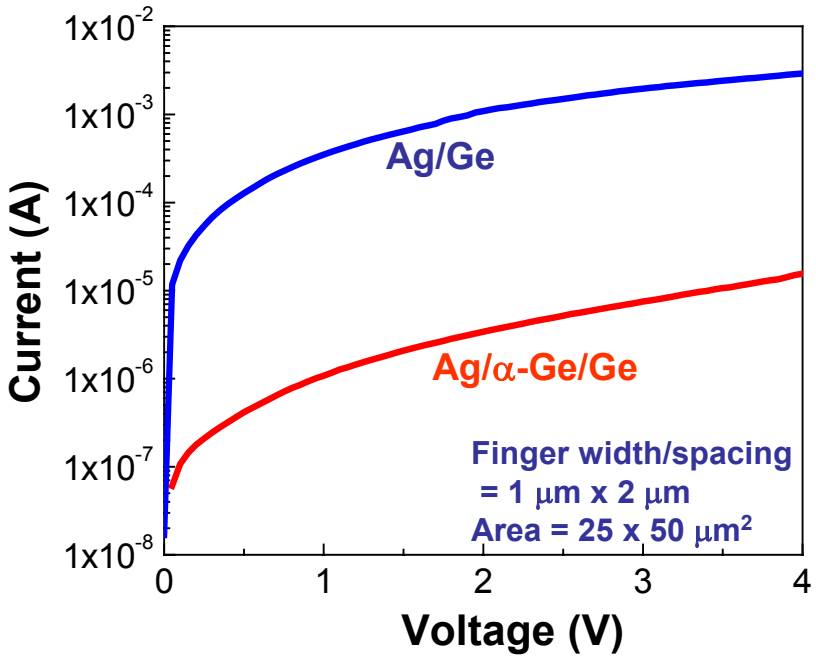


Figure 6.19 Dark current of 1 μm x 2 μm (finger width x spacing) MSM with 25 x 50 μm^2 active area with and without α-Ge Schottky enhancement layer

6.4.2 Photodiode Quantum Efficiency

Figure 6.20 shows the external quantum efficiency. The measured quantum efficiency was not strongly dependent on bias. To have a high signal to noise ratio, the quantum efficiency was measured at a low bias of 0.2 V. At the wavelength of 1.3 μm, the external quantum efficiency was 14.3 % (internal quantum efficiency = 23.4 % and responsivity = 0.15 A/W) without an anti-reflecting coating. This was about 50 % of the theoretical value calculated for a

top Ge layer thickness of 700 nm and a reflection loss of 39 %, which could be reduced to 12 % with a 224 nm-thick SiO_2 anti-reflecting coating. The decrease in the quantum efficiency at the wavelength of 1.55 μm resulted from a lower absorption coefficient.

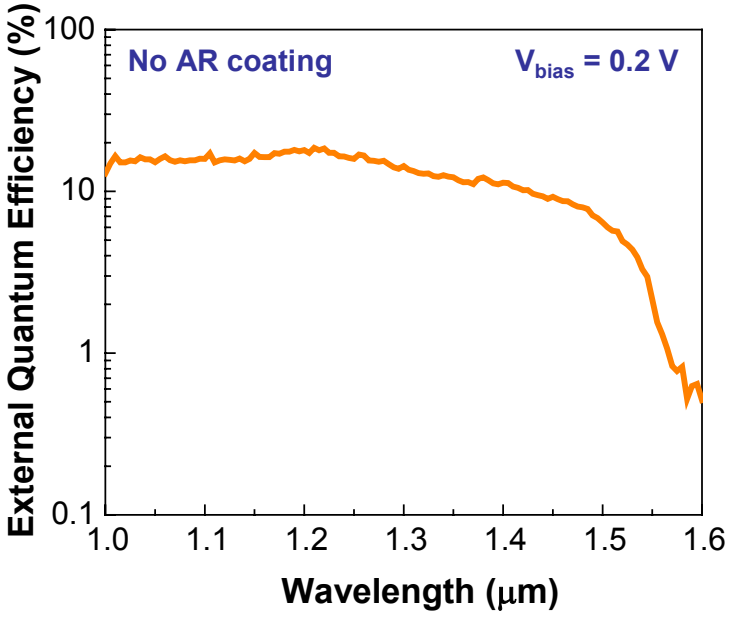


Figure. 6.20 External quantum of 1 μm x 2 μm (finger width x spacing) MSM with 25 x 50 μm^2 active area with amorphous Ge Schottky enhancement layer

6.4.3 Photodiode Frequency Response

The frequency response is shown in Figure 6.21. At biases of 1 V, 2 V, 3V, and 4V, the 3-dB bandwidths were found to be 1.5 GHz, 2.8 GHz, 3.1 GHz, and 4.3 GHz, respectively. The fact that these photodetectors operate at low

bias voltages is attractive for integration with Si ICs. In comparison with the interdigitated Ge PINs fabricated on Ge/GeSi/Si substrate, the Ge MSMs on Ge/Si substrate without buffer layer showed higher bandwidths even at lower biases. This was possible because fewer carriers were generated in the low-field Si regions where the carrier velocity was relatively low. The bandwidths reported here are the highest for Ge photodetectors on Si substrate at 1.3 μm.

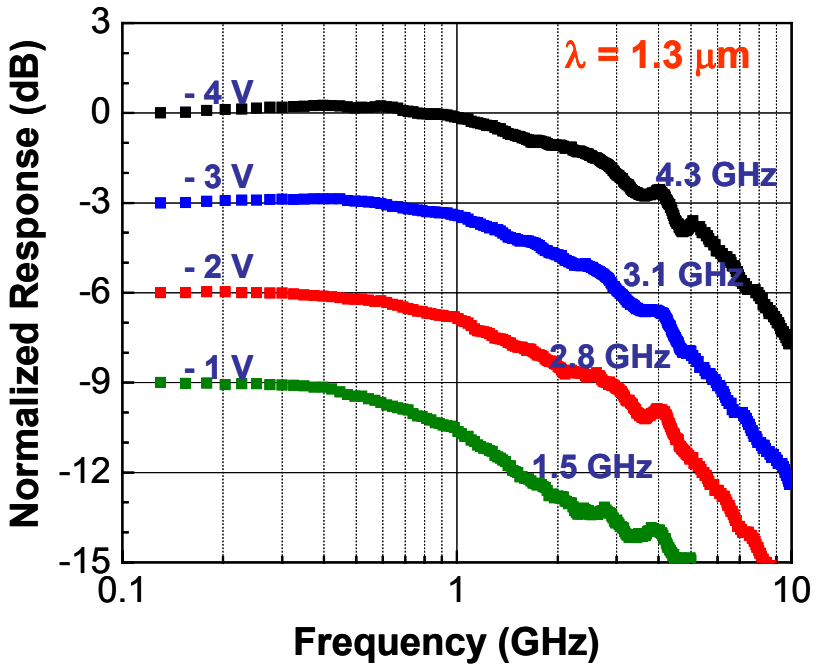


Figure 6.21 Frequency response of 1 μm x 2 μm (finger width x spacing) MSM with 25 x 50 μm^2 active area with amorphous Ge Schottky enhancement layer at reverse bias of 1 V, 2V, 3 V, and 4 V

6.4.3 Surface passivation

The formation of a stable passivation layer on a Ge surface has been a critical issue in Ge technology. As discussed in Chapter 3, Ge native oxide is not stable. The oxidation of Ge and the desorption of Ge oxides occurred in ways such that the simultaneous reactions resulted in surface loss. Thermal desorption and deoxidation happen to all semiconductor materials. However, the extent is not as significant as we found with Ge. Ge photodetectors fabricated in this work showed a relatively high dark current compared with other semiconductors. The dark current increased because of the planar structure and the high surface electric field without stable passivation.

To reduce the dark current in Ge MSMs fabricated on Ge epitaxial layers grown directly on Si substrates, amorphous Ge interfacial layers were used. To further reduce the leakage current, surface passivation was investigated using chemical treatments on Ge surface. In this study, Ge MSMs fabricated on bulk Ge wafer were used. Several types of chemical treatments have been reported for surface passivation [6-13]-[6-18]. These chemical treatments passivated semiconductors by leaving the surface H-, Cl-, S-, or alkyl-terminated. In this work, completed MSMs were dipped into a $(NH_4)S_x$ solution for 10 min. Following this chemical treatment, the dark current was reduced by more than one order of magnitude, as shown in Figure 6.22.

In surface passivation, the ambient stability is another important issue. To evaluate the ambient stability, the dark current of MSMs was re-measured a few days after surface passivation. The increase in the dark current was small even after a week. This indicated that the S-terminated Ge surface was quite stable. An overlayer, however, was required to keep the S-terminated Ge surface stable for a long period of time. In the deposition of an overlayer, the temperature has to be low enough to be able to maintain the passivation layer. The dependence of an S-terminated Ge surface on the temperature will require further research.

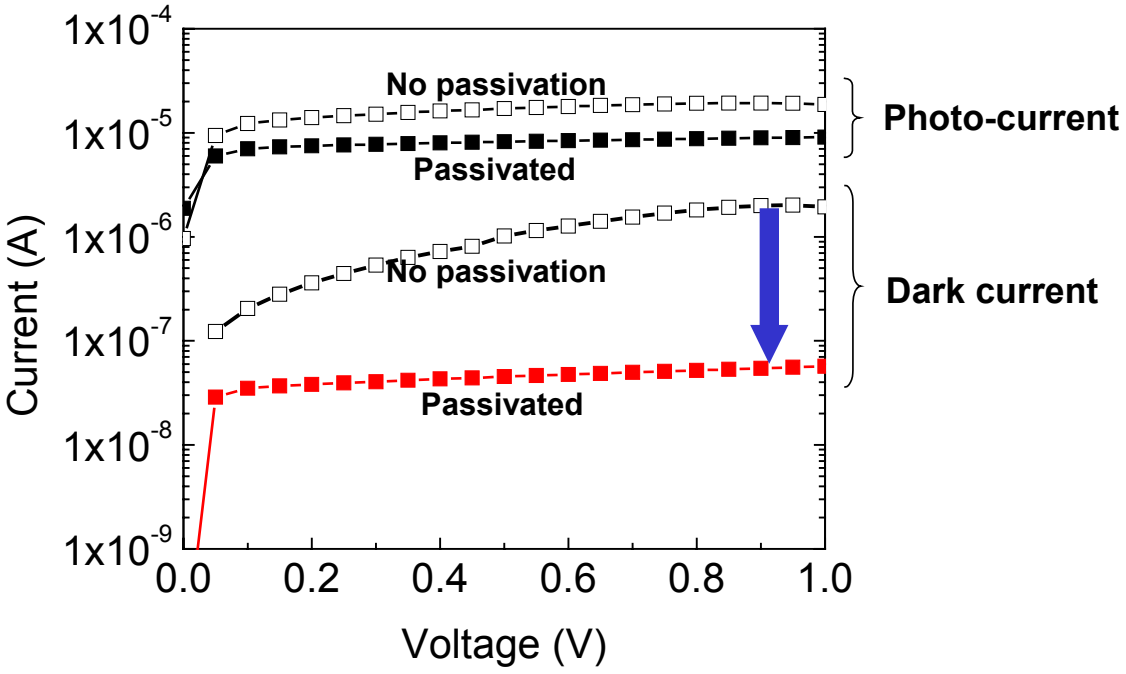


Figure 6.22 Reduced dark current of MSMs after $(NH_4)S_x$ surface passivation

6.5 Mesa Heterojunction Photodiodes

Figure 6.23 shows a schematic of the device structure. Mesa heterojunction devices were fabricated by standard lithography, etching, and metallization processing steps. Mesas were etched by RIE to the Si substrate, and passivated with 2000Å of SiO_2 on the sidewall to reduce the surface leakage current. Ti/Au(350 Å /1250 Å) for the p- and n-type contacts were deposited by e-beam evaporation and patterned by lift-off process. In order to illuminate from the backside, the Si wafer was polished and 2000Å of SiO_2 was deposited as an anti-reflecting coating. Microwave contact pads were fabricated for high-speed measurement.

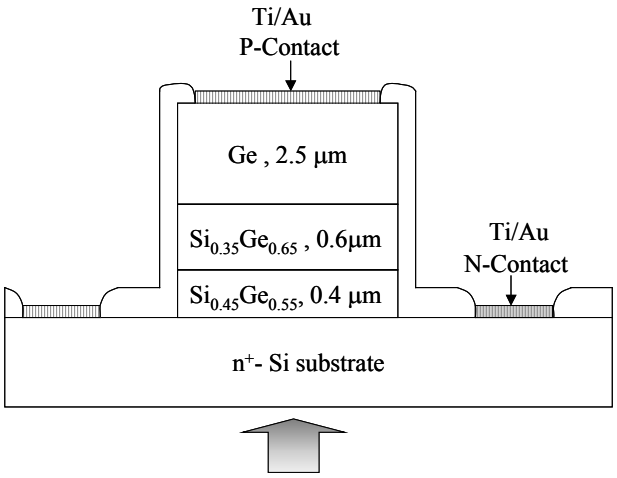


Figure 6.23 Cross sectional schematic of the Ge on Si photodiode structure

Figure 6.24 shows the current voltage curves for 24 μm, 48 μm and 100 μm-diameter mesas. For 24μm-diameter devices, the dark current was 0.06μA, 0.27 μA and 1.07 μA at reverse biases of 1V, 3V and 10V, respectively.

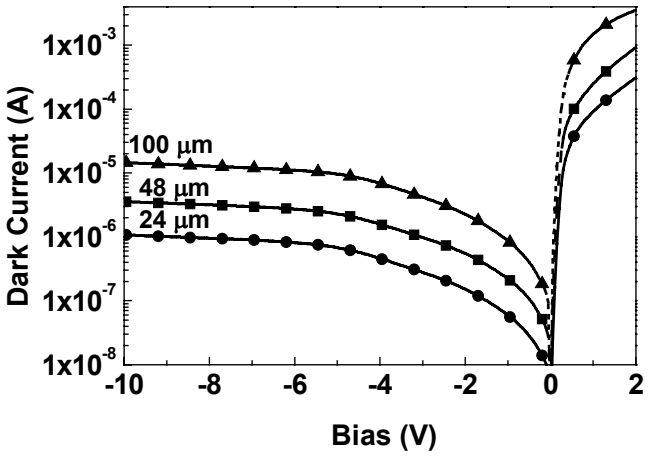


Figure 6.24 I-V characteristics of Ge mesa diodes of different diameters. Dark circle and solid line: 24μm; Dark square on solid line: 48μm; Dark triangle on solid line: 100μm

Figure 6.25 shows the dark current versus mesa diameter. The square on dash-dotted line shows the calculated dark current including contributions from bulk leakage current (proportional to area) and surface leakage current (proportional to diameter). The triangle on dashed line was calculated assuming only bulk leakage current. At 1V reverse bias, the dark current can be fit to the quadratic curve very well, which indicates that bulk leakage dominates. At high

bias voltage, the surface leakage current become more prominent, but the bulk component still dominates. It appears, therefore, that the dark current is mainly attributable to defects in the epitaxial layer. The dark current density is 12mA/cm^2 at -1Vand 28mA/cm^{2}at -2V. This is lower than a heterojunction photodetector fabricated without the SiGe buffer layers [6-19], but higher than devices fabricated on optimized graded buffer layers [6-20].

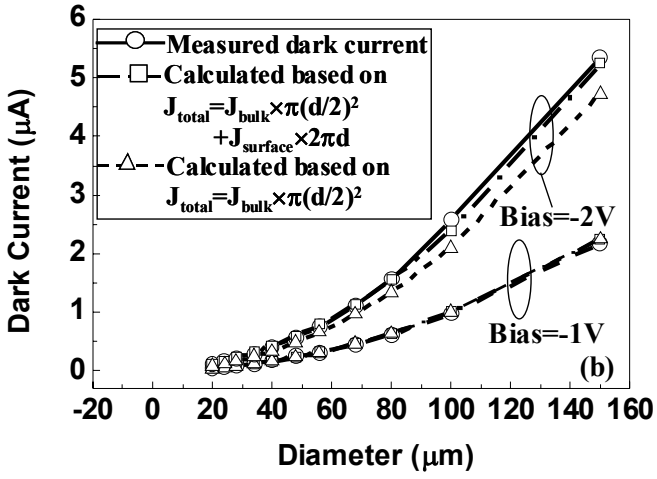


Figure 6.25 Dark current versus area at 1V and 2V reverse bias; Circle on solid line: measured data; Square on dash dotted line: fit from bulk leakage/area and surface leakage/diameter; Triangle on dashed line: fit to square of the diameter. At –1V, the bulk current density is 12mA/cm^2, the surface current density is 0.318μA/cm; and at –2V, the bulk current density is 28mA/cm^2, the surface current density is 0.7μA/cm.

6.6 Summary

A Ge photodiode structure that can be integrated with CMOS has been fabricated. Previously, our lab fabricated the Si optical receivers using Motorola's 130 nm process technology. Those receivers were successfully demonstrated and achieved the best performance in terms of operating bit rate and receiver sensitivity reported to date. In order to move the operating wavelength of those receivers from 850 nm to 1300 nm, we have proposed to substitute a Ge photodiode for the Si photodiode. Currently, most of optoelectronic communications systems are based upon III-V compound optoelectronic components. Although III-V semiconductors provide high detection efficiency and high speed, incorporating them in the existing Si technology is difficult and expensive. Hybrid III-V photodetectors can be used as photodetectors but a monolithically integrated Si-based optical receiver can further reduce the cost and realize mass-produced optoelectronic integrated circuits (OEICs).

In developing the process technology for a Ge interdigitated photodiode, ion implantations were used to form the n^+- and p^+- regions. In the initial phase of this work we used bulk Ge substrates. The devices that were subsequently fabricated achieved good quantum efficiency at 1.3 μm (67% without an antireflection coating) and excellent bandwidth (1.8 GHz at 5 V). In the middle

part of the project, we received Ge-on-Si wafers that were grown by Unaxis using low energy plasma enhanced chemical vapor deposition (LEPECVD). These wafers consisted of a 1 μm-thick Ge epitaxial layer grown on Si substrate using a 10 μm-thick graded SiGe buffer layer. The PIN structures that were developed on bulk substrates were fabricated on these Ge-on-Si wafers. The dark current was approximately 10x higher owing to a higher defect density but it was still acceptable. The quantum efficiency was somewhat lower than the bulk devices because the absorption region was thinner. The thin Ge active region also resulted in improved frequency response. Bandwidths of 2.2 GHz, 3.5 GHz, and 3.8 GHz were achieved at bias voltages of -1 V, -3 V, and -5 V, respectively.

In the latter part of the project, taking a more practical approach to the fabrication of monolithically integrated Si-Ge optical receivers, we grew a thin epitaxial Ge layer directly on Si substrates. The metal-Ge-metal photodetectors were fabricated on 700 nm-thick epitaxial Ge layers directly grown on Si substrate. Ge epitaxial layers were highly defective and found to be p-type with an acceptor concentration of $\sim 10^{17}$ cm^{-3}. A higher bandgap amorphous Ge layer was introduced between the Schottky contact and the Ge epitaxial layer to increase Schottky barrier height, which decreased the leakage current by more than two orders of magnitude. However, the thermal stability of those photodetectors was found to be unstable. I annealed those MSMs at 450 ^{o}C for

5 minutes and then made the dark current measurement at room temperature. The dark current increased dramatically. What this indicated was that amorphous Ge might transform to polycrystalline Ge because of solid-state epitaxy. In that experiment, I used an amorphous Ge interfacial layer as an aid to reduce the dark current. The best way to improve the dark current of the photodetector is to grow high-quality Ge epitaxial layers with minimal defect density.

To improve the material quality of Ge-on-Si, many techniques have been investigated. Recently, a growth technique that utilized thin buffer layers has been reported. By optimizing the Ge concentration of two thin SiGe buffer layers, many threading dislocations were "trapped" at the heterojunction interface, thereby reducing the dislocation density in the Ge layer. I have utilized that approach to improve material quality and device performance. Mesa-heterojunction photodiodes were fabricated on a Ge epitaxial layer grown on Si substrate using two intermediate buffer layers.

I used germanium as a photodetector material in the fabrication of Si/Ge-based optical receivers. It is advantageous to use Ge photodetectors instead of Si photodetectors when a longer wavelength, a thinner absorbing layer, a higher quantum efficiency and/or a higher speed of the photodetector is needed. Although higher-speed photodetectors have been built in a variety of III-V compound semiconductors for long-haul optical transmission, the use of Ge is

beneficial in terms of lower cost fabrication and compatibility with Si complementary metal oxide semiconductor (CMOS) processes using existing silicon manufacturing infrastructure.

Despite these advantages, integration of Ge technology into Si CMOS process has not been widely deployed because of a difficulty of Ge epitaxy on Si substrate. We have conducted many types of Ge epitaxy techniques to reduce the defect density. Recently, we utilized a thin SiGe buffer technique and demonstrated high performance photodetectors. I believe that in the future we can improve crystal quality and photodetector performances by optimizing growth conditions such as the gradient of Ge concentration in SiGe layers, the number of heterostructure interfaces, and the thermal annealing. The progress in Ge and SiGe epitaxy on Si substrate also has a significant impact on electronic devices. For example, in strained-Si MOSFETs technology, SiGe is selectively grown in the source/drain region to induce a stress to the channel region. Also, SiGe layer is used as a virtual substrate for the strained Si layer.

Appendix: Publications

1. Jungwoo Oh and J. C. Campbell, "Thermal desorption of Ge native oxides and the loss of Ge from the surface," *J. Electronic Materials*. vol. 33, pp. 364-367, 2004.

2. Jungwoo Oh, S. K. Banerjee, and J. C. Campbell, "Metal-germanium-metal photodetectors on heteroepitaxial Ge-on-Si with amorphous Ge Schottky barrier enhancement layers," *IEEE Photon. Technol. Lett*. vol. 16, pp.581-583, 2004.

3. Jungwoo Oh and J. C. Campbell, *IEEE LEOS,* ThJ4, 2003.

4. R. Jones, S. Thomas, S. Bharatan, R.Thoma, C. Jasper, T. Zirkle, G. Edwards, R. Liu, X. Wang, Q. Xie, C. Rosenblad, J. Ramm, G. Isella, H.von Kanel, Jungwoo Oh, Joe Campbell, "Gigahertz photodetectors fabricated in heteroepitaxial Ge-on-Si for use in integrated receivers," *American Physical Society*, March Meeting, 2003.

5. Jungwoo Oh and J. C. Campbell, "Interdigitated Ge p-i-n Photodetectors fabricated on Si substrate using graded SiGe buffer layers," *IEEE J. Quantum Electron*, vol. 38, pp. 1238-1241, 2002.

6. Jungwoo Oh, S. Csutak, and J. C. Campbell, "High-speed interdigitated Ge PIN photodetectors," *IEEE Photon. Technol. Lett*. vol. 14, pp.369-371, 2002.

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9. Jung-Woo Oh and J-L. Lee, "Application of nonalloyed PdGe ohmic contact to self-aligned gate AlGaAs/InGaAs pseudomorphic high-

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