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# Germanium MOS Devices Integrating High-κ Dielectric and Metal Gate

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# Germanium MOS Devices Integrating High-κ Dielectric and Metal Gate

**by**

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## Dissertation

Presented to the Faculty of the Graduate School of
The University of Texas at Austin
in Partial Fulfillment
of the Requirements
for the Degree of

## Doctor of Philosophy

The University of Texas at Austin
May 2007

# Dedication

To my grandmother, my parents and my younger sister

## Acknowledgements

It has been a long way since I came to Austin to start my PhD study. I have experienced many happy times and also many hard times. I have earned a lot but also had some regrets. In these years, so many people have given me support, help and encouragement. Firstly, I wish to express my deepest appreciation to my supervisor, Dr. Dim-Lee Kwong. Without his guidance, support, advice, encouragement and trust, this work could not have been done. He can always catch the newest directions with the technology development in our research area and I have learned so many things from him. Great thanks to my committee members, Dr. Register, Dr. Dodabalapur and Dr.Chen at UT-Austin and Dr. Peterson at Intel Corporation for their insight advice in my research. Dr. Peterson has carefully reviewed my manuscript and given me many good suggestions for this dissertation. Deeply thank the technical and facility staffs at UT Microelectronics Research Center, William Ostler, William James, William Fordyce, and James Hitzfelder, for their excellent jobs and supports in building and maintaining the systems we used in the research. Many thanks go to Carol Assadourian and Jean Toll for all their assistance in my graduate study.

Special thanks to Dr. Hongfa Luan, my mentor when I started my research. He guided me and taught me everything in my early time at MRC.

I would like to express my deep gratitude to my group members. Thank Choongho Lee, Songjoo Lee and Teaksoo Jeon for their help and guide in my early research period. Thank Nan Lu, my research partner, for so many helps from her and

so many valuable discussions with her. Thank Jongjin Lee, Sangho Bae, Younghee Kim, Changhwan Choi, Jang Sim, Xuguang Wang, Huangchun Wen, Jun Liu, Feng Zhu, and Chiahsun Tu. I sincerely appreciate your help, advice, and cooperation offering me and I have enjoyed and I miss so many happy times and funs with you all.

My college classmates in Austin, Yang Chen, Kui Wu, Geng Wang, Shuling Wang, Heling Yi, Jianan Yang, and my friends Junjun Liu, Xia Lu, Zhihong Huang, Dingyuan Lu and Yueran Liu have given me lots of helps for my life and my study. Thank you so much.

I also want to acknowledge our research collaborators, Dr. Dimitri A. Antoniadis, Dr. Andrew P. Ritenour, and Dr. Minjoo Larry Lee at the Microsystems Technology Laboratory, Massachusetts Institute of Technology. They helped to perform a lot of TEM and other physical analyses in the research. Thank Amado Rarmrez and Advanced Micro Devices Corporation to supply the germanium wafers and performance sample physical analyses for us.

I would like to express my special thank to Yinghui Cai. She has given me precious encouragement in my hard time and I will always appreciate her.

Finally, I want to express my greatest gratitude to my parents for their support and to my mother for her everlasting love. My grandmother brought me up and she had always wished me to earn the highest degree. Her wish has come true finally. My sister' trust and love always inspire me. And I would also like to express my deep gratitude to my aunts and my cousins, and their families for their long-time support and encouragement.

# Germanium MOS Devices Integrating High-κ Dielectric and Metal Gate

Publication No._____

Weiping Bai, Ph.D.

The University of Texas at Austin, 2007

Supervisor: Dim-Lee Kwong

ABSTRACT

This dissertation investigates the fabrication and characteristics of the metal-oxide-semiconductor (MOS) devices built on germanium substrates integrating $HfO_2$ high-κ dielectric and TaN metal gate electrode. The metal-gate/high-κ/germanium MOS stack, by taking the advantages of the high carrier mobility from the germanium channel and the sub-nm equivalent-oxide-thickness (EOT) scaling capability from the high-κ dielectric and the metal gate electrode, offers a possible solution for the future advanced complementary MOS (CMOS) applications to further boast the transistors' driving current for faster operation.

Due to the unstable and poor-quality natively grown germanium oxide, surface treatment is very critical in germanium device fabrication in order to remove the native oxide and prevent its growth, as well as suppress the interdiffusion across the interface. Several wet cleaning methods and an *in situ* cleaning technique by Ar anneal have been investigated. Surface passivation techniques, including $NH_3$-based surface nitridation (SN) by forming a $GeO_xN_y$ layer and silicon interlayer (SiIL) passivation by growing an ultra-thin (several monolayer) silicon layer between the high-κ dielectric and the substrate, have been studied and proved able to improve device performance significantly. Both p- and n-channel germanium transistors have been successfully fabricated. 1.8X enhancement of peak mobility in p-channel and 2.5X in n-channel over the silicon control devices have been achieved.

The interface growth mechanism between the germanium substrate and the dielectric layer has been investigated. Two competing processes occurring at the interface determine the formation of the interfacial layer and affect Ge outdiffusion. Substrate dopants are found playing important roles, which causes the variations in the interfacial layer formation on different types of substrates and so on in the electrical properties. The relatively high diffusivity of dopants and germanium atoms in bulk germanium and the induced structural defects near the surface may severely degrade the device performance. This can well explain the very poor performance of the n-channel devices reported recently by several groups.

Performance degradation of the germanium devices after thermal anneal, which is resulting from the interdiffusion and germanium oxide desorption, suggests that thermal stability is a concern in high temperature processes and more stable

passivation techniques may be required. Long term reliability study indicates that $HfO_2$ dielectric with SN treatment on germanium is robust against TDDB stress and the long term reliability (TDDB) is not a concern for germanium MOS devices.

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# Chapter 1: Introduction

## 1.1 BACKGROUND

Since the 1960s, metal-oxide-semiconductor (MOS) device technologies have been improving at a dramatic rate [1]. A large part of the success of the MOS transistor is due to the fact that it can be scaled to increasingly smaller dimensions, which results in higher performance — transistor delay time has decreased by more than 30% per technology generation resulting in a doubling of microprocessor performance every two years.

The aggressive scaling of MOS devices is quickly reaching the fundamental limits of $SiO_2$ as the gate insulator since the oxide thickness should decrease at each technology node to improve the on-current of a transistor. Large on-current can charge the node capacitors more easily; this increases circuit speed. At the same time, the rules require that the supply voltage be lowered as well to reduce dynamic power consumption and to mitigate hot-carrier-induced degradation. However, in the process, the gate oxides have become fantastically thin — according to the International Technology Roadmap for Semiconductors (ITRS) [1] complementary-metal-oxide-semiconductor (CMOS) devices with gate length below 70 nm will need an oxide thickness of less than 1.5 nm, which corresponds to a few layers of silicon dioxide ($SiO_2$) atoms. With such a thin gate oxide, direct tunneling occurs resulting in an exponential increase of gate leakage current. Even though transistors can still function, the resulting gate leakage current will increase the standby power

dissipation (an extremely important factor in low-power wireless electronics) and will deteriorate the device performance and circuit stability for very large scale integration (VLSI) circuits. An alternative gate dielectric with dielectric constant (κ) greater than that of $SiO_2$ (κ = 3.9) has been proposed to reduce the gate tunneling leakage with an increase in physical thickness of the gate insulator, and thus obviate integrated circuit (IC) power concern, while still achieving the required gate electrode capacitive coupling with silicon. This has resulted in wide investigation and strong progress in the development of high-κ dielectrics. Among various high-κ gate dielectrics, hafnium oxide ($HfO_2$) and hafnium oxide-based compounds have become the leading candidates to meet the scaling requirements stated in the ITRS [2] and the initial use will be for low standby power applications in the very near future as shown in Fig. 1.1. $HfO_2$ have fairly high κ ~ 20-25, and sufficiently large bandgap ($E_g$) ~ 5.6 eV. Additionally, $HfO_2$ is thermo-dynamically stable in contact with silicon, and has been scaled down to an equivalent oxide thickness (EOT) ≤ 10 Å [3]. Although EOT scaling and low gate leakage current ($J_g$) have been demonstrated, many challenges regarding high-κ materials' implementation remain. One of the major challenges is the significantly lower channel mobility for the transistors made of high-κ dielectrics as compared to their $SiO_2$ counterparts [4][5], which is mainly due to the worse quality of the high-κ/Si interface compared to $SiO_2$/Si.

A potential solution to this problem is to change the substrate from silicon to another semiconductor material with higher carrier mobility, such as strained silicon, SiGe, GaAs and germanium. Originally transistors were fabricated on germanium substrate, but lack of stable germanium oxide has been an obstacle in CMOS device

realization in germanium. Therefore, for decades silicon has been used in CMOS technology due to better qualities of its native oxide such as low leakage current, low interface state density, and good thermal stability. Therefore, once $SiO_2$ cannot be used anymore for future advanced devices, part of the advantages of silicon as the semiconducting element in a MOS transistor is gone, and other semiconductors with a higher mobility are attractive to be studied.

As the conventional gate electrode, poly-Si gate has many advantages such as adjustable work function, excellent compatibility to $SiO_2$ and superior thermal stability. However, as CMOS devices are scaled into sub-0.1 um regime, poly-depletion effects and boron penetration become significant concerns [6][7][8]. They increase the EOT (0.3-0.5 nm), degrade the device performance, and make further gate oxide scaling problematic. Moreover, for high-κ dielectric applications, its compatibility to the dielectric material and the work function's Fermi-level pinning effect cause other problems. Therefore, metal gate electrodes are being explored to replace the polysilicon gate to minimize the poly-depletion effects in addition to reducing the gate-line sheet resistance. Metal gate is a requirement for high-κ application in advanced CMOS realization [7]. Among all the candidates, tantalum nitride (TaN) [9] has been widely investigated as one of the candidates with good thermal stability in high-κ gate stack MOSFETs. Because of its mid-gap work function, TaN is also a promising gate material for the advanced non-bulk device applications in the future [10].

## 1.2 MOTIVATIONS FOR THE STUDY OF GERMANIUM CHANNEL MOS DEVICES

Germanium channel MOS devices have recently received renewed interest because germanium offers much higher intrinsic mobility for both holes (4X) and electrons (2.5X) than silicon does due to the smaller effective mass of carriers. The higher intrinsic carrier mobility will improve injection current density and thus allow faster operation speed in VLSI circuits. Besides this, the smaller bandgap (0.66 eV at 300K) germanium will enable a low-voltage operation and, in turn, reduced power consumption. The main physical properties of germanium and silicon are listed in Table 1.1 [11]. As compared to silicon, germanium also has higher intrinsic carrier density, larger dielectric constant, lower melt point, and slightly larger lattice constant.

In the past forty years, many gate dielectric materials, such as germanium oxynitride ($Ge_2N_2O$) [12][13][14], $Ge_3N_4$ [15][16], $SiO_2$ [17][18] and $Al_2O_3$ [19][20], have been investigated in germanium-based MOS system. The peak channel mobilities of 1200 $cm^2$/V-s for electrons and 1050 $cm^2$/V-s for holes have been reported by using $Ge_2N_2O$ dielectric with the EOT of 200 Å and 130 Å, respectively [12][13]. The availability of high-κ materials used as the gate dielectric in recent years makes it possible to use germanium as a CMOS channel material beyond the 32-nm technology node. Integrating high-κ and germanium substrate would be expected to achieve higher channel mobilities for both electrons and holes than the high-κ/Si system and sub-1 nm EOT scaling down can still remain.

Because the diffusivities of various atoms in germanium are much higher than in silicon [21], it allows and requires lower processing temperature (especially

for dopant activation) for the germanium-based devices (500-600°C) as compared to that for silicon-based devices (900-1000°C). This reduces the need of thermal budget in process and alleviates the concern on the thermal stability of metal gate/high-κ system, suggesting an attractive possibility for integration of high-κ dielectric and metal gate in the germanium MOS technology.

Since 2002, high-κ/Ge system has received more and more attentions [22]. Promising results have been demonstrated in both bulk germanium [22]-[28] and germanium-on-insulator (GOI) devices [29]-[32]. As compared to high-κ/Si control devices, more than 2X mobility enhancement for both electrons and holes in high-κ/bulk Ge system [22]-[28] have been achieved.

The smaller bandgap offers germanium another advantage over silicon in optoelectronic integration since it broadens the absorption wavelength spectrum, which will enhance CMOS functionality.

In recent years, silicon based optoelectronics for communications is being widely studied due to the advantages of i) dramatic cost reduction; ii) a collapse of system size through the integration of different optoelectronic components on the same substrate; and iii) a seamless integration with control and management electronics [33]. However, due to its 1.12 eV bandgap (corresponding to a wavelength of 1.11 μm), silicon is unable to detect near-infrared (NIR) light in the second (1.3 μm) and third (1.55 μm) window of optical fiber communications. The narrower bandgap of germanium (0.66 eV) broadens the absorption wavelength spectrum and make it to be one of the promising candidates for NIR photodetectors. Germanium-on-silicon (GOS) photodetectors have been fabricated by several

techniques such as epitaxially grown, CVD and thermally evaporated germanium on silicon [34][35][36]. The high dislocation density of GOS gave rise to high dark current. Directly using germanium substrate, high quality photodetectors can be fabricated. Therefore, successful germanium CMOS technology will simplify germanium optoelectronic fabrication and make it much easier to implement optoelectronics/CMOS on-chip applications.

### 1.3 CONSTRAINTS AND CHALLENGES

Changing the substrate from silicon to germanium brings new challenges in the formation of high-κ gate stacks. Native germanium oxides (GeO and $GeO_2$) are hygroscopic, water-soluble and inherently thermodynamically unstable. This has been a technology bottleneck in introducing Ge channels to CMOS technology. In addition, the native $GeO_x$/Ge system exhibits poor interface electrical properties [18] and might be too disordered intrinsically [37]. High interface state density ($D_{it}$) of $2\times10^{12}$ /cm$^2$-eV was reported for thermally grown native oxide/Ge interface [38]. J.C. Philips [39] suggested that the rigid glassy $GeO_2$ clusters with locally hexagonal morphologies are unable to completely cover the Ge surface and satisfying all the Ge surface bonds, unlike the case of $SiO_2$/Si interface. Therefore, a key challenge which quickly emerges is the development of a proper germanium surface passivation technique prior to high-κ deposition to obtain a low $D_{it}$ interface. Surface treatment prior to gate dielectric passivation is more critical to improve the interface quality and preserve the advantage of high carrier mobilities in germanium-based MOS devices.

The melting point of Ge (937°C) is much lower than that of Si (1415°C) [11]. This limits the temperatures in many fabrication processes such as activation annealing, postdeposition treatment. The volatility of GeO at as low as 400°C [40] and the high diffusivities of atoms in germanium [21] could be another concern, which may cause poor thermal stability and lead to degradation of the electrical properties of germanium devices during thermal processes.

Though smaller bandgap of germanium offers advantages on optoelectronic system integration and low voltage operation, it also causes higher off-current in MOSFET due to the higher source/drain (S/D) junction leakage. Fortunately, germanium-on-insulator (GOI) technology may eliminate this issue.

The fore-mentioned constraints and challenges must be noted in order to implement germanium-based MOS devices in future applications. Low temperature processes as compared to the conventional silicon processes and some special treatments might be indispensable for a successful Ge CMOS fabrication.

## 1.4 OUTLINE

The key issue for the realization of germanium-based MOS devices in ultra large scale integration (ULSI) applications is the interface quality between the germanium substrate and the dielectric layer. Compared to the silicon-based process, this issue becomes more challenging because of the presence of unstable and poor quality germanium native oxide. It has been observed in silicon-based processes that oxygen diffusion and reaction with silicon during high-κ dielectrics deposition and other thermal processes result in the formation of $SiO_x$ (or silicate) and the increase

of EOT. In case of germanium, it may not only increase EOT, but degrade the quality of the interface and the whole dielectric layer. In this study, we will focus on the germanium surface treatment in order to minimize the influence of $GeO_x$ and improve the interface quality. This work is mainly based on TaN/$HfO_2$/Ge MOS system. The energy band diagrams of this system and TaN/$HfO_2$/Si MOS system are shown in Fig. 1.2.

In Chapter 1, the background about the developments of high-κ dielectrics, metal gate electrodes and channel materials in MOS device applications is given. The motivations of the study on germanium channel MOS devices are discussed and the advantages over silicon-based system are illuminated. The constraints in germanium-based device fabrication and challenges in this study are also discussed.

The overall fabrication processes as well as electrical characterization for germanium-based MOS devices, including capacitors and transistors, are introduced in Chapter 2. The CVD $HfO_2$ deposition process and system are also included.

In Chapter 3, the electrical properties of $GeO_2$ are investigated first. Then the precleaning methods and $NH_3$-based surface nitridation (SN) technique are discussed and the improvements on device performance are demonstrated. Finally the characteristics of Ge p-MOSFET devices fabricated with SN technique are presented.

Another two surface passivation techniques — *in situ* cleaning technique by Ar anneal and silicon interfacial layer passivation are demonstrated in Chapter 4.

The characteristics of Ge n-MOSFETs are demonstrated in Chapter 5. The possible mechanism responsible for the reported poor performance of bulk germanium n-MOSFETs is then discussed.

Due to the abnormal behaviors of the germanium devices on highly doped substrates, in Chapter 6, the electrical properties of germanium MOS devices built on various substrates with different doping types and concentrations are compared. The interfacial layer growth kinetics as well as its dependence on substrate doping (substrate doping effect) is investigated.

In Chapter 7, the thermal stability of germanium MOS devices at a temperature range from 400-700°C is investigated. The study on reliability characteristics are addressed in Chapter 8.

Finally, the conclusions of this research are summarized and the future research topics are proposed in Chapter 9.

| Properties | Si | Ge |
|---|---|---|
| Lattice constant (Å) | 5.431 | 5.646 |
| Density (g/cm$^3$) | 2.328 | 5.327 |
| Breakdown field (V/cm) | ~3×10$^5$ | ~10$^5$ |
| Energy gap at 300K (eV) | 1.12 | 0.66 |
| Dielectric constant | 11.9 | 16.0 |
| Intrinsic carrier concentration (/cm$^3$) | 1.45×10$^{10}$ | 2.4×10$^{13}$ |
| Electron affinity (eV) | 4.05 | 4 |
| Effective Mass | | |
| Electrons | $m_l$*=0.98 | $m_l$*=1.64 |
| | $m_t$*=0.19 | $m_t$*=0.082 |
| Holes | $m_{lh}$*=0.16 | $m_{lh}$*=0.044 |
| | $m_{hh}$*=0.49 | $m_{hh}$*=0.28 |
| Electron mobility (cm$^2$/V-s) | 1500 | 3900 |
| Hole mobility (cm$^2$/V-s) | 450 | 1900 |
| Intrinsic Debye length (μm) | 24 | 0.68 |
| Intrinsic resistivity (Ω-cm) | 2.3×10$^5$ | 47 |
| Melting point (°C) | 1415 | 937 |
| Coefficient of thermal expansion (/°C) | 2.6×10$^{-6}$ | 5.8×10$^{-6}$ |

Table 1.1 Properties of Si and Ge at 300 K [11]

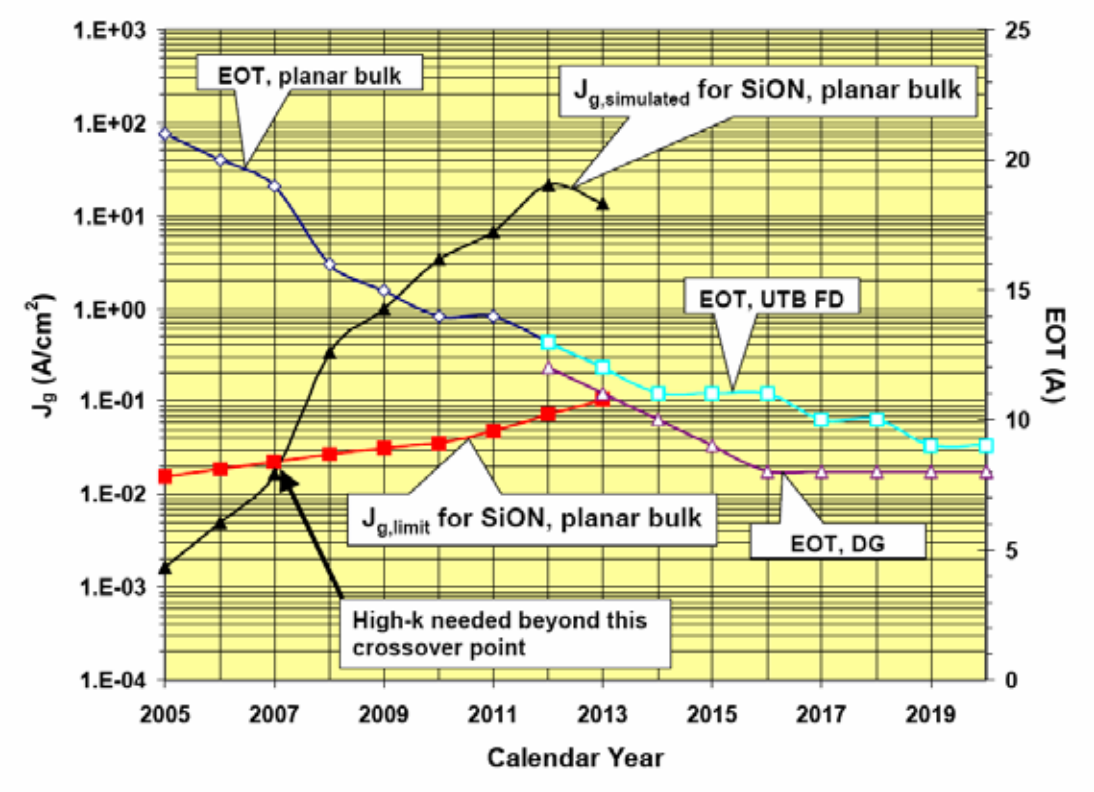



Fig. 1.1 The limit of the gate leakage current ($J_{g,limit}$) required by ITRS versus the simulated gate leakage current ($J_{g,simulated}$) for low standby power applications [1]

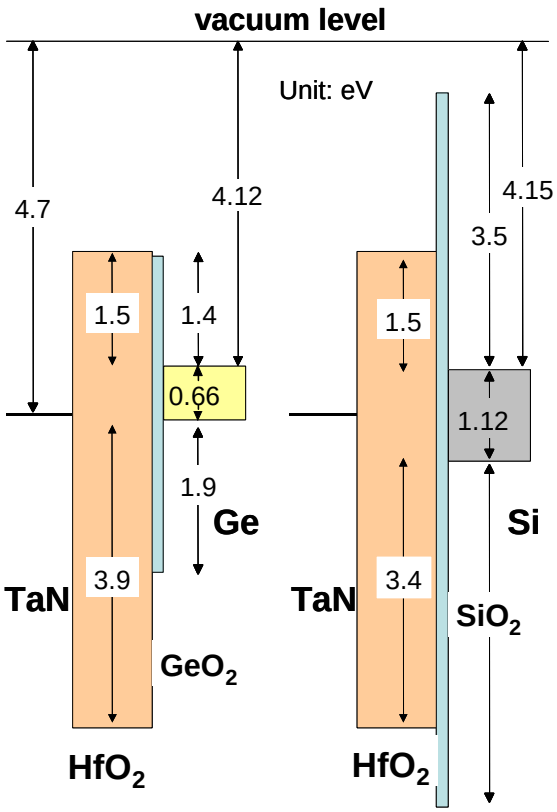



Fig. 1.2 Energy band diagrams of Ge- and Si-based MOS systems with TaN as the gate electrode and $HfO_2$ as the gate dielectric [41][42]

# Chapter 2: Fabrication of germanium MOS devices with CVD $HfO_2$ dielectric and TaN gate electrode

We have discussed the motivations for germanium MOS devices study in the previous chapter. In this chapter we introduce the overall experimental procedures in this study, including the $HfO_2$ dielectric layer deposition and properties, fabrication processes for germanium MOS capacitors and transistors, as well as the electrical and physical characterizations.

## 2.1 CHEMICAL VAPOR DEPOSITION OF $HfO_2$

There are mainly three film growth techniques used for gate dielectric deposition: chemical vapor deposition (CVD), physical vapor deposition (PVD) and atomic layer deposition (ALD). In this study we mainly used CVD technique for $HfO_2$ deposition, which has been proven be able to form high quality high-κ dielectric on silicon [43][44]. PVD technique was also used for selected samples' fabrication, which will be introduced in chapter 6.

In Fig. 2.1-2.2, the diagram and the picture of the CVD system used in this work is displayed. This is an ultra-high vacuum (UHV) metal-organic chemical vapor deposition (MOCVD) system. The base pressure can reach as low as $3\times10^{-7}$ torr at room temperature. As shown in Fig. 2.1, this system has the capability to process various kinds of gas and provides the possibility to attempt various *in situ* treatments in device fabrications. Equipped with halogen lamps, the system can heat a wafer very rapidly by infrared light (tens of centigrade degrees pre second). In

$HfO_2$ deposition, Ar gas was used both as the carrying gas for hafnium-t-butoxide precursor ($Hf(OC_4H_9)_4$) and as the diluted gas for pressure and gas flow control.

The experimental procedure for $HfO_2$ dielectric layer growth is following: the prepared wafer was first loaded into the load-lock and then transferred to the process chamber when the load-lock was pumped down to 50 mtorr. The process chamber was preheated to 150°C to degas the chamber. Until the pressure decreased to $3\times10^{-6}$ torr and the chamber temperature was around 130°C, the reaction gas flowed in and the sample was heated to 400°C in 30 sec and kept at 400°C for desired deposition time (usually 3 min for 5 nm deposition). The chamber pressure during deposition was kept at 3 torr. To improve devices' electrical properties, several kind of *in situ* surface treatments prior to $HfO_2$ deposition have been attempted, including $NH_3$-based surface nitridation, Ar-based *in situ* cleaning, and $SiH_4$-based silicon interlayer passivation. These surface treatment techniques will be discussed in the later chapters.

Fig. 2.3(a) shows the physical thicknesses of the deposited $HfO_2$ films on silicon as a function of the deposition time. The thicknesses were measured by an ellipsometer with a wavelength of 632.8 nm. Fig. 2.3(b) displays the EOT values as a function of the physical thickness. According to the linear relationship

$$EOT = t_{IL} + (\varepsilon_{ox}/\varepsilon_{high\text{-}\kappa})\, t_{high\text{-}\kappa}, \qquad (2.1)$$

where $t_{IL}$ is the thickness of the $SiO_x$ interfacial layer (IL) between the high-κ dielectric and Si substrate, $\varepsilon_{ox} = 3.9$ is the dielectric constant of $SiO_2$ and $t_{high\text{-}\kappa}$ is the

physical thickness of the high-κ dielectric layer, we obtain 0.4-0.5 nm thick IL and $\varepsilon_{high\text{-}\kappa}$ is around 25, which is consistent with the reported dielectric constant of $HfO_2$ in literature [41][43].

## 2.2 GERMANIUM MOS DEVICE FABRICATION

### 2.2.1 Capacitors

The staring materials are (100) oriented germanium substrates. For p-type devices, the substrates are antimony (Sb) doped with a doping concentration of ~$5\times10^{16}$ $cm^{-3}$. For n-type devices, gallium (Ga) doped substrates with several different doping concentrations were used: $3\times10^{18}$, $4\times10^{17}$ and $1\times10^{15}$ $cm^{-3}$. The effects caused by different doping types and concentrations and detailed investigation will be presented in Chapter 5 and 6.

The process flow for germanium MOS capacitor fabrication is summarized in Table 2.1. The first step is wafer surface cleaning. Several surface cleaning methods have been attempted. Cyclical HF precleaning method was decided to be the standard precleaning method since it offers the best results electrically and physically (this will be shown in the next chapter). After the precleaning, surface treatments were performed in order to improve the interface quality and device performance. Following the surface treatments, CVD $HfO_2$ was *in situ* deposited at 400°C, as discussed in the previous section. PVD $HfO_2$ has also been grown for selected samples by oxidizing the sputtered Hf metal layers. Postdeposition anneal (PDA) was carried out for selected samples. 1500 Å TaN metal was reactively sputtered in Ar and $N_2$ at room temperature in a Kurt J Lesker (KJL) sputtering system. The

process pressure during sputtering was 10 mtorr, the power was 700W and the deposition rate was around 400 Å/min. After photo-lithography for pattern defining, gate etching was done by reactive ion etching (RIE) with $CF_4$ as the reactive gas. For selected capacitor samples, postmetallization anneal (PMA) was performed in $N_2$ or forming gas (4% $H_2$ in $N_2$) ambient at 400-700°C for the purpose of thermal stability study.

### 2.2.2 Transistors

Unlike $SiO_2$, thermally grown $GeO_2$ is unable to be used as the field oxide for device isolation due to the soluble property. Germanium oxynitride ($GeN_2O$) is insoluble and thermally stable and can be used as the isolation layer. But the grown process is complex. To eliminate the isolation step and simplify the fabrication process, ring-type structures were used for transistor fabrication. The top image of a typical ring-type structure is shown in Fig. 2.4. The ring-type gate acts as a mask against S/D ion implantation and isolates the source region and drain region which locates inside and outside the ring respectively. The gate length is the width of the ring. The effective gate width is

$$W_{\text{eff}} = \frac{8L}{\ln(1+2L/W_1)}, \tag{2.2}$$

where $W_1$ is the lateral length of the square inside the ring and $L$ is the width of the ring. The derivation of Equation (2.2) is illustrated in Fig. 2.5.

The process flow for germanium transistors is similar to the capacitor process before ion implantation step, as shown in Table 2.1. After the gate patterning, ion implantation was carrier out to form source and drain region. $1\times10^{16}$ $cm^{-2}$ $BF_2$ was implanted at 30 KeV for p-type transistors and $1\times10^{15}$ $cm^{-2}$ As was implanted at 40 KeV for n-type transistors. S/D activation anneal was performed at 400-500°C in forming gas or nitrogen. 200 nm aluminum (Al) was sputtered on both the frontside and the backside of the wafers for metallization. Finally, 300°C annealing was performed in forming gas for 30 min after S/D metal pattering.

Si-based devices were fabricated for control devices. (100) oriented silicon substrates are used for both types of devices. The resistivity of p-type substrates (boron doped) is 1-10 Ω-cm and n-type substrates (phosphorus doped) is 4-7 Ω-cm. The S/D activation annealing for silicon devices was performed at 900°C for 30 sec in $N_2$ ambient.

### 2.3 ELECTRICAL AND PHYSICAL CHARACTERIZATION

The MOS devices were electrically characterized by means of capacitance-voltage (*C-V*) and current-voltage (*I-V*) measurements. *C-V* measurements were performed using a HP 4140B pA meter/DC voltage source and a HP 4275A multi-frequency LCR meter. *I-V* measurements were performed using a HP 4155A semiconductor parameter analyzer. The EOT data were extracted from high-frequency (1 MHz) *C-V* curves by NCSU CVC program [7] for silicon devices or UC Berkeley's *C-V* simulation program for Ge devices taking into account of the quantum mechanical effect [45].

Physical characterizations, including atomic force microscopy (AFM), x-ray photoelectron spectroscopy (XPS), secondary ion mass spectrometry (SIMS), electron energy loss spectroscopy (EELS) and cross-sectional transmission electron microscopy (XTEM) were carrier out for selected samples.

## 2.4 SUMMARY

In this chapter we have introduced the entire experimental part in this work, including the growth of CVD $HfO_2$ dielectric, fabrication procedures for Ge MOS capacitors and transistors and characterizations for MOS devices.

| Processes | Capacitors | Transistors |
|---|---|---|
| Starting material | Ge n-type: ~$5\times10^{16}$ Sb / p-type: $3\times10^{18}$;$4\times10^{17}$; $1\times10^{15}$ Ga | |
| Precleaning | cyclical HF; $H_2O_2$+HF; HF dip | cyclical HF |
| Surface treatment | $NH_3$; Ar; SiIL | $NH_3$ |
| Dielectric deposition | CVD $HfO_2$: 400C 3min with hafnium-t-butoxide precursor ($Hf(OC_4H_9)_4$) / PVD $HfO_2$ | |
| PDA | $N_2$ / $O_2$ / vacuum @ 500-600°C | |
| Metal gate electrode | Reactive sputtering ~1500Å TaN @ 10 mtorr | |
| Gate photo and Patterning | RIE etch with $CF_4$ ~ 4 min | |
| PMA | Forming gas / N2 @ 400-700°C | |
| S/D implantation | | $BF_2$ for p-type / As for n-type |
| S/D activation | | 400-500°C |
| Frontside metal deposition | | 200 nm Al |
| Metal photo and patterning | | Commercial Al etchant |
| Backside metal deposition | | 200 nm Al |
| Anneal | | 300°C in forming gas |

Table 2.1 The fabrication process flow for Ge capacitors and transistors

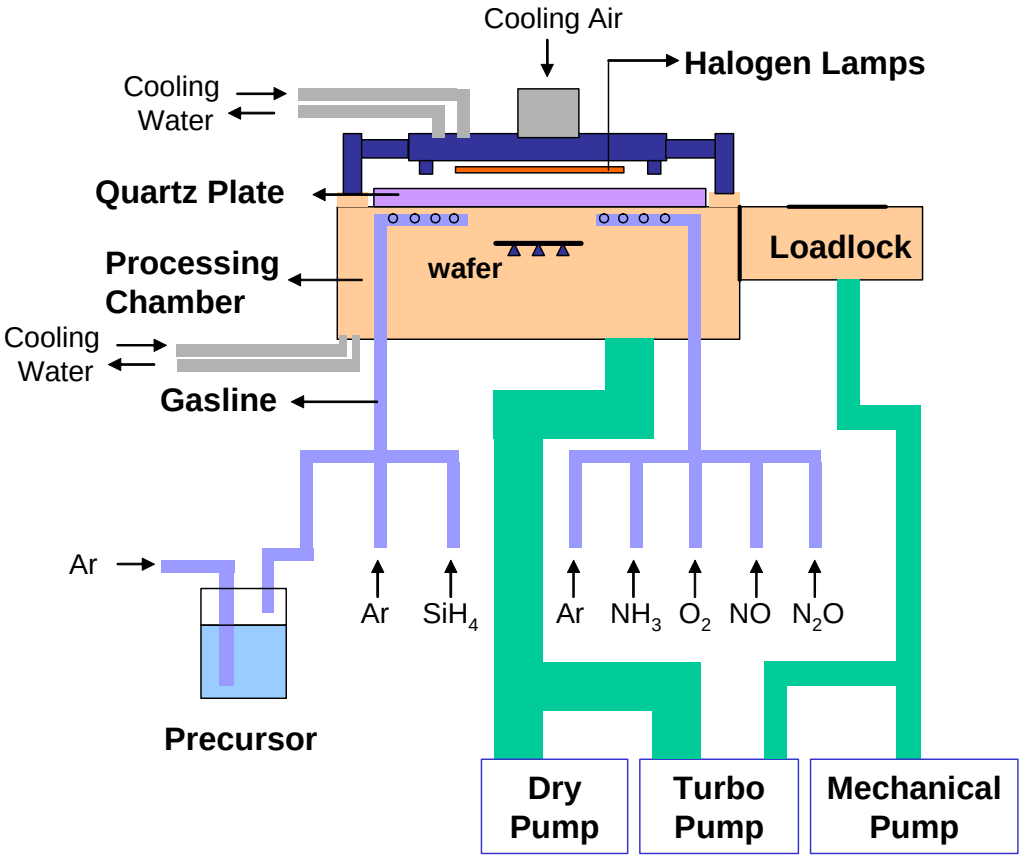
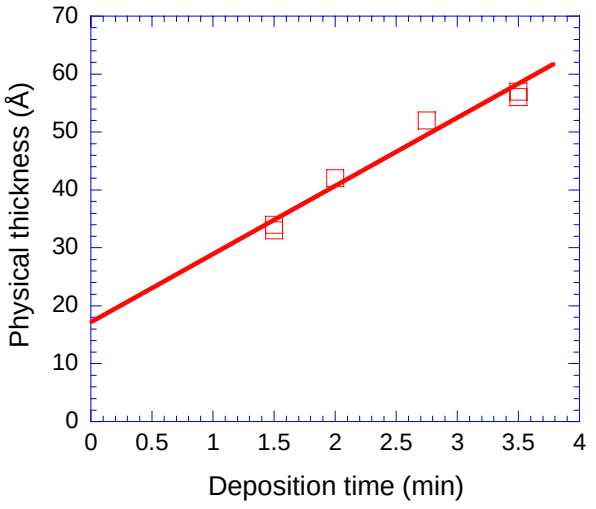
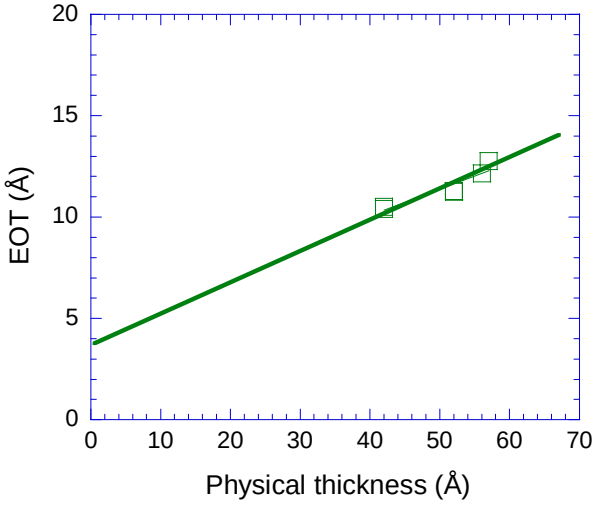



Fig. 2.1 Diagram of the MOCVD system for $HfO_2$ deposition

Fig. 2.2 Picture of the MOCVD system for $HfO_2$ deposition




(a)




(b)

Fig. 2.3 (a) Physical thickness versus deposition time and (b) EOT versus physical thickness for CVD $HfO_2$ films

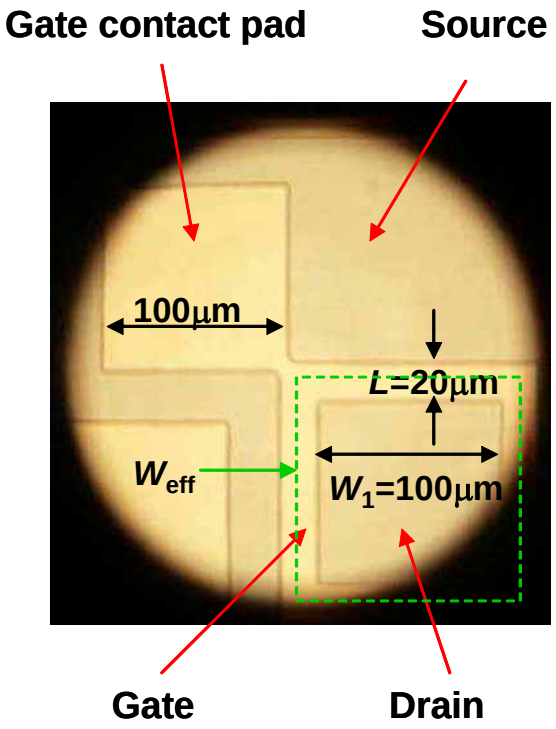



Fig. 2.4 Top image of a typical ring-type transistor structure (before metallization)

$$J = q\,n\,v = q\,n\,\mu\,E \tag{1}$$

$$\begin{aligned} I_{\mathrm{d}}(y) &= \int J\,dx[4W(y)] = Q_{\mathrm{n}}(y)\,\mu\,E[4W(y)] \\ &= C_{\mathrm{i}}[V_{\mathrm{gs}} - V_{\mathrm{t}} - V(y)]\,\mu\,E[4W(y)] \end{aligned} \tag{2}$$

where $J$ is the drain current density, $I_{\mathrm{d}}$ is the drain current, and $E$ is the electric field in the channel, $q$ is the coulomb charge, $n$ is the carriers' density, $\mu$ is the carriers' mobility, $Q_{\mathrm{n}}$ is the charge density per unit area, $C_{\mathrm{i}}$ is the gate capacitance per unit area, $V_{\mathrm{gs}}$ is the gate voltage, $V_{\mathrm{t}}$ is the threshold voltage and $V(y)$ is the voltage at $y$.

$$W(y) = W_1 + (W_2 - W_1)\frac{y}{L} = W_1 + 2\,y,\;\; E = \frac{dV}{dy} \tag{3}$$

$I_{\mathrm{d}}$ is a constant independent of y since the current is continuous everywhere.
Submitting (3) into (2) and integrating from the source to the drain yields

$$\begin{aligned} &\int_0^L \frac{I_{\mathrm{d}}}{W(y)}\,dy = \int_0^{V_{\mathrm{ds}}} 4\,C_{\mathrm{i}}[V_{\mathrm{gs}} - V_{\mathrm{t}} - V(y)]\,\mu\,dV \\ &\frac{I_{\mathrm{d}}}{2}\ln\left(1 + \frac{2L}{W_1}\right) = 4\,\mu\,C_{\mathrm{i}}\left[(V_{\mathrm{gs}} - V_{\mathrm{t}})\,V_{\mathrm{ds}} - \frac{{V_{\mathrm{ds}}}^2}{2}\right] \\ &I_{\mathrm{d}} = \frac{8L/\ln(1 + 2L/W_1)}{L}\,\mu\,C_{\mathrm{i}}\left[(V_{\mathrm{gs}} - V_{\mathrm{t}})V_{\mathrm{ds}} - \frac{{V_{\mathrm{ds}}}^2}{2}\right] \end{aligned} \tag{4}$$

where $V_{\mathrm{ds}}$ is the drain voltage.
Finally, we have

$$W_{\mathrm{eff}} = \frac{8L}{\ln(1 + 2L/W_1)} \tag{5}$$

Fig. 2.5 Derivation of Equation (2.2); readers may refer to [46]

# Chapter 3: Precleaning effect and $NH_3$-based surface nitridation treatment

## 3.1 INTRODUCTION

As introduced in Chapter 1, surface treatment and passivation is much more important for germanium devices than for silicon devices due to the poor quality of native germanium oxide. As the first step in fabrication, precleaning is not only to remove contaminants and native oxides, but also to achieve high-quality starting surface for devices built on. In this chapter, several precleaning methods have been investigated and cyclical HF cleaning exhibited the best results. $NH_3$-based surface nitridation (SN) technique has been successfully applied in high-κ/Si system to obtain lower EOT and $J_g$ by forming a silicon oxynitride layer, which acts as a diffusion barrier and prevents surface oxidation during subsequent thermal processes [47]. Germanium oxynitride ($GeO_xN_y$) is thermally stable and not soluble in water [48]. It has been proven to be a good passivation layer in germanium MOSFET fabrication [12][13][14]. Based on these, $NH_3$-based germanium surface treatment is proposed and dramatic improvements have been achieved, which is presented in Section 3. Finally the excellent performance of germanium p-MOSFETs based on the cyclical HF precleaning and SN treatment is demonstrated.

## 3.2. PRECLEANING EFFECT

Firstly, to investigate the electrical properties of germanium native oxide, and to demonstrate the importance of precleaning, germanium oxide was thermally

grown on n-type Ge substrate in $O_2$ at 500°C for 2 min as the insulator layers and TaN was sputtered as the gate electrodes. *C-V* and *I-V* characteristics are displayed in Fig. 3.1. The capacitance equivalent thickness (CET) is 46.6 Å and the gate leakage current ($J_g$) at 1.5V gate bias ($V_g$) is $7.9\times10^{-3}$ A/cm$^2$, which is more than ten orders of magnitude higher than that of $SiO_2$, as shown in Fig. 3.2. The very high leakage current is attributed to the much smaller bandgap of $GeO_2$ (3.98 eV) as compared to $SiO_2$ (9.0 eV). Very large *C-V* hysteresis (1.1 V @ –2 V ⇆ 3 V sweep) is also observed in Fig. 3.1(a), indicating large amount of traps presented in gate dielectric. The poor electrical properties of germanium native oxide manifest that effectively removing germanium native oxide is critical in order to form high quality gate dielectric and interface.

Several precleaning methods were attempted, as listed in Table 3.1. Both $H_2O_2$+HF and HF (1:5) dip methods caused high gate leakage current and abnormal *C-V* characteristic (Fig. 3.3). Atomic force microscopy (AFM) images show that the high concentration HF solution caused many defects on the germanium surface (Fig. 3.4(a)). $H_2O_2$+HF method produced pretty rough surface with RMS = 2.94 Å (Fig. 3.4(b)). Cyclical HF cleaning brought very smooth surface (RMS = 0.76 Å) (Fig. 3.4(c)) and much improved electrical properties in terms of well-behaved *C-V* and low leakage current, as displayed in Fig. 3.3. In Fig. 3.5, the *ex situ* x-ray photoelectron spectroscopy (XPS) spectra of the samples before cleaning and two days after cyclical HF cleaning are displayed. The intensity switch between Ge peak and Ge-oxide peak in XPS spectra before and after cleaning confirms the effective

removal of germanium native oxide. Hydrogen in HF solution may act to passivate the Ge surface to resist oxidation even after two days' exposure in air.

Based on its physical and electrical advantages, cyclical HF cleaning was selected as the precleaning method in germanium MOS device fabrication.

### 3.3. $NH_3$-BASED SURFACE NITRIDATION TREATMENT

$NH_3$-based surface nitridation treatment in germanium devices was carrier out at 500°C for 2 min in $NH_3$ ambient prior to $HfO_2$ deposition. The $NH_3$ pressure was around 300 torr. In order to investigate the influence of SN treatment, four germanium samples with/without precleaning (cyclical HF dip) and with/without SN treatment were prepared, as referred to as "HF-last", "oxide-last", "SN/HF", and "SN/oxide" samples respectively. The *C-V* and *I-V* characteristics are compared in Fig. 3.6. For these two samples without any precleaning, very negative flatband voltage ($V_{fb}$) were observed, indicating the presence of large amount of positive fixed charges either in the germanium native oxide or on its interfaces to the substrate or $HfO_2$ layer. The minima of $J_g$ are clearly set off from $V_g$ = 0 V. This is caused by the charge exchange between the substrate and the large amount of traps near the interface, which produces a charging/discharging current superimposed on the tunneling current.

With a SN treatment following the precleaning, an EOT of 12.9 Å was achieved with excellent gate leakage current of 6 mA/cm$^2$ @ $V_g$ = 1 V, which is comparable with the reported results on Si and significantly better than the sample without $NH_3$ treatment (EOT = 27.0 Å, $J_g$ = 147.5 mA/cm$^2$ @ $V_g$ = 1 V) as well as

those two samples without precleaning (EOT ≈ 27 Å). SN treatment exhibits a crucial effect on reducing the EOT and the leakage current. This improvement is believed to be contributed to the formation of a $GeO_xN_y$ interfacial layer — it may block chemical interaction between the deposited $HfO_2$ film and the substrate and prevent the growth of low-κ layer during CVD $HfO_2$ deposition, in keeping with the well-known diffusion barrier characteristics of silicon nitride and similar materials.

Physical analyses prove the formation of the $GeO_xN_y$ interfacial layer. The cross sectional transmission electron microscope (XTEM) image of the SN/HF treated stack is shown in Fig. 3.7. An 8 Å amorphous interfacial layer is clearly observed between the germanium substrate and the $HfO_2$ layer. In Fig. 3.8, the electron energy loss spectroscopy (EELS) confirms the incorporation of N in the interfacial layer. Taking dielectric constant $\varepsilon$ = 4.7 [14][49] for $GeO_xN_y$, the dielectric constant of the $HfO_2$ layer is estimated to be 25 from the EOT data and the physical thickness in the XTEM image, consistent with the our previous result and the reported result of CVD $HfO_2$ on Si [43].

The XTEM images of the oxide-last and the HF-last samples are displayed in Fig. 3.9. Without precleaning, the oxide-last sample has a 10 Å native oxide layer initially on the surface prior to the CVD $HfO_2$ process. It is interesting to notice that no interfacial layer can be seen between $HfO_2$ and Ge in Fig 3.9(a). In Fig. 3.9(b), the HF-last sample has a rough surface and does not show clear amorphous interface as observed on the SN/HF surface. This is quite different from the observations in Si-based stacks where a thin layer of $SiO_x$ interfacial layer can be always found. We believe it is associated with the desorption of GeO considering the volatility of GeO

as well as the surface reaction $GeO_2 + Ge \rightarrow GeO$, which was reported by Law [50] that 50% $GeO_2$ can be removed at 200°C and the amount of removal increases as the temperature increases [40].

In Fig. 3.10 Ge depth profiles of those three TEM samples with different surface preparation were compared. Ge diffusion is observed clearly and it is dependent on the surface condition. The more Ge oxide on the surface, the more Ge diffusion was detected in the dielectrics. The nitrided surface sample shows a much reduced Ge profile in the dielectric, indicating suppressed Ge diffusion into the dielectric as a result of $NH_3$ passivation with the precleaning. Ge diffusion has also been reported by other groups in MOCVD deposition of $HfO_2$ at 400-485°C [51][52] and during 600°C anneal in PVD $HfO_2$ process [53].

Besides the reaction taking place at the interface mentioned above: $Ge + GeO_2 \rightarrow GeO$, the formation and desorption of Ge-rich Hf-Ge-O product [54], which is possibly volatile, may be another mechanism for Ge updiffusion. One hafnium atom could replace a germanium atom from the oxide since Hf is more electropositive. Further investigations of the surface reaction mechanism are presented in Chapter 6.

The XTEM images have proved the consumption of $GeO_2$. The incorporation of Ge in the $HfO_2$ dielectrics can lower the dielectric constant, resulting in a large EOT as shown in Fig. 3.6. Meanwhile, the diffusion species, GeO and Hf-Ge-O create the traps and leakage pathways. A rough surface may degrade the interfacial layer and the dielectric layer on top of it as well, as demonstrated in the previous section for the cases of poor precleaning. HF-last stack exhibits a relatively rough

interface, which should be owed to the non-uniform growth of $GeO_x$. The rough interface may further aggravate the gate leakage through the dielectric layer.

The nitrided surface effectively suppresses the growth of $GeO_x$ and Ge diffusion. Besides the improvements in EOT and $J_g$ reduction, the interface quality is improved and the traps density is also reduced. Extracted by Terman method [55] from the high frequency *C-V* curves, the interface state densities ($D_{it}$) are shown in Fig. 3.11. SN treatment dramatically improves the interface characteristics and $D_{it}$ is reduced to $8\times10^{10}$ /cm$^2$-eV, much lower that the $D_{it}$ of the other samples which exhibit $D_{it}$ values around $6\times10^{11}$ /cm$^2$-eV. The effective suppression of the formation of a large amount of dangling bonds created by $GeO_x$ reaction with Ge or $HfO_2$ is the reason. The *C-V* hysteresis behaviors for a sweep bias of –2 V ⇆ 3 V are shown in Fig. 3.12. A large flatband voltage shift ($\Delta V_{fb}$) of 1.37 V is observed in the oxide-last sample. This is due to the enhanced Ge diffusion with a significant amount of germanium oxide existence. The Ge diffusion into $HfO_2$ generates a large amount of defects, resulting in significant charge trapping during the gate voltage sweep. Contributed to the suppression of Ge diffusion thus both improved interface and dielectric film quality, significant reduction of $\Delta V_{fb}$ is observed for in the SN-treated samples. Higher temperature SN treatment at 600°C further reduces $\Delta V_{fb}$ from 0.35V to 0.1V which is believed to be resulting from the improvement of nitrided interfacial layer with more nitrogen atoms incorporated at higher temperature.

Postdeposition anneals (PDA) were carried out at 500-600°C in either $N_2$ or $O_2$ ambient. As shown in Fig. 3.13, PDA treatments cause device degradation with 2-3 Å EOT increase due to oxygen diffusion and oxidation of germanium.

To investigate the conduction mechanism of the leakage current the temperature-dependent characteristics of *I-V* for both germanium and silicon devices are shown in Fig. 3.14. With $\log(J_g)$-$V_g^{1/2}$ and $\log(J_g/V_g)$-$1000/T$ plots [56], we found that Poole-Frenkel emission dominates at low field and Schottky emission dominates at high field for silicon devices. At temperature below 100°C, Schottky emission dominates for germanium devices. From the slope of $\log(J_g)$-$V_g^{1/2}$, $\varepsilon$ is extracted to be 21-24, which is consistent with the result obtained from EOT and XTEM image. At higher temperature, significant increase of leakage current was observed, which may be caused by the excitation of some shallow traps [22] near the interface.

### 3.3 CHARACTERISTICS GERMANIUM P-MOSFETS

With cyclical HF cleaning and SN treatment, ring-type germanium p-MOSFETs were fabricated following the process flow as shown in Table 2.1. SN treatment was done at 600°C for 2 min. The S/D ion implantation condition was $1\times10^{16}$ $cm^{-2}$ $BF_2$ at 35 KeV. 450°C 30 min anneal followed by 600°C 2 min anneal in nitrogen was performed for ion activation. Fig. 3.15 and 3.16 show the typical as-measured drain current-gate voltage ($I_d$-$V_g$), drain current-drain voltage ($I_d$-$V_d$) and split *C-V* data for the bulk Ge p-MOSFETs. The p-type Ge devices have a -0.19V threshold voltage, 80 mV/decade subthreshold swing (S.S.), and 1.8 nm CET (extracted from the inversion-side of the split *C-V*). The silicon control devices with a simultaneously processed gate stack also exhibited normal characteristics. The low-field mobility for all devices was extracted by using the integrated inversion charge

$Q_{inv}$ (obtained from the inversion-side of the split $C$-$V$) and $I_d$-$V_g$ data from the same device. The effective vertical field ($E_{eff}$) was calculated from the expression [57]:

$$E_{eff} = \frac{1}{\varepsilon_{Ge}}\left(|Q_b| + \frac{|Q_{inv}|}{3}\right), \tag{3.1}$$

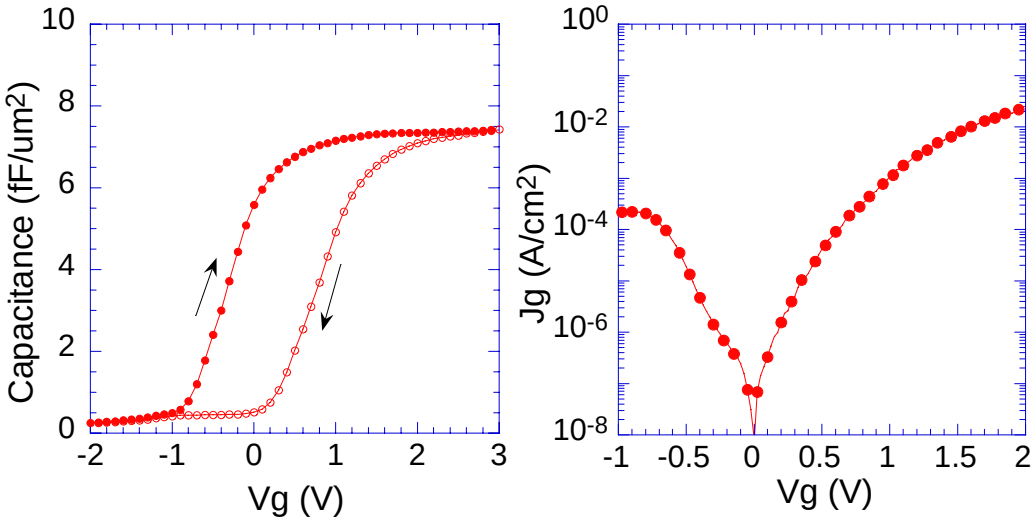
where $\varepsilon_{Ge}$ is the dielectric constant of Ge and $Q_b$ is the bulk depletion charge calculated from the body doping concentration. Fig. 3.17 compares the extracted hole mobility from germanium devices, silicon control devices, and Ge p-MOSFETs with a germanium oxynitride gate dielectric from the literature [49]. Compared to the silicon control wafer, the bulk Ge devices show an enhancement of 1.4-1.8X.

### 3.4 SUMMARY

In this chapter, we have demonstrated the critical roles of precleaning and germanium pre-gate surface treatment in germanium device fabrication. Cyclical HF cleaning and $NH_3$-based SN treatment lead to significant improved device performance. By successfully forming a $GeO_xN_y$ layer, SN treatment effectively suppresses the surface reactions and Ge diffusion into the dielectric layer, causing reduced EOT, $J_g$, $D_{it}$ and trap density. PDA effect and $I$-$V$ conduction mechanism are also investigated. Based on the cyclical HF cleaning and SN treatment, excellent performance of germanium p-MOSFETs incorporated with CVD $HfO_2$ dielectric and TaN gate has been demonstrated. Compared to silicon control devices, 1.4-1.8X enhancement in hole mobility has been achieved.

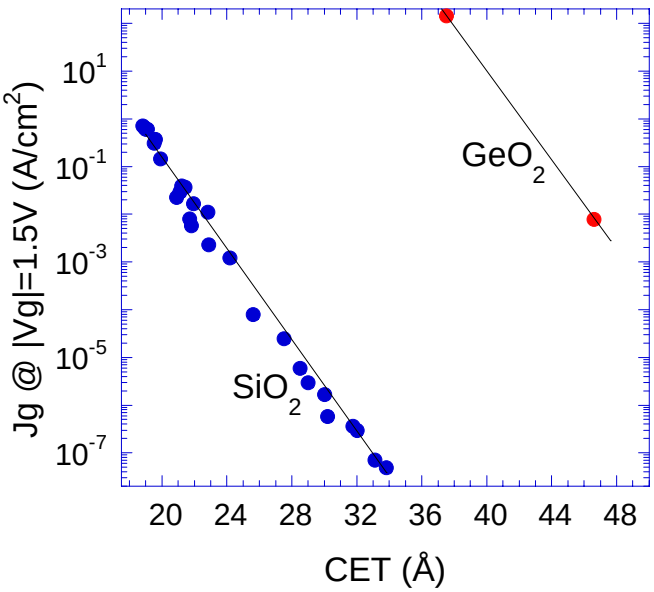
| Pre-cleaning | HF dip | $H_2O_2$+HF | Cyclical HF |
|---|---|---|---|
| Method | 1:5 HF solution ~ 5 min | $H_2O_2$ 2 min + 1:50 HF 3 min | 1:50 HF 15 sec + DIW 15 sec 5 cycles |
| surface AFM | many defect points | RMS = 2.94Å | RMS = 0.76Å |
| Electrical result | high leakage | high leakage | low leakage |

Table 3.1 Comparison of Ge surface cleaning methods




(a) (b)

Fig. 3.1 (a) *C-V* and (b) *I-V* characteristics of thermally grown $GeO_2$ passivated Ge MOS capacitors

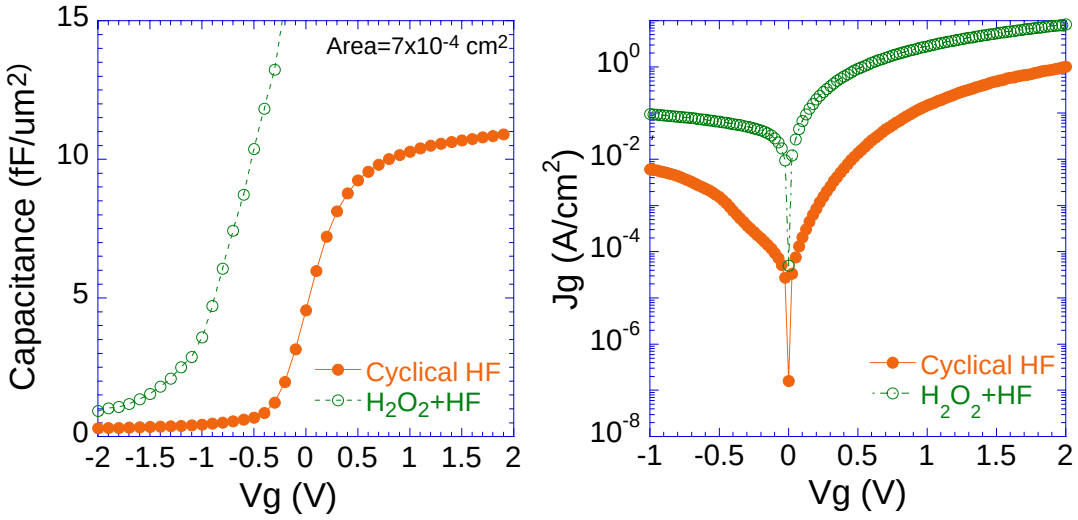



(a)

| Properties | $GeO_2$ | $SiO_2$ |
|---|---|---|
| ε | 5.2 | 3.9 |
| $E_g$ (eV) | 3.98 | 9 |
| $\Delta E_c$ (eV) | 1.4 | 3.5 |

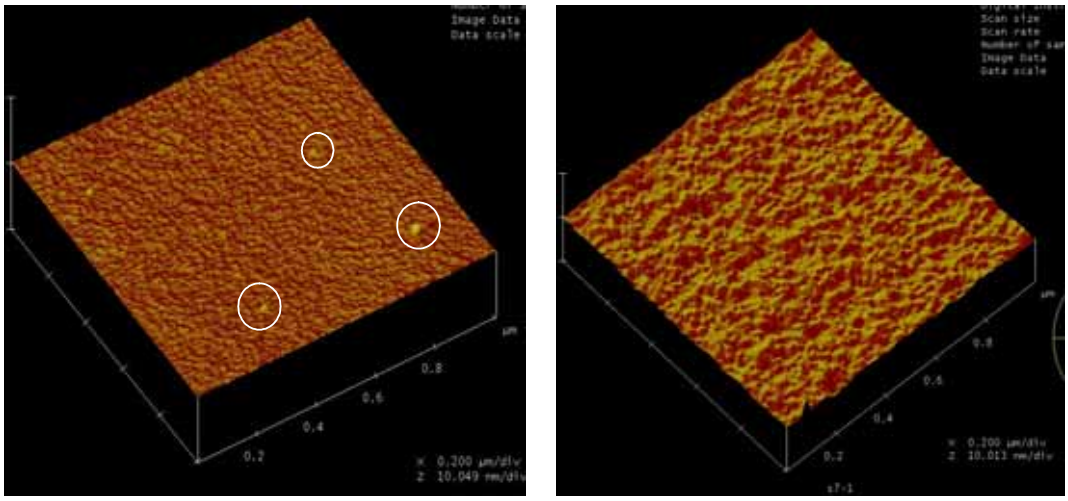
(b)

Fig. 3.2 (a) $J_g$ @ $V_g$ = 1.5 V as a function of CET and (b) physical properties of $SiO_2$ and $GeO_2$ gate dielectrics

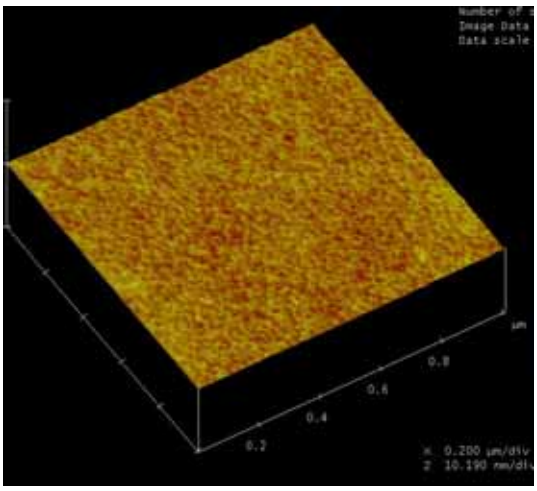



(a) (b)

Fig. 3.3 (a) *C-V* and (b) *I-V* characteristics of TaN/$HfO_2$/n-Ge stacks with different precleaning methods

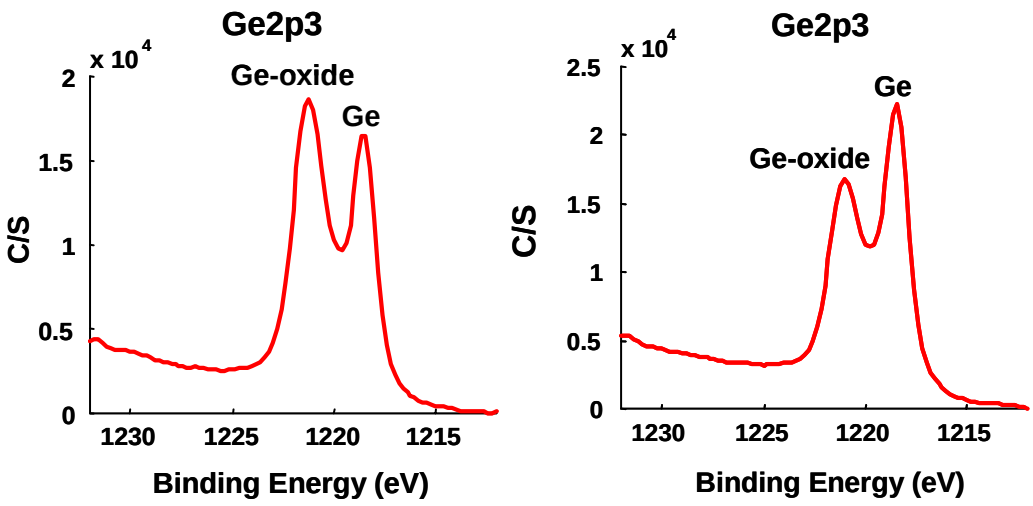


(a) (b)



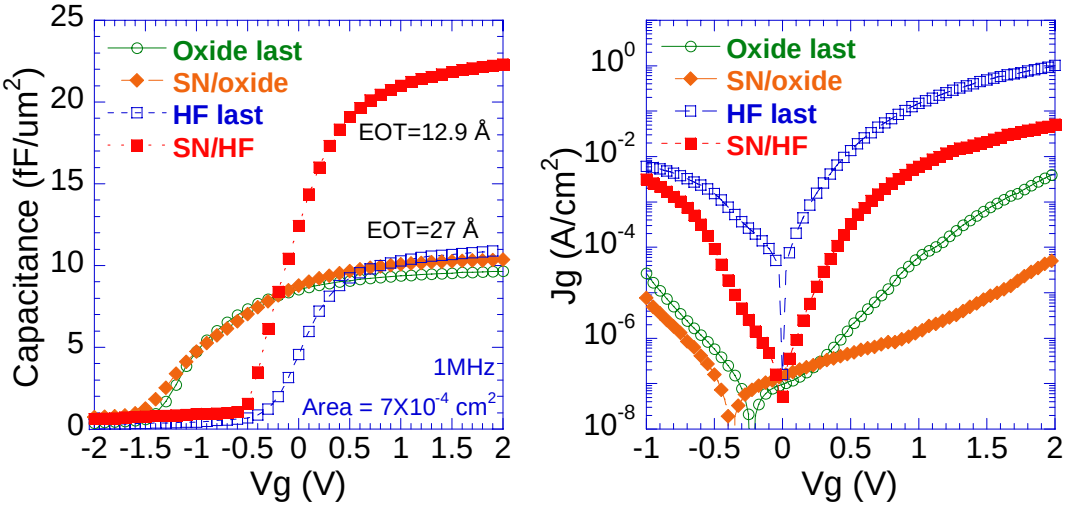
(c)

Fig. 3.4 AFM images of Ge surfaces after precleaning: (a) HF (1:5) dip; (b) $H_2O_2$+HF dip; and (c) cyclical HF cleaning




(a) (b)

Fig. 3.5 *Ex situ* XPS spectra of (a) uncleaned Ge substrate and (b) cyclical HF cleaned Ge substrate (exposed in air for two days)




(a) (b)

Fig. 3.6 (a) *C-V* and (b) *I-V* characteristics of TaN/HfO2/n-Ge stacks with and without precleaning and/or SN treatment

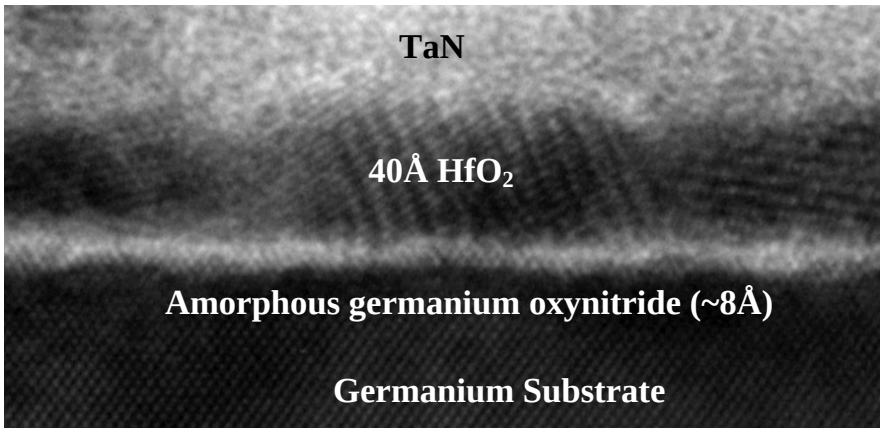



Fig. 3.7 XTEM image of TaN/$HfO_2$/n-Ge stack with precleaning and SN treatment prior to $HfO_2$ deposition. $NH_3$ annealing was carried out at 500°C for 2 min.

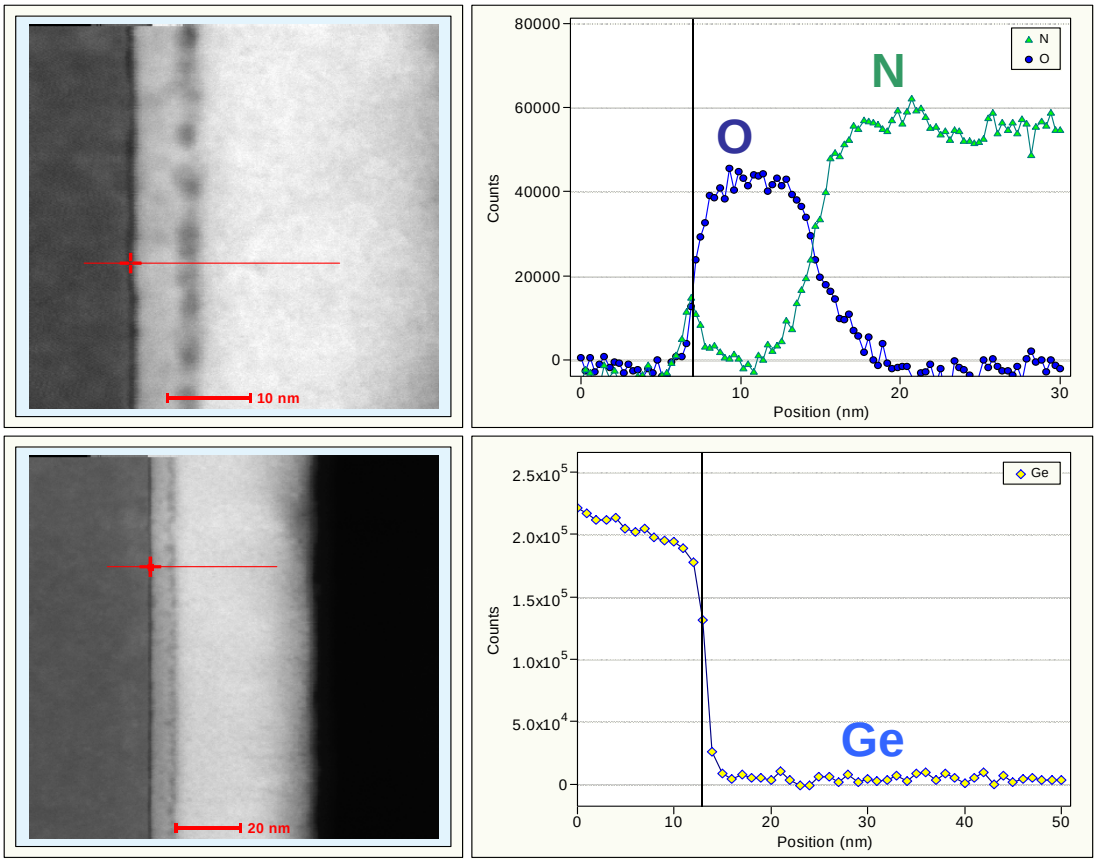
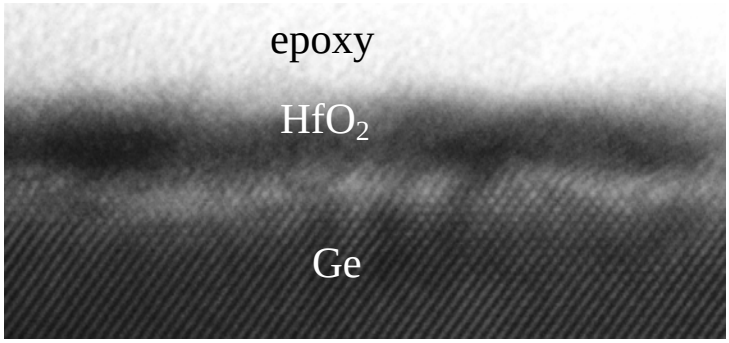
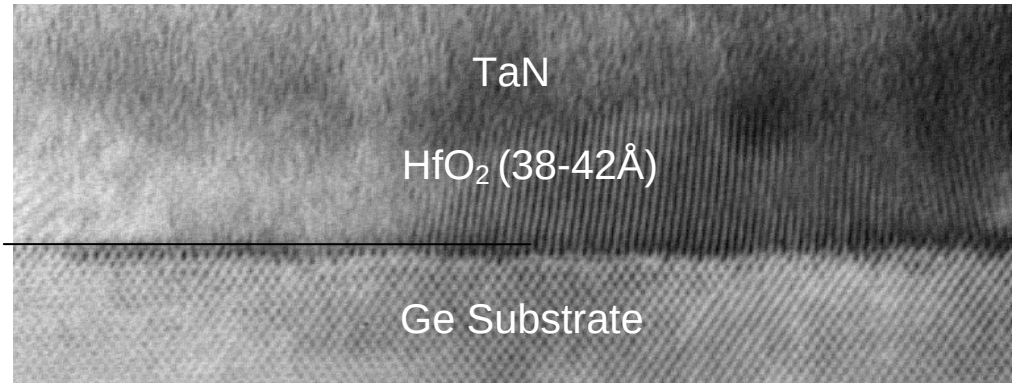



Fig. 3.8 EELS spectra of TaN/$HfO_2$/n-Ge stack with precleaning and SN treatment prior to $HfO_2$ deposition




(a)




(b)

Fig. 3.9 XTEM images of TaN/$HfO_2$/n-Ge stacks (a) on HF-last surface and (b) on oxide surface

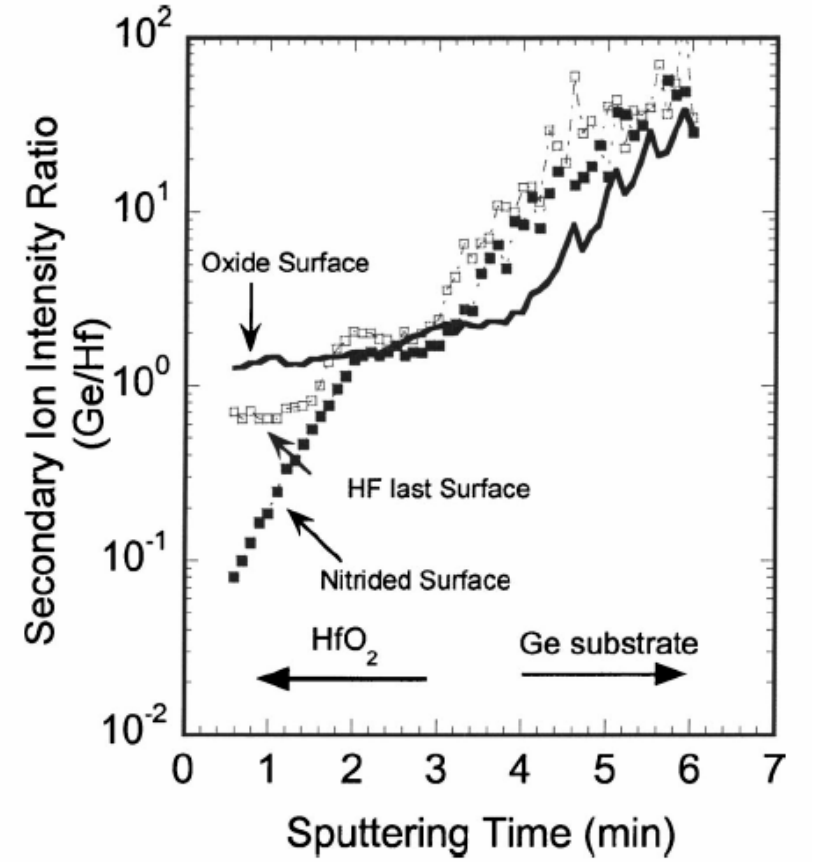



Fig. 3.10 Ge/Hf ratio in TaN/$HfO_2$/n-Ge stacks with different surface treatment conditions, measured by Quad-SIMS

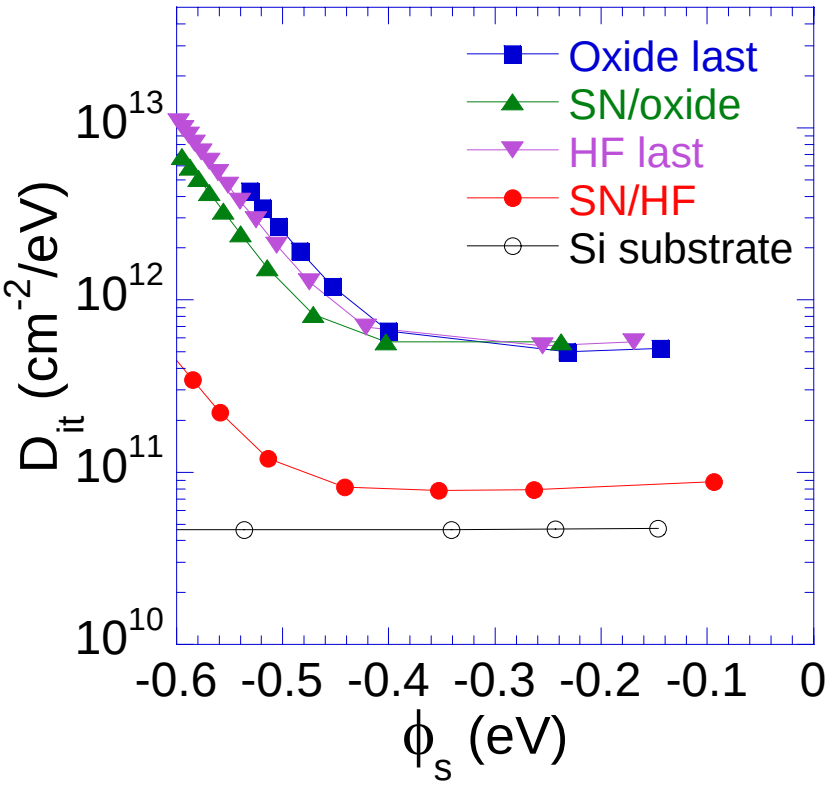



Fig. 3.11 $D_{it}$ of TaN/$HfO_2$/n-Ge MOS devices with different surface treatment conditions, extracted by Terman method from high frequency *C-V*s

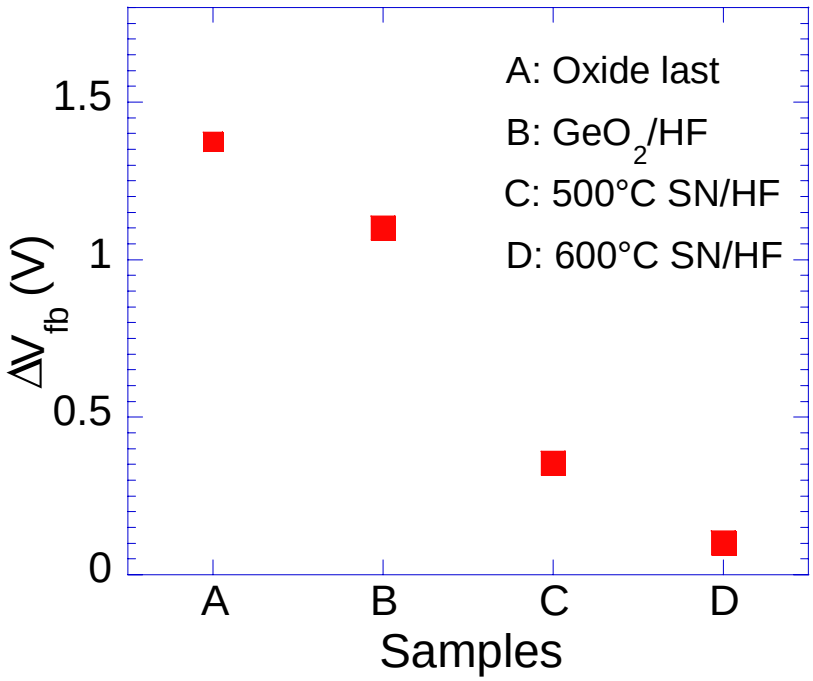



Fig. 3.12 *C-V* hysteresis characteristics of TaN/$HfO_2$/n-Ge MOS devices with different surface treatment conditions: A: oxide-last; C: 500°C SN/HF; D: 600°C SN/HF; and B: *C-V* hysteresis of TaN/$GeO_2$/n-Ge MOS devices with precleaning. $GeO_2$ was thermally grown in oxygen ambient at 500°C for 2 min.

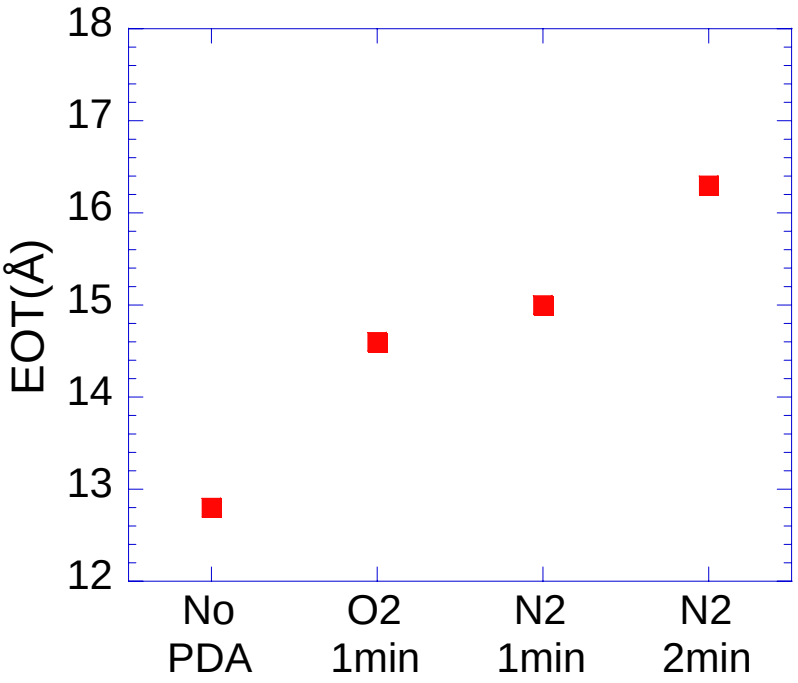
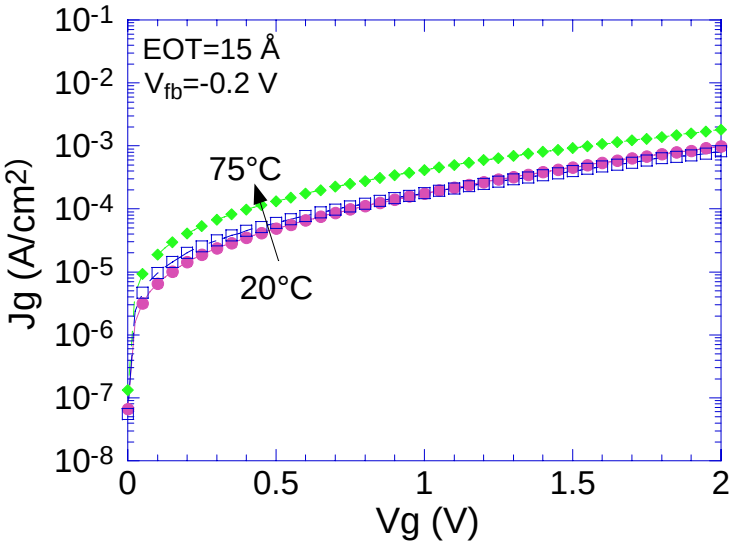
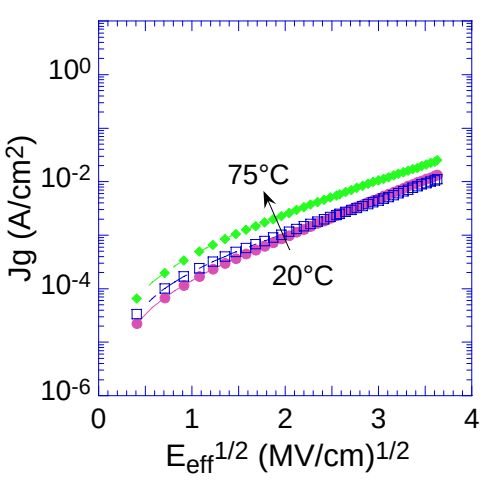


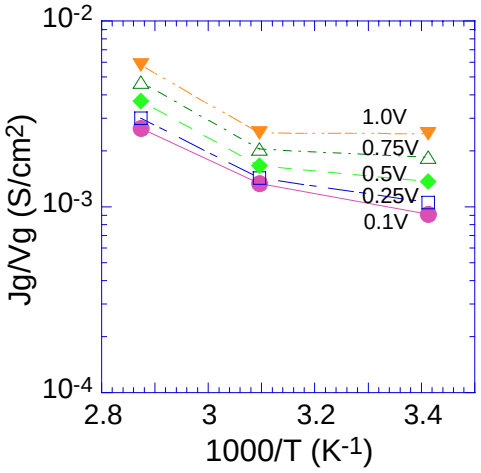

Fig. 3.13 EOT values as a function of PDA condition for TaN/$HfO_2$/n-Ge MOS devices with precleaning and SN treatment




(a)

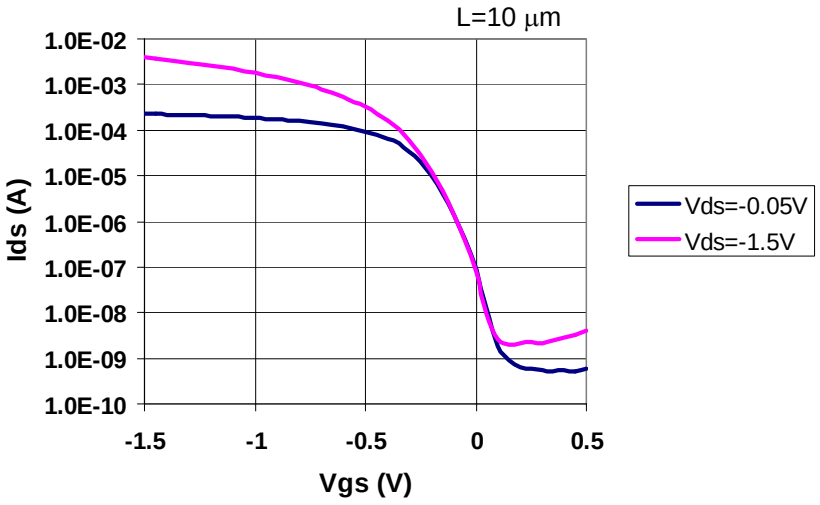



(b)

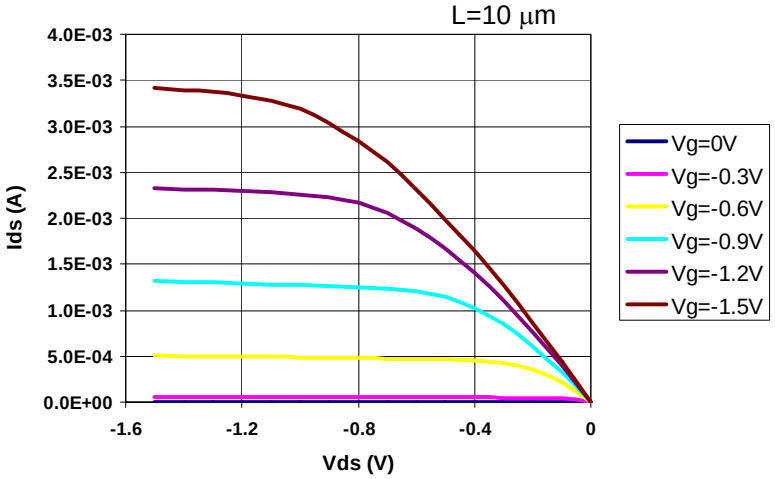



(c)

Fig. 3.14 (a) Temperature dependence of *I-V* characteristics of TaN/$HfO_2$/n-Ge MOS device; (b) log($J_g$)-$V_g^{1/2}$ and (c) log($J_g$/$V_g$)-1000/$T$ plots for the Ge p-MOS devices




(a)




(b)

Fig. 3.15 (a) $I_d$-$V_g$ and (b) $I_d$-$V_d$ characteristics for Ge p-MOSFET devices

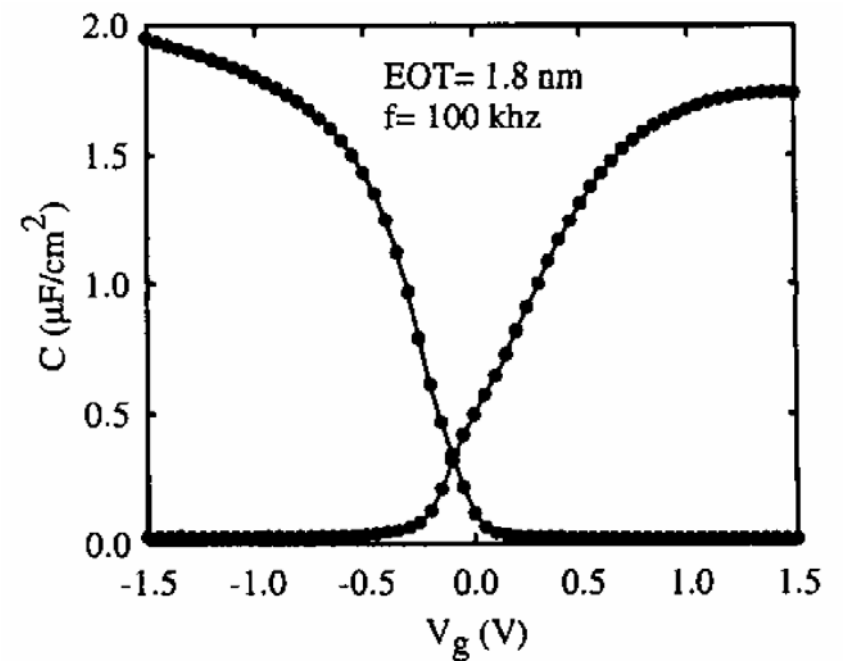



Fig. 3.16 Split *C-V* characteristics for Ge p-MOSFET devices

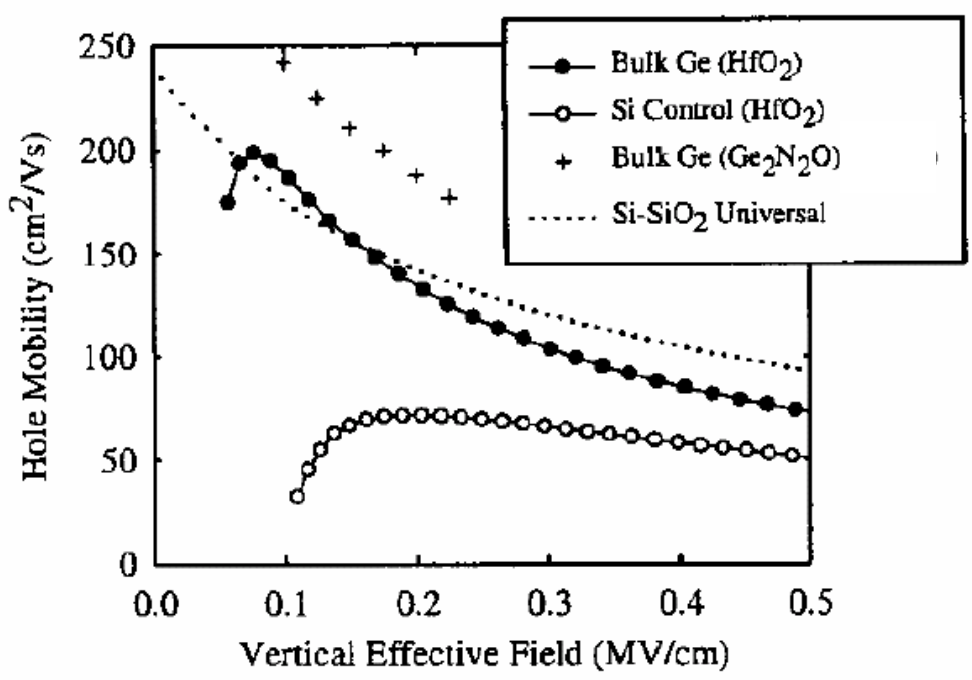



Fig. 3.17 Comparison of extracted channel mobilities for Ge and Si control p-MOSFETs. The Ge devices show 1.4-1.8X enhancement compared to the silicon control. Si-$SiO_2$ universal curve and data from Ref. [49] (Ge p-MOSFETs with germanium oxynitride gate dielectric) have been included for reference.

# Chapter 4: *In situ* cleaning effect and silicon interlayer passivation

## 4.1 INTRODUCTION

In the previous chapter, we have demonstrated that $NH_3$-based surface nitridation treatment is an effective passivation technique to form a more stable and better quality $GeO_xN_y$ interfacial layer. Enhanced channel mobility of high-κ/Ge over high-κ/Si system has been achieved. But the nitrogen incorporation may be not sufficient to fully passivate the dangling bonds on Ge surface and it also induces positive fixed charges. Considering the 4X higher hole mobility in bulk Ge than in Si, there must still be room to promote the channel mobility of Ge MOSFETs by improving the interface quality.

In order to further improve germanium MOS interface quality and passivate germanium surface, in this chapter we will discuss two surface passivation techniques for germanium device fabrication: *in situ* cleaning technique and silicon interlayer (SiIL) passivation.

## 4.2. IN SITU CLEANING TECHNIQUE BY ARGON ANNEAL

Since native $GeO_x$ is formed immediately after wet chemical precleaning [58], *in situ* surface cleaning is possibly helpful to remove the residual oxide and to form a better interface. It has been reported that germanium oxide can be removed by thermal desorption/decomposition in ultrahigh vacuum at a temperature above 390°C and which has already been used as an *in situ* germanium surface cleaning method

[59][60][61]. In this experiment, after wet cleaning and drying, the wafers were loaded in the chamber immediately. Then an *in situ* germanium surface cleaning by annealing the germanium substrates at 550°C for 60 sec in argon (Ar) gas was performed before $NH_3$-based SN treatment and CVD $HfO_2$ deposition. For comparison, the samples without Ar treatment and/or without SN treatment were also prepared.

The EOT values and $J_g$ @ $V_g$ = 1 V data as a function of the surface treatment condition are summarized in Fig. 4.1. The oxide cleaning effect can be observed apparently from the non-SN-treated samples. With Ar anneal, about 3 Å thinner EOT and more than one order of magnitude lower $J_g$ have been achieved. It is known that depositing high-κ dielectrics on HF-last Ge substrates forms thinner interfacial layers but larger EOTs than on SN-treated Ge substrates [51][52][62]. This is attributed to the desorption of volatile GeO or Hf-Ge-O species and Ge updiffusion into the dielectric during the deposition, which degrades the dielectric constant of high-κ layer and causes the film leaky due to the traps introduced [52][62]. We have also found that more germanium oxide on the surface led to more Ge diffusion into the dielectric. With the thermal annealing in the inert gas prior to the CVD process, the native germanium oxide, which is quickly formed after wet cleaning, is thermally desorbed. Therefore less GeO desorption and less Ge incorporation into the high-κ dielectric offer thinner EOT as compared to the devices without the *in situ* cleaning. The reduced leakage current may not only be resulting from the suppressed GeO desorption. It has been observed that poor surface conditions, such as surface defects or rough surface caused by improper precleaning methods like high-concentration

HF dip or $H_2O_2$+HF (as demonstrated in the last chapter) lead to severe degradation of *C-V* and dramatic increase of gate leakage (see Fig. 3.3). Noting the crucial role of substrate surface condition, we believe that the improved surface condition after removing the residual oxide may also contribute to the reduction of the gate leakage.

The samples with SN treatment exhibit reduced EOT and $J_g$ due to the formation of a $GeO_xN_y$ interfacial layer, which effectively blocks the formation of germanium oxide and the inter-diffusion across the interface. Because of the residual oxygen inside the chamber and also in the $NH_3$ gas [51], incorporation of oxygen into the interface is inevitable. As displayed in Fig. 4.2, 0.4-0.5 nm interfacial layer is observed from the cross-sectional transmission electron microscopy (XTEM) picture and the physical thickness of $HfO_2$ layer is ~ 4 nm. Combining with the EOT value (~ 1.0 nm), the dielectric constant of $HfO_2$ is determined around 25, identical to that of $HfO_2$ films on Si substrates. From the viewpoint of EOT and $J_g$, Ar treatment seems having no significant influence on these SN-treated samples, implying that the thicknesses of the $GeO_xN_y$ interfacial layers are very similar. This can be attributed to the saturation of the surface nitridation process when the nitridation time is sufficiently long (2 min in this experiment).

*C-V* and *I-V* characteristics of the two SN-treated samples with or without Ar treatment are shown in Fig. 4.2. With Ar treatment, the *C-V* shifts 0.1 V negatively, indicating an increase of the positive fixed charges ($Q_f$) of $1.7\times10^{12}$ $cm^{-2}$. The increase of $+Q_f$ is attributed to the increase of nitrogen component in the interfacial layer [51], resulting from the oxide removal effect by Ar anneal. *C-V* stretchout near the flatband voltage ($V_{fb}$) is improved, suggesting a reduction of the interface states

of $2.2\times10^{11}$ $cm^{-2}$ near the valence band edge. Both samples show identical *I-V* characteristics at the gate bias above 0 V. Note that the shifts of $J_g$ minima from zero bias are different, suggesting different trapping/detrapping properties [63]. To further investigate this phenomenon, the slow trap density ($D_{st}$) was estimated using the dynamic *I-V* technique [64][65][66]. By this technique, $D_{st}$ with response time at milliseconds can be estimated. Fig. 4.3(a) shows $D_{st}$ as a function of the gate voltage. No remarkable peaks are observed, suggesting an even distribution of the traps in the energy bandgap. $D_{st}$ as a function of the trap response time is shown in Fig. 4.3(b). Ar surface treatment results in more than 50% reduction of $D_{st}$, which is also confirmed by the *C-V* hysteresis data ($\Delta V_{fb}$: 0.06 V with Ar treatment versus 0.09 V without Ar treatment for a voltage sweep range from −1 V to 1 V). Similar time constants ($t_0 \propto D_{st0}\ R$) mean larger average resistance ($R$) to charge the traps for the Ar treated sample since its $D_{st0}$ is smaller. In other words, Ar treatment mainly reduces the traps near the interface and thus causes the average location of the traps farther away from the substrate. The above results reflect improved interface quality, which is contributed to the suppressed GeO desorption during the growth of $GeO_xN_y$ interfacial layer.

### 4.3. SILICON INTERLAYER PASSIVATION

Silicon interlayer (SiIL) technique, with several monolayers of silicon grown between the dielectric and the substrate, has been applied on Ge [67][68], GaAs [69][70] and other compound semiconductors [71] to improve the interface quality. With even very thin silicon layer (≤ 1 monolayer) incorporated into high-κ/Ge

interface by $SiH_4$ surface annealing at 400°C, enhanced hole mobility has been reported recently [25][72]. In this section, we demonstrate the fabrication and characteristics of Ge MOS capacitors using Si interlayer technique with $NH_3$ surface treatment and rapid thermal CVD $HfO_2$ gate dielectric.

Silicon interlayer was deposited at 580°C using $SiH_4$ gas (5 sccm) diluted with Ar. The process pressure is 3 torr and the growth time is 30 sec. Prior to $HfO_2$ dielectric deposition, rapid thermal annealing (RTA) in $NH_3$ ambient was performed at 550°C for 2 min in order to form a more stable interfacial layer and prevent the growth of interfacial oxide.

In order to take the advantage of the silicon interlayer, its thickness must be well controlled: it must be thick enough to remain at the interface despite the subsequent thermal processes, and on the other hand, it must be sufficiently thin to minimize the effect on channel transport and avoid defect generation during growth. The optimal thickness is several to a few monolayers [67][69]. The *ex situ* XPS spectra of $SiH_4$ treated samples are shown in Fig. 4.6. The spectra confirm the coverage of Si layer on Ge surface. The thickness of the Si layer was determined to be ~ 10 Å from the attenuation of the Ge peak intensity.

In Fig. 4.7, the measured high frequency (1 MHz) *C-V* (HFCV) and simulated low-frequency *C-V* (LFCV) are compared for Ge MOS capacitors with and without SiIL. Superior agreement between HFCV and LFCV is observed for the sample with SiIL, suggesting significant improvement in the interface quality. Using Terman method [55], excellent mid-gap $D_{it}$ of $7\times10^{10}$ /cm$^2$-eV has been extracted. The SiIL devices show higher EOT (12.4 Å) than the non-SiIL devices (9.8 Å),

which is due to the partial oxidation of the Si layer since the nitridation on Si layer is not as efficient as that on Ge surface at 550°C. The improved interface quality suggests the significant role of SiIL treatment. At first, terminating Ge surface with Si effectively passivates the dangling bonds on Ge surface due to their good bond matching by forming Si-Ge or Si-O-Ge bonds. Second, formation of the leaky and trap-filled Ge native oxides as well as the poor $GeO_x$/Ge interface has been prevented.

The *C-V* hysteresis behaviors are shown in Fig. 4.8. Large *C-V* hysteresis ($\Delta V_{fb}$ = 0.45 V) is observed for the non-SiIL devices. The hysteresis is mainly caused by the plasma induced oxide damage during PVD gate sputtering process, which could usually be eliminated by a high-temperature anneal at 800-900°C for Si devices [73]. To clarify this point, Ge MOS capacitors with identical $HfO_2$ process but with evaporated Al gate were fabricated. Al gated devices showed pretty small hysteresis ($\Delta V_{fb}$ = 0.1 V) as compared with the PVD TaN gated devices (Fig. 4.8), confirming that the TaN sputtering process is the main source of the hysteresis. The large EOT of Al gated devices is attributed to the formation of $Al_xO_y$ interfacial layer on the Al/$HfO_2$ interface [74]. The SiIL significantly reduces the hysteresis ($\Delta V_{fb}$ = 0.15 V) for the TaN gated samples, suggesting that most of the hysteresis is caused by the damage-induced traps near the $HfO_2$/Ge interface and Si interlayer can effectively immunize the interface against the damages. Another evidence for this point can be found from an experiment on silicon devices. As in Fig. 4.9, the hysteresis values ($\Delta V_{fb}$) of the TaN gated Si MOS capacitors with thermally grown $SiO_2$ dielectric are shown as a function of the $SiO_2$ layers' thickness (i.e., EOT).

With the thickness of the dielectric layer increasing, the hysteresis decreases. Note that

$$\Delta V_{fb} = q\, N_{trap} / C_{ox} \approx q\, N_{trap}\, \mathrm{EOT} / \varepsilon_{ox}, \tag{4.1}$$

where $N_{trap}$ is the trap density related to hysteresis, $C_{ox}$ is the oxide capacitance and $\varepsilon_{ox}$ is the dielectric constant of the oxide. If the hysteresis is caused by the traps in the dielectric layer, $\Delta V_{fb}$ should increase with the thickness of the oxide layer increasing ($\Delta V_{fb} \propto \mathrm{EOT}^2$ considering $N_{trap} \propto \mathrm{EOT}$). Therefore, the hysteresis must mostly come from the interface. And the induced traps by the plasma damages increases dramatically with the barrier's (i.e., the dielectric layer's) thickness decreasing.

Frequency dispersion characteristics are shown in Fig. 4.10. Without SiIL passivation, the 10 KHz *C-V* exhibits low-frequency behavior. This may be due to i) fast minority carrier generation in Ge resulting from a smaller band gap and ii) surface recombination processes with surface traps. The trap-induced recombination processes might be alleviated by SiIL with reduced surface traps. The kinks in the depletion region at lower frequency indicate that there still existed some "slow" interface traps near Ge substrate [22]. $V_{fb}$ of the SiIL devices shifts positively (0.3 V shift), indicating the reduction of the fixed charges resulting from less nitrogen incorporation into the interface.

For the SiIL samples, $J_g$ at $V_g$ = 1 V is $5\times10^{-7}$ A/cm$^2$ with an EOT of 12.4 Å. For the non-SiIL samples, $J_g$ is $5\times10^{-5}$ A/cm$^2$ with an EOT of 9.8 Å. About six orders

of magnitude lower gate leakage has been achieved for both devices compared with that of $SiO_2$ with the same EOT.

### 4.4. SUMMARY

In this chapter we have discussed two surface treatment techniques for germanium devices: *in situ* cleaning technique by Ar anneal and silicon interlayer passivation. By effectively removing the residual native oxide formed after wet cleaning, *in situ* cleaning suppresses the desorption of GeO in the following SN treatment process. Both the interface state density and the slow trap density are reduced. Silicon interlayer passivation takes the advantage of a few monolayers of silicon between the dielectric and the germanium substrate. Benefiting from the good match to germanium and effective suppression of the germanium oxide formation, excellent interface quality has been achieved with $D_{it}$ around $7\times10^{10}$ /cm$^2$-eV. The silicon interlayer also immunizes the plasma damages to the interface caused by the gate electrode sputtering process and significantly reduces the *C*-*V* hysteresis.

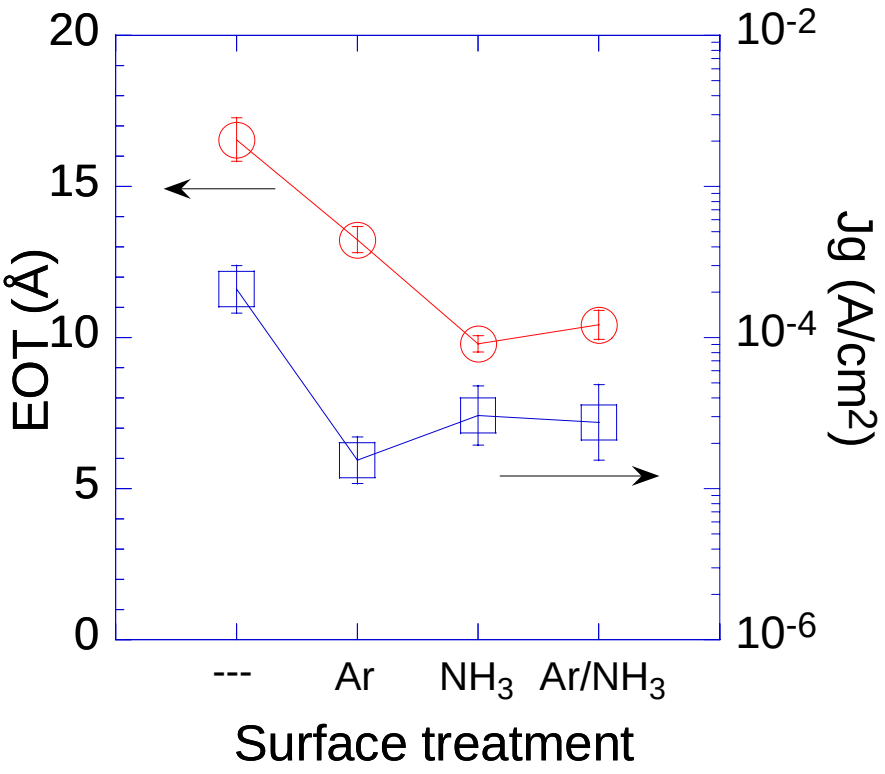



Fig. 4.1 EOT values and $J_g$ @ $V_g$ = 1 V data of the devices with different Ge surface treatments: ---: without any treatment; Ar: Ar treatment only; $NH_3$: $NH_3$ treatment only; and Ar/$NH_3$: with both Ar and $NH_3$ treatment.

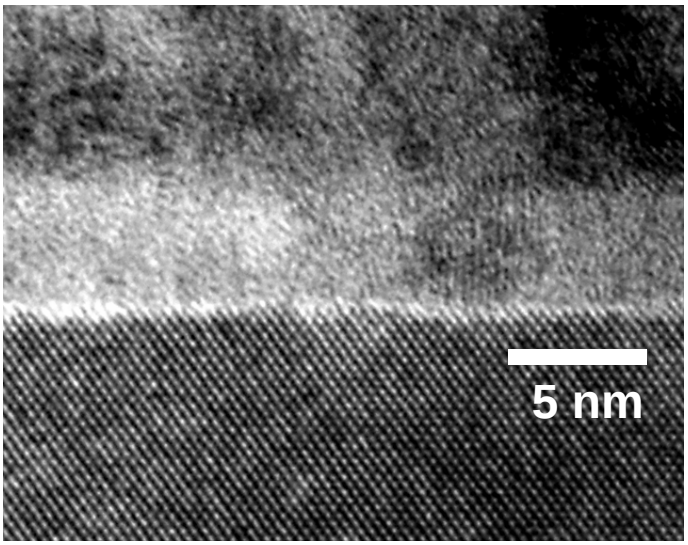



Fig. 4.2 XTEM image of $NH_3$/Ar-treated TaN/$HfO_2$/Ge stack

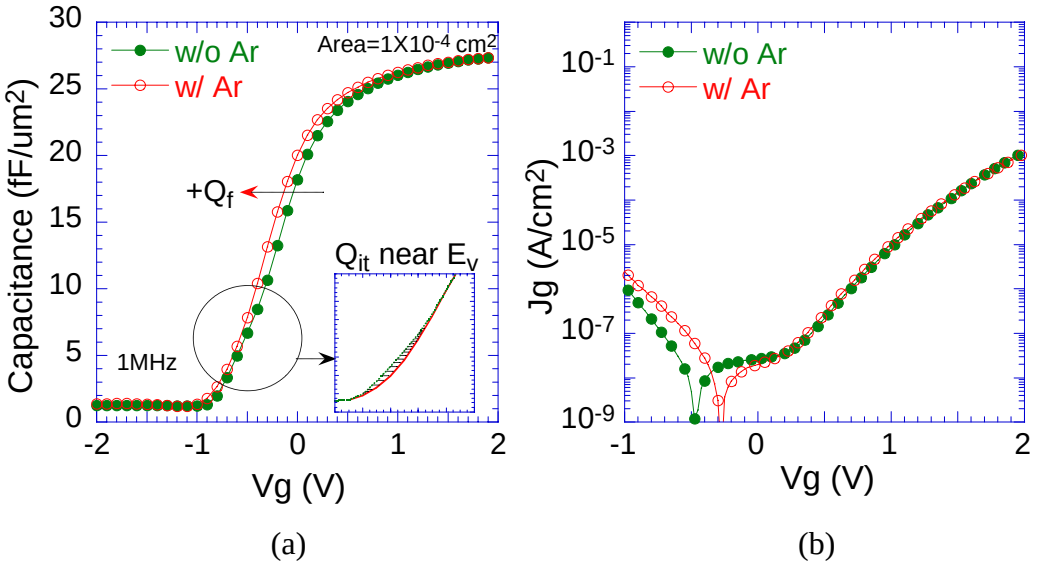



Fig. 4.3 (a) High-frequency *C-V* and (b) *I-V* characteristics of SN-treated devices with or without Ar treatment before SN. The stretchout near the flatband voltage is compared in detail in the inset of (a) by shifting the *C-V* of the Ar treated device +0.1 V. The reduction of $D_{it}$ was estimated by integrating the shadow area in the inset.

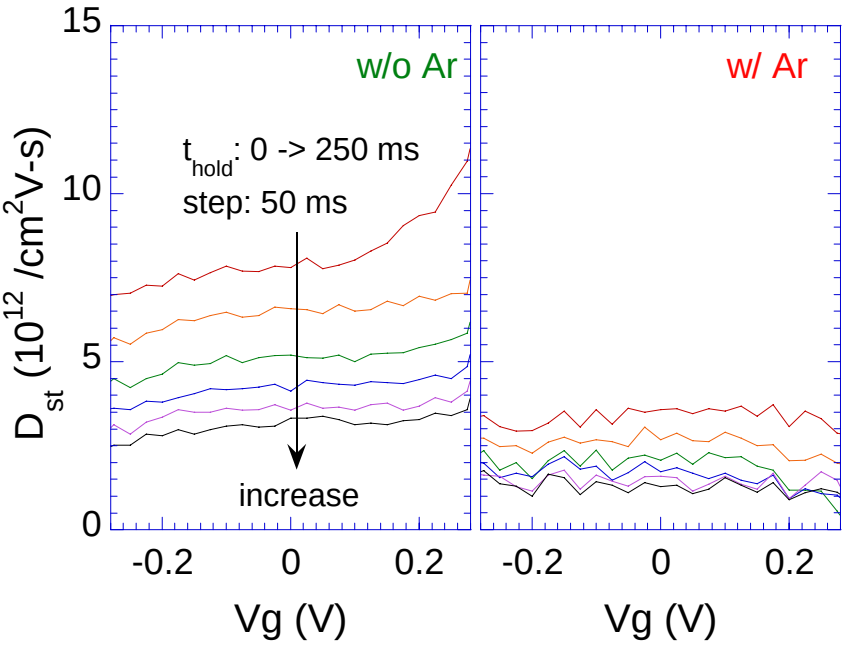



Fig. 4.4 Slow trap densities of the samples with (w/) and without (w/o) Ar treatment as a function of the gate voltage. SN treatment was done prior to $HfO_2$ deposition. The measurement holding time was taken from 0 to 250 ms with a step of 50 ms.

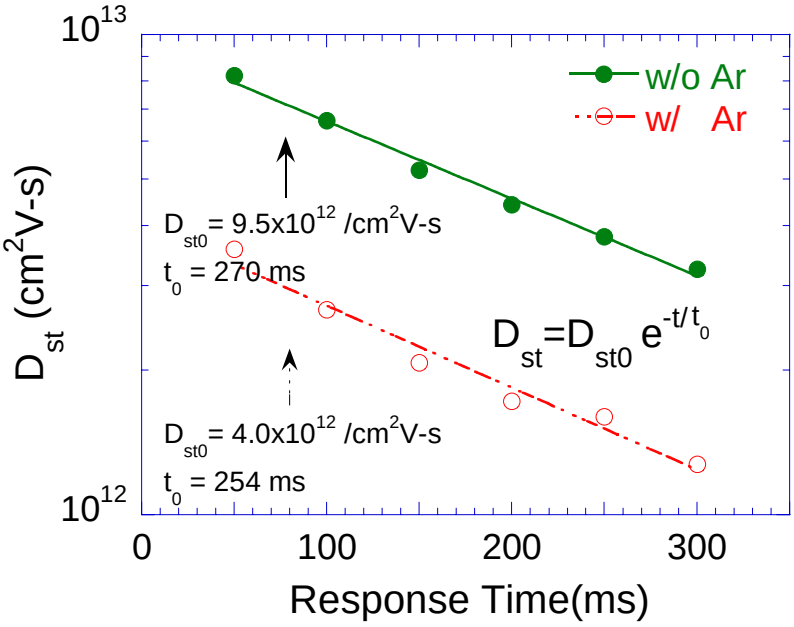



Fig. 4.5 Slow trap densities as a function of the trap response time, which equals to the sum of the measurement holding time and the setup time (~ 50 ms). The slow trap density values were taken at $V_g = 0$ V.

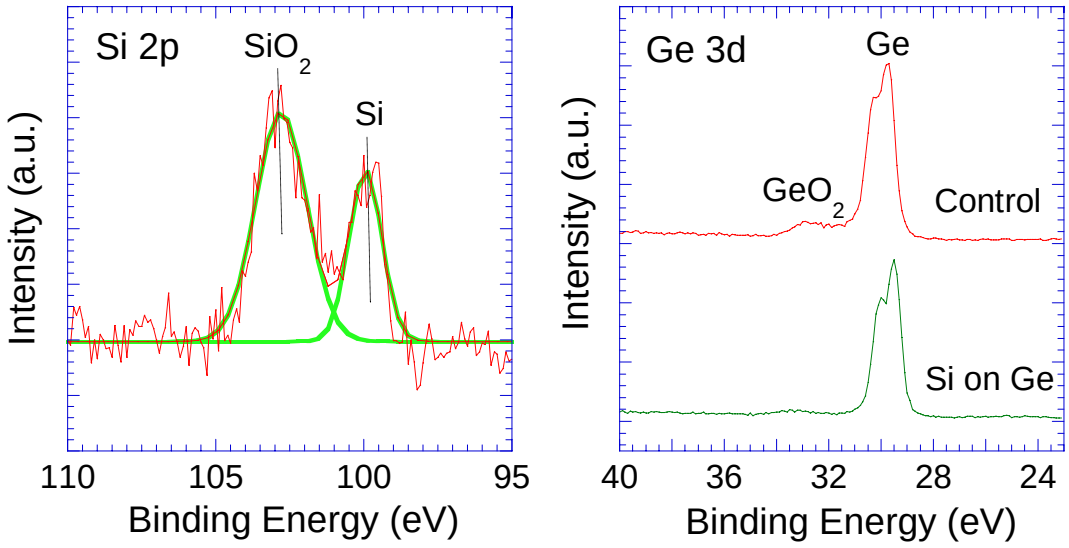



Fig. 4.6 XPS spectra of germanium surface with silicon interlayer deposited at 580°C with $SiH_4$ gas

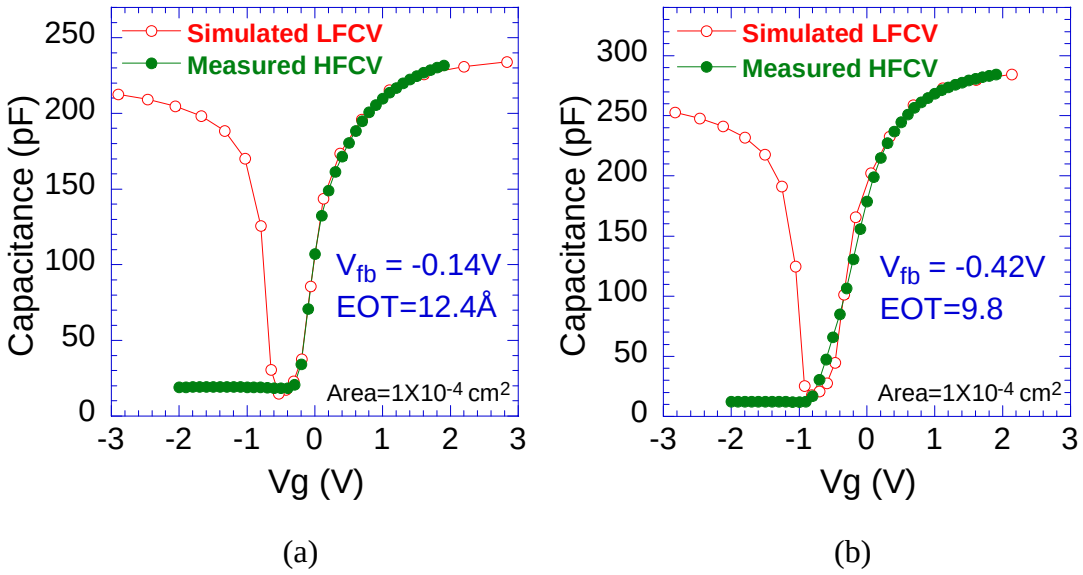



Fig. 4.7 Comparison of measured HFCV and simulated LFCV for both Ge MOS devices (a) with and (b) without Si interlayer passivation

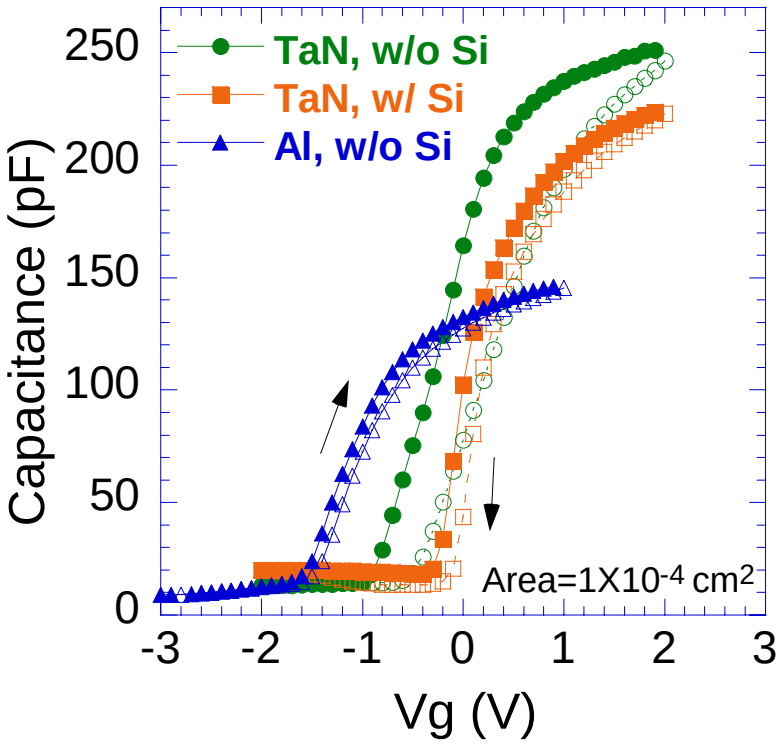



Fig. 4.8 *C-V* hysteresis characteristics for Ge MOS devices with and without Si interlayer passivation. The bias was swept from –2 V → 2 V → –2 V for TaN gated devices and from –3 V → 1 V → –3 V for Al gated devices.

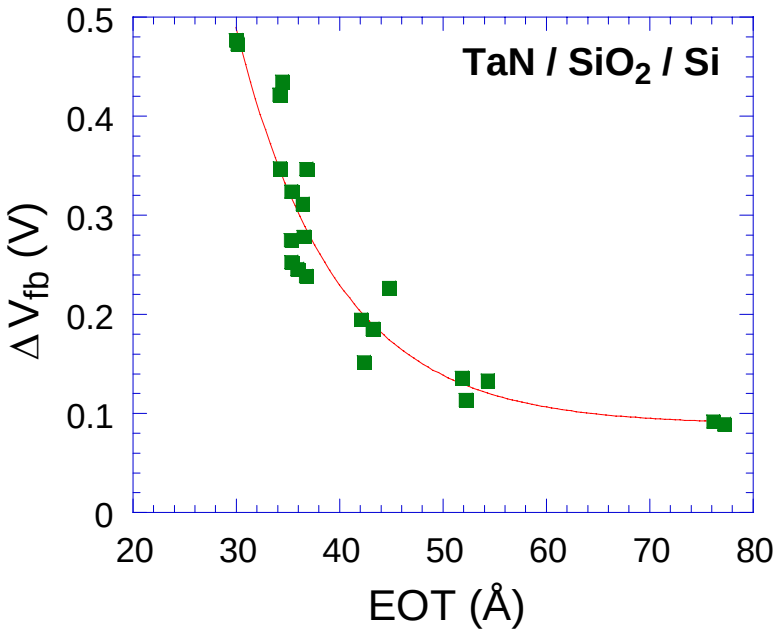



Fig. 4.9 *C-V* Hysteresis as a function of EOT for PVD TaN gated Si MOS devices with $SiO_2$ as the gate dielectric

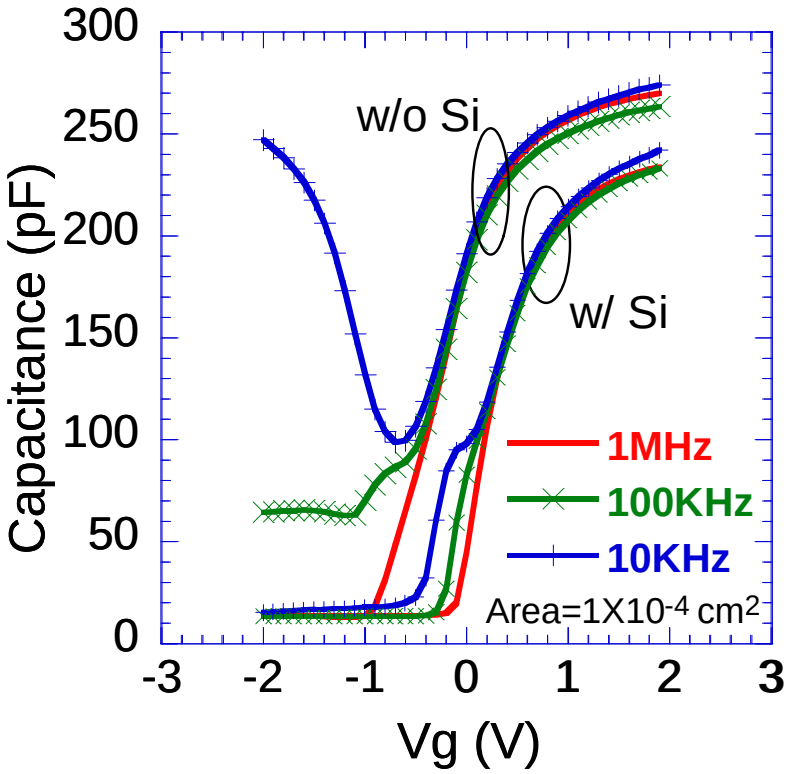



Fig. 4.10 Frequency dispersion behaviors (10 KHz - 1 MHz) for Ge MOS devices with and without Si interlayer passivation

# Chapter 5: Electrical properties of Ge n-MOSFETs

## 5.1 BACKGROUND

Promising results for bulk Ge p-channel MOSFETs with both high-κ dielectrics [22]-[26] and $GeO_xN_y$ dielectric [49] have been demonstrated, with 2X hole mobility enhancement. Germanium-on-insulator (GOI) devices also showed excellent performance [29]-[32][75][76] for both p-type and n-type. Enigmatically, bulk Ge n-channel MOSFETs exhibited very poor performance. The drive currents of n-type devices were one to two orders lower than those of their p-type counterparts [23][77][78], even through the fabrication processes were almost identical [22][23][49]. Recently, improved characteristics of bulk Ge n-MOSFETs were reported, with plasma-$PH_3$ treatment or AlN surface passivation [26]. However the cause for the poor performance of n-channel devices has not been clarified yet. In this chapter, a successful fabrication of Ge n-MOSFETs on lightly doped ($\leq 1\times10^{15}$ $cm^{-3}$) substrates is demonstrated. The poor Ge n-MOSFETs characteristics reported before are discussed and the possible mechanism is suggested.

## 5.2 ELECTRICAL PROPERTIES OF BULK GERMANIUM N-MOSFETS ON LIGHTLY DOPED SUBSTRATES

### 5.2.1 Fabrication

MOSFETs were fabricated on (100) oriented p-type Ge substrates (Ga, $\rho > 3$ ohm-cm). Ge wafers were precleaned using cyclical HF dip method. Rapid thermal $NH_3$ anneal was performed at 450°C or 550°C for 2 min for SN treatment. 5 nm

$HfO_2$ film was then *in situ* deposited at 400°C by rapid thermal CVD using the hafnium-t-butoxide precursor ($Hf(OC_4H_9)_4$) either with or without the introduction of $O_2$. Note that the precursor can release oxygen itself when dissolving at high temperature and the introduction of $O_2$ to react with the precursor is not a requirement for this CVD $HfO_2$ growth. The experiments based on Si have shown similar $HfO_2$ quality for both conditions. 1500 Å TaN was reactively sputtered as the top electrode layer. Ring-type transistor structures were used. After gate patterning, $1\times10^{15}$ $cm^{-2}$ As was implanted at 40 KeV [79], followed by 500°C 5 min source/drain (S/D) activation in a forming gas furnace. 200 nm Al was sputtered on both the frontside and the backside of the wafers for metallization. Finally, 300°C anneal was performed in forming gas for 30min after S/D metal pattering. In addition, Ge n-MOS capacitors on highly doped Ge p-substrates ($N_a = 4\times10^{17}$ $cm^{-3}$ and $3\times10^{18}$ $cm^{-3}$) were also fabricated.

Si control devices were fabricated for comparison. To achieve effective surface nitridation, $NH_3$ anneal for Si devices was carried out at 700°C for 10 sec. S/D activation anneal was performed at 900°C for 30 sec.

### 5.2.2 Electrical properties

The typical transistor characteristics of the germanium n-MOSFET devices are displayed in Fig. 5.1. The gate stack growth condition for these devices was non-$O_2$ $HfO_2$ deposition with a 550°C SN treatment. Fig. 5.1(a) shows $I_d$-$V_g$ and transconductance ($G_m$)-$V_g$ characteristics. The off-current ($I_{off}$) is found about two orders of magnitude lower than the on-current ($I_{on}$), which is due to the low substrate

doping level and the narrow bandgap of germanium. Well-behaved $I_d$-$V_d$ characteristics are shown in Fig. 5.1(b). Fig. 5.2(a) shows the split *C*-*V* characteristics. 10.8 Å EOT was extracted from the inversion *C*-*V* measurement considering the quantum mechanical effect [45]. The capacitance increase on the accumulation *C*-*V* at $V_g > 0.1$ V and on the inversion *C*-*V* at $V_g < -0.2$ V is caused by the narrow bandgap of germanium and the lightly doped substrate, which make the p-n junction between S/D and channel more conducting under reverse bias. *I*-*V* characteristics (Fig. 5.2(b)) demonstrate extremely low leakage current of 0.64 mA/cm$^2$ at −2 V. The non-zero $J_g$ at zero $V_g$ is due to trapping/detrapping current and/or dielectric relaxation current [63]. The dependence of the peak transconductance ($G_{m\text{-}peak}$) and $I_d$ at $V_g$ = 2 V on the channel length ($L$) of these devices is shown in Fig. 5.3. In linear region,

$$V_d / I_{d\text{-}measured} = R_{tot} = R_s + L \cdot [V_d / (W \cdot I_{d\text{-}ideal})], \quad (5.1)$$

where $R_{tot}$ is the total resistance, $R_s$ is the S/D series resistance, $W$ is the channel width, $I_{d\text{-}measured}$ is the measured drain current, and $I_{d\text{-}ideal}$ is the ideal (non-$R_s$) drain current per square. The intercepts on y-axis of Fig. 5.3 indicate significant $R_s$, which is possibly caused by insufficient implantation dose and/or poor ion activation at 500°C. To accurately calculate the electron mobility ($\mu_{eff}$), $I_{d\text{-}ideal}$ was extracted by

$$(W / L)\, I_{d\text{-}ideal} = I_{d\text{-}measured} \cdot [R_{tot} / (R_{tot} - R_s)]. \quad (5.2)$$

The mobility was extracted by using $I_{\text{d-ideal}}$-$V_{\text{g}}$ data and the integrated inversion charge ($Q_{\text{inv}}$) (obtained from split *C-V* measurements). The effective vertical field ($E_{\text{eff}}$) was calculated from the expression [57]:

$$E_{\text{eff}} = \frac{1}{\varepsilon_{\text{Ge}}}\left(|Q_{\text{b}}| + \frac{|Q_{\text{inv}}|}{2}\right), \tag{5.3}$$

where $\varepsilon_{\text{Ge}}$ is the dielectric constant of Ge and $Q_{\text{b}}$ is the bulk depletion charge calculated from the body doping concentration. Electron mobility as a function of the effective field is shown in Fig. 5.4. Compared to Si control devices, 2.5X enhancement of peak mobility (330 $cm^2/V{\cdot}s$) was achieved for Ge n-MOSFETs.

### 5.2.3 The influence of surface treatment and dielectric deposition conditions on device performance

As mentioned in Section 5.2.1, several surface treatment and dielectric deposition conditions have been attempted. Results show that different conditions have significant influence on device performance. As shown in Fig. 5.5, the devices treated with higher temperature (550°C) $NH_3$ anneal and non-$O_2$ $HfO_2$ deposition exhibit the highest mobility (330 $cm^2/V{\cdot}s$). Deposition of $HfO_2$ with the introduction of $O_2$ degrades the channel transport characteristics with a peak mobility of 283 $cm^2/V{\cdot}s$. Devices with 450°C $NH_3$ treatment shows the worst peak mobility of 230 $cm^2/V{\cdot}s$. SN treatment at higher temperature and non-$O_2$ dielectric deposition form a more stable interfacial layer with more nitrogen and less oxygen incorporated [52][80]. This helps to prevent the formation of poor quality $GeO_x$ interlayer [37][81] and results in better channel transport characteristics.

## 5.3 ANALYSIS OF THE REPORTED POOR PERFORMANCE OF BULK GERMANIUM N-MOSFETS AND THE POSSIBLE MECHANISM

In Fig. 5.6, the normalized effective mobility in this work and the recently reported data of bulk germanium n-MOSFETs are compared. As clearly shown, the device performance is boosted dramatically in this work. However, the reason for those reported poor results has not been clarified yet. In Table 5.1 the key data and process conditions of bulk germanium MOSFETs in recent published papers for both n-type and p-type are summarized [22][23][25][26][77][78]. One noticeable fact is that the doping levels of the substrates used in p-MOSFET fabrications are at a range from $3\times10^{15}$ to $5\times10^{16}$ $cm^{-3}$. For those n-MOSFETs which exhibited poor performance, the substrate doping levels are above $2\times10^{17}$ $cm^{-3}$. Poor dopant activation and high S/D series resistance might be one possible reason since S/D activation might need different activation conditions for different types of substrates. However, the saturated drain voltage ($V_{dsat}$) is much less than the difference of the gate-source bias ($V_{gs}$) and the threshold voltage ($V_{th}$), as shown in $I_d$-$V_d$ plots in Fig. 5.7 [23][78], revealing the presence of severe channel carrier scattering instead of high S/D series resistance.

S. J. Whang et al. [26] reported improved characteristics of Ge n-MOSFETs. It is noticed that the p-substrates used in their experiment are with a doping concentration of $5\times10^{16}$ $cm^{-3}$. The saturated drive current of the n-MOSFETs is almost the same as the p-type counterparts, indicating the degradation in n-type

devices still exists. Significant improvements on both peak mobility and saturated drive current have been achieved in our experiments by using the substrate at lower doping level ($\leq 1\times10^{15}$ cm$^{-3}$). The substrate doping concentration seems to play a key role in the poor n-MOSFET performance reported recently. The much more severe degradation of drive currents with increased substrate doping, as compared with Si devices, indicates that other scattering mechanism exists in additional to the Coulomb scattering by ionic impurities.

Fig. 5.8 shows the typical high-frequency *C-V* and *I-V* characteristics of Ge n-MOS capacitors fabricated on two high doped p-substrates ($4\times10^{17}$ cm$^{-3}$ and $3\times10^{18}$ cm$^{-3}$) with identical process conditions. Their almost identical *I-V* characteristics indicate the same dielectric properties on both substrates. However, the devices fabricated on the substrate of $3\times10^{18}$ cm$^{-3}$ exhibit abnormal *C-V* characteristics, i.e., a low-frequency shape in the inversion region even at 1 MHz measurement frequency. In most semiconductors indirect recombination is the dominant recombination process [82]. The generation/recombination rate ($R$) is proportional to the doping concentration. Thus the *C-V* measurements in the inversion region should not depend on the bulk doping level according to the high/low *C-V* criterion [83], i.e.,

$$\begin{aligned} &\frac{1}{\sqrt{2}}\left(\frac{N_a}{n_i}\right)\varpi\tau >> 1 \text{ for high-frequency } C\text{-}V \\ &\frac{1}{\sqrt{2}}\left(\frac{N_a}{n_i}\right)\varpi\tau << 1 \text{ for low-frequency } C\text{-}V, \end{aligned} \tag{5.4}$$

where $N_a$ is the substrate doping concentration, $n_i$ is the intrinsic carrier concentration, $\tau$ is the minority carrier lifetime ($\tau = 1/R$), and $\varpi$ is the *C*-*V* measurement frequency. Therefore, there must be some other surface recombination processes that significantly reduce $\tau$ when the substrate doping level is sufficiently high. More discussions about the dependence of *C*-*V* shape on the substrate doping are presented in Section 6.5.

Fig. 5.9 compares the diffusion coefficients of several impurities in silicon and in germanium, including silicon and germanium's self diffusion coefficients. It shows that both impurity atoms and germanium atom itself have much higher diffusivity in germanium than in silicon. The diffusion coefficient of Ga in Ge is three orders of magnitude higher and the self-diffusion coefficient of Ge is five orders of magnitude higher than that in Si, respectively. Noting this property of germanium, a possible degradation mechanism is suggested that the highly doped Ga impurities may form diffusion-induced dislocations [84] or other structural defects near the substrate surface. These defects in turn enhance the atom diffusion and help to form more defects [85]. The dramatically increased defects near surface lead to severe additional scattering on the channel carriers and significantly reduce the carrier mobility. These surface defects can also act as the generation/recombination centers of minority carriers, enhancing surface recombination process and reducing the lifetime of minority carriers. Consequently minority carriers can response to small signals even at pretty high measurement frequency when the doping level is sufficiently high.

More investigations, especially physical characterization and evidence are needed for the detailed study on the mechanism.

## 5.4 SUMMMARY

In this chapter, the fabrication of bulk germanium n-MOSFETs on lightly doped substrates is introduced. Excellent characteristics have been demonstrated with 2.5X enhancement of peak electron mobility compared to silicon control devices. Different surface treatment and dielectric deposition conditions have significant influence on device performance and the non-$O_2$ $HfO_2$ deposition with higher temperature SN treatment offers the best result due to less oxygen incorporation into the interface. The reason for the significantly improved device performance in this work compared to the recently reported poor results of bulk germanium n-MOSFET has been investigated. It is found that the poor performance is correlated to the high doped substrates used in those experiments. The structural defects, which may form near germanium surface due to the high diffusivities of impurity and germanium atoms in germanium, are possibly responsible for the severe degradation of device performance.

| FET Type | $N_d/N_a$ ($cm^{-3}$) | Surface treatment | Dielectric | Gate | EOT (Å) | $I_{dsat}$ @ \|Vg-Vt\|~1.5V (μA/sqare) | Peak Mobility ($cm^2$/V-s) | Ref. |
|---|---|---|---|---|---|---|---|---|
| p | 5.5E15 | | GeON/LTO | Al | 80 | 40 | 310 | [49] |
| | 2E16 | $NH_3$ | CVD $HfO_2$ | TaN | 18 | 82 | 200 | [23] |
| | 1E16 | | UV ozone oxidized $ZrO_2$ | Pt | 19 | 92 | 313 | [22] |
| | 5E16 | $NH_3$ | CVD $HfO_2$ | TaN | 12.5 | 56 | 80 | [25] |
| | 5E16 | $SiH_4$ | CVD $HfO_2$ | TaN | 15.5 | 88 | 194 | [25] |
| | 3E15 | $PH_3$; AlN | CVD $HfO_2$ | TaN | 7.5 | 80 | 120 | [26] |
| | | | | | | | | |
| n | 5E17 | | GeON/LTO | W | 84 | 1.2 | | [78] |
| | 4E17 | $NH_3$ | CVD $HfO_2$ | TaN | 18 | 0.14 | | [23] |
| | 2E17 | $NH_3$ | ALD $ZrO_2$ or $HfO_2$ | Pt | 22.2 | 6.75/12.8 | | [77] |
| | 5E16 | $PH_3$; AlN | CVD $HfO_2$ | TaN | 7.5 | 85 | 300 | [26] |
| | ≤1E15 | $NH_3$ | CVD $HfO_2$ | TaN | 10.8 | 130 | 330 | # |

Table 5.1 Summary of bulk Ge p- and n- MOSFET results published recently. Note: # refers to this work; $N_a$ in [77] was estimated from the minimum capacitance in *C-V* measurements; EOT in [22][23][49][78] are CET data; $I_{dsat}$ in [23][26] are values at $|V_{gs}-V_t| = 1.2$ V. The recent results for GOI devices are not included for comparison because the surface doping levels of GOI substrates were unclear.

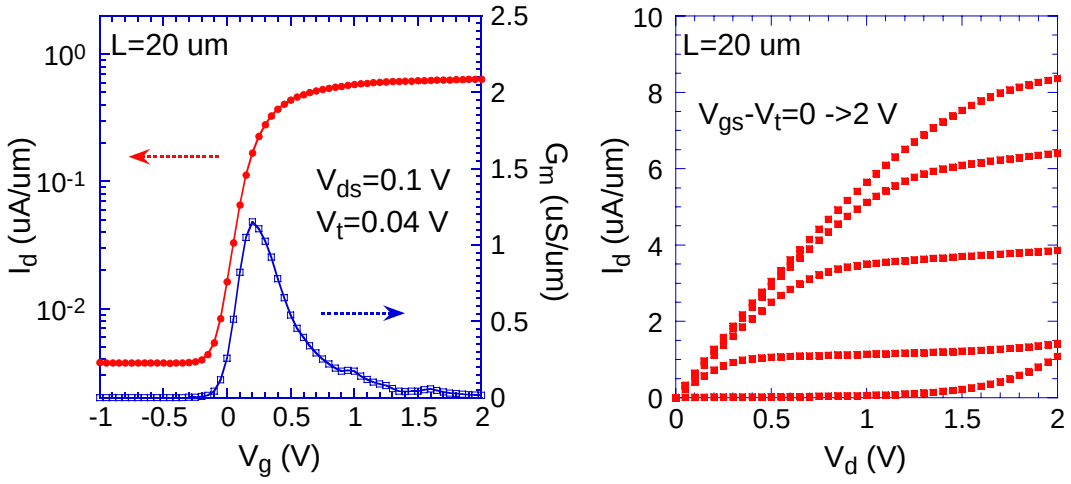
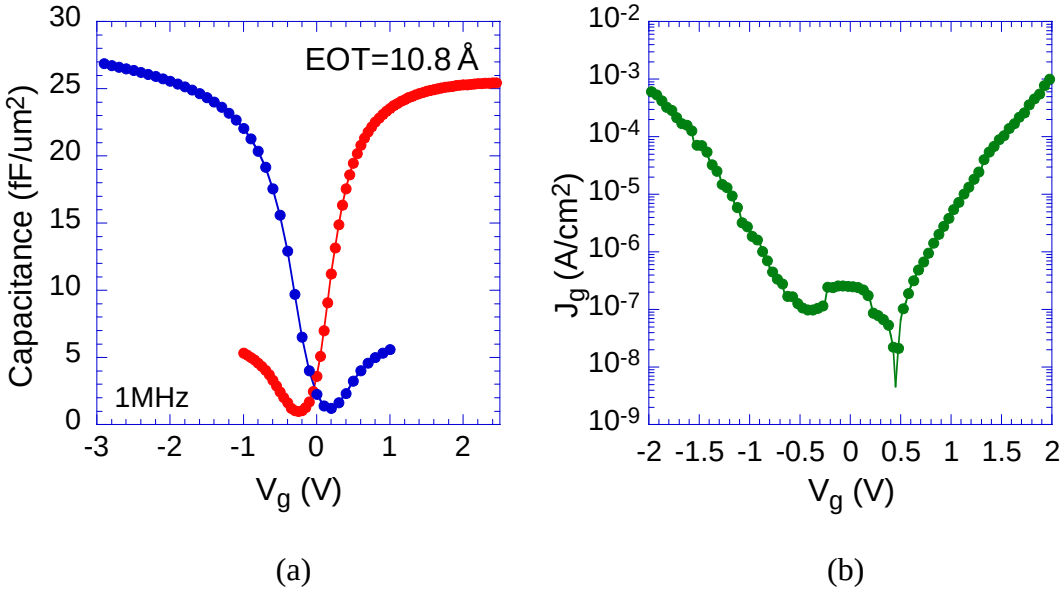



Fig. 5.1 (a) $I_d$-$V_g$, $G_m$-$V_g$ and (b) $I_d$-$V_d$ characteristics for Ge n-MOSFETs on lightly doped substrates with 550°C SN treatment and non-$O_2$ $HfO_2$ deposition




(a) (b)

Fig. 5.2 (a) Split *C-V* and (b) *I-V* characteristics for Ge n-MOSFETs on lightly doped substrates with 550°C $NH_3$ SN treatment and non-$O_2$ $HfO_2$ deposition

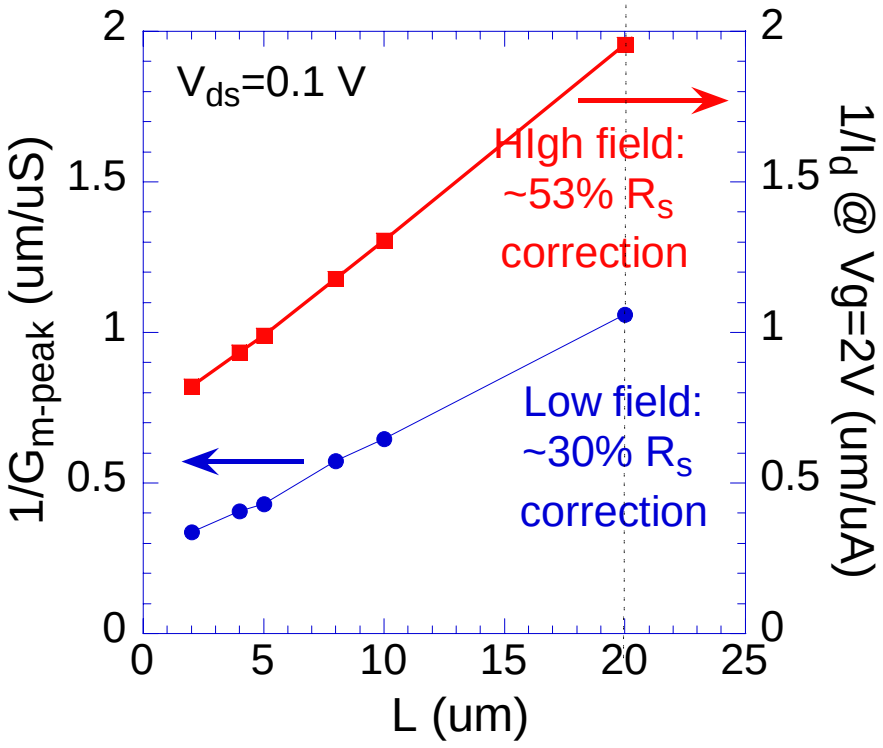



Fig. 5.3 Peak transconductance (left y-axis) and drive current at $V_g$ = 2 V (right y-axis) as a function of the channel length for Ge n-MOSFETs. The peak $G_m$ and $I_d$ data were extracted from the $I_d$-$V_g$ plots. Due to the degradation of drive current resulting from S/D series resistance, 30% correction at low field and 53% correction at high field were made in calculation of mobility by using the $I_d$-$V_g$ data of $L$ = 20 um devices

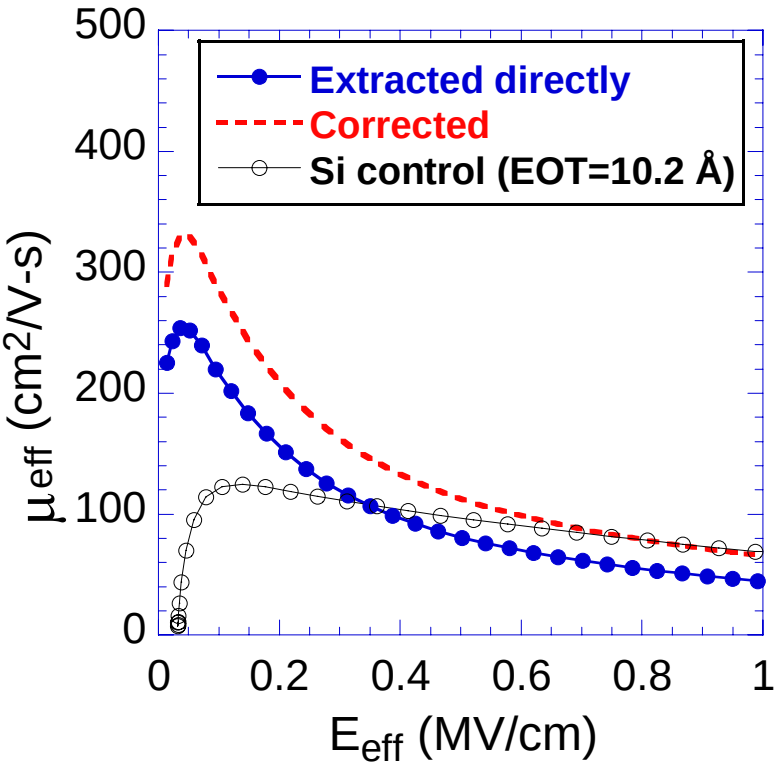



Fig. 5.4 Comparison of extracted electron mobilities for bulk Ge and Si control n-MOSFETs. The Ge devices show 2.5X enhancement in peak mobility compared to the silicon control.

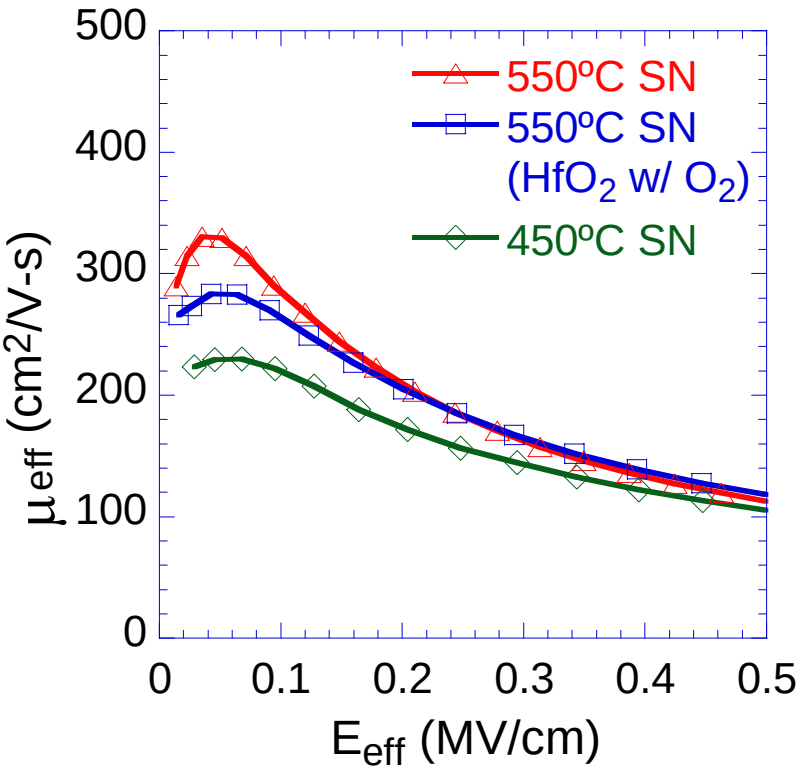



Fig. 5.5 Extracted electron mobilities as a function of effective electric field for bulk Ge n-MOSFETs with different SN treatment and CVD $HfO_2$ deposition: Δ 550°C SN + $HfO_2$ without $O_2$; □ 550°C SN + $HfO_2$ with $O_2$; and ◊ 450°C SN + $HfO_2$ without $O_2$

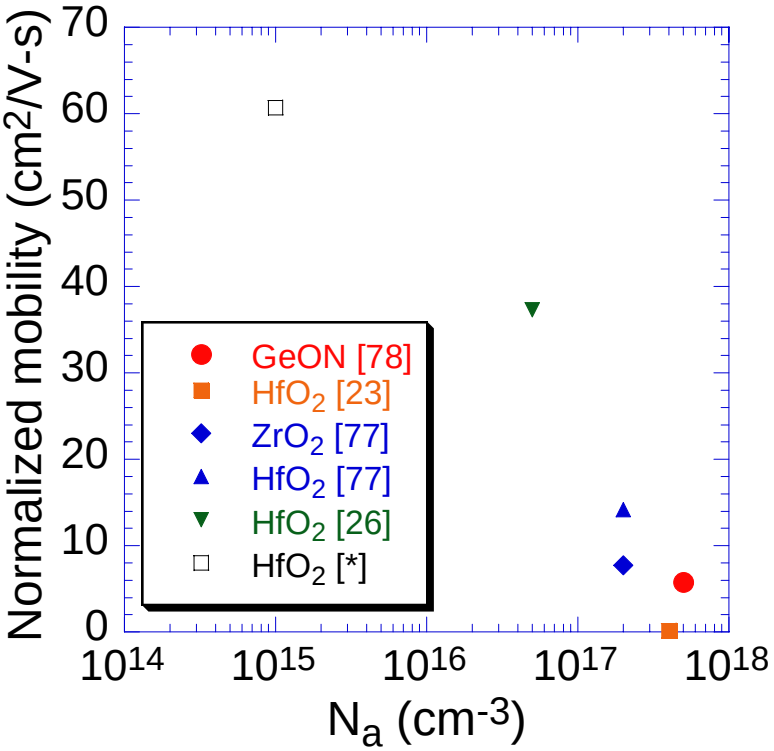



Fig. 5.6 Normalized mobilities v.s. substrate doping concentrations for bulk Ge n-MOSFETs with various dielectrics. Data come from Ref. [78][23][77][26] and this work [*], respectively. The normalized mobilities were extracted from $I_{dsat}$ at $V_g - V_t \sim 1$ V in $I_d$-$V_d$ curves with the equation of $I_{dsat} = 0.5\ (W / L)\ \mu_{eff}\ C_{ox}\ (V_g - V_t)^2$.

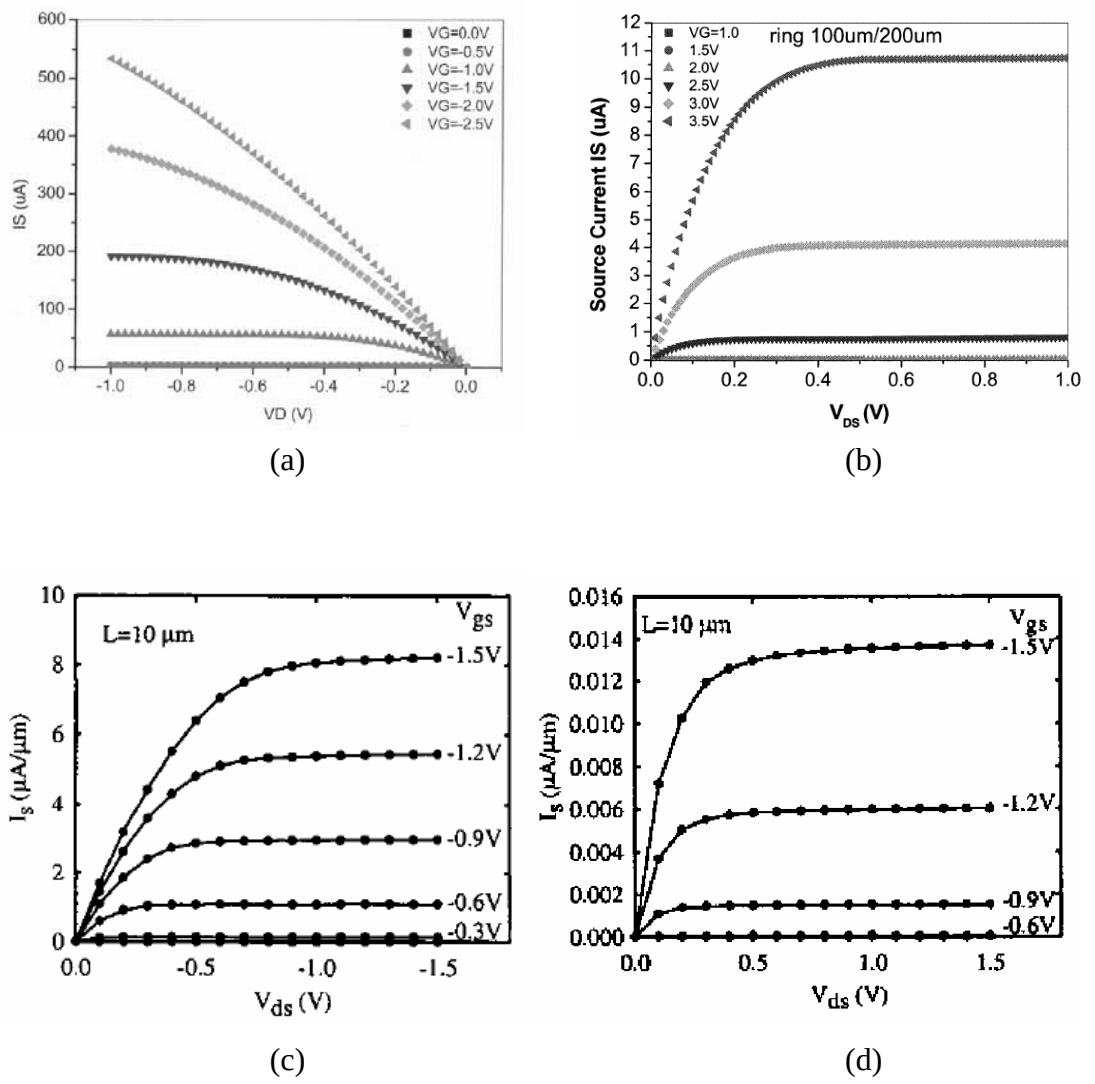



Fig. 5.7 Comparison of the $I_s$-$V_d$ characteristics for Ge p-MOSFETs and n-MOSFETs in literature: (a) $GeO_xN_y$ passivated p-MOSFET [49]; (b) $GeO_xN_y$ passivated n-MOSFET [78]; (c) CVD $HfO_2$ passivated p-MOSFET [23] and (d) n-MOSFET CVD $HfO_2$ passivated n-MOSFET [23]. The n-MOSFETs show much lower drive current compared to their p-type counterparts though the fabrication processes are almost identical for p- and n- type devices.

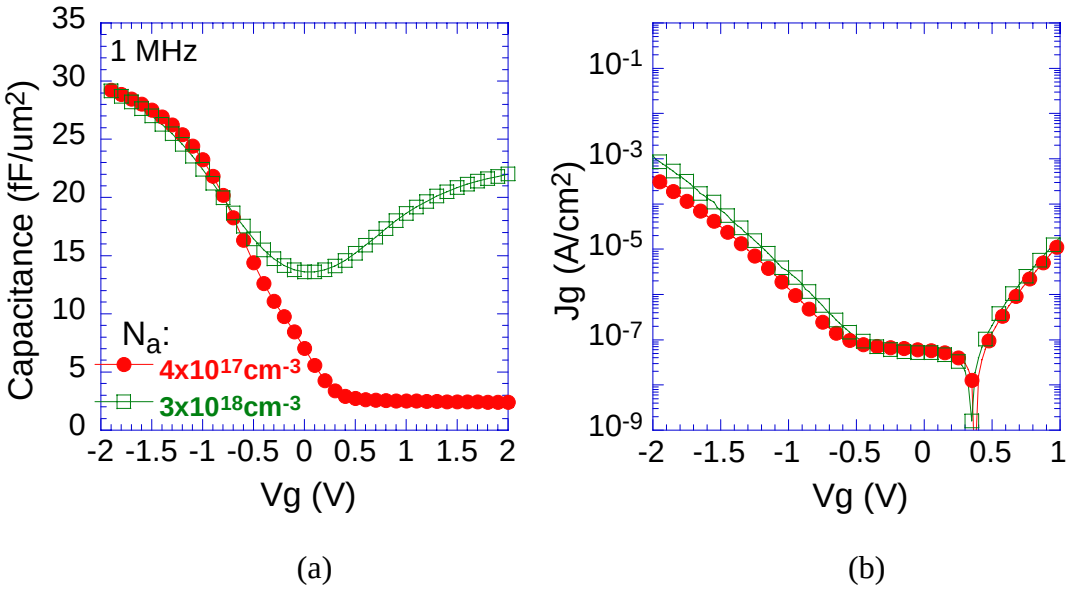



Fig. 5.8 (a) High frequency *C-V* and (b) *I-V* characteristics of Ge n-MOS capacitors fabricated on p-substrates with doping concentration of $4\times10^{17}$ $cm^{-3}$ and $3\times10^{18}$ $cm^{-3}$. 550°C SN surface treatment and $HfO_2$ deposition with $O_2$ were carried out for these devices.

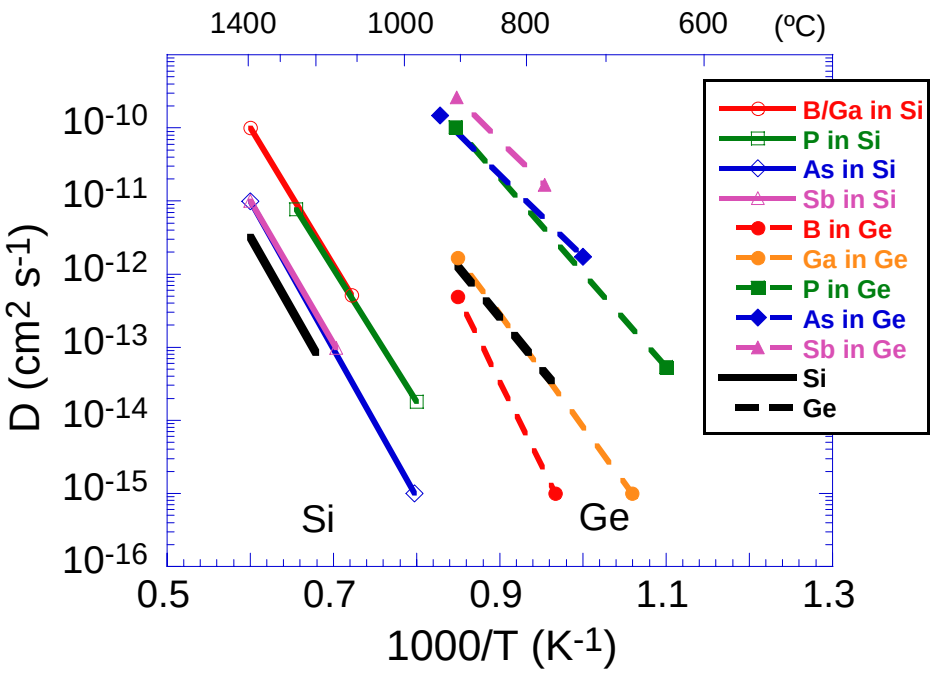



Fig. 5.9 Diffusion coefficients of B, Ga, P, As and Sb in Si and Ge and the self diffusion coefficients of Si and Ge as a function of the inverse of temperature [21]

# Chapter 6: Interfacial layer growth mechanism in Ge MOS devices and the substrate doping effect

## 6.1 INTRODUCTION

In Chapter 3 and 4, $NH_3$-based SN treatment, *in situ* cleaning by Ar anneal and SiIL passivation have been demonstrated to be effective passivation techniques to improve the electrical properties of Ge devices by forming a more stable interfacial layer and suppress the growth of $GeO_x$ as well as the interdiffusion across the interface. Some other surface pretreatment techniques like $SiH_4$ anneal [25][72], AlN passivation and $PH_3$ treatment [26] have also been reported improving the device performance. Surface pretreatments play a very crucial role in a successful Ge MOS device fabrication but the factors affecting the surface passivation and the kinetics of the interface growth and Ge updiffusion are still not very clear. Therefore, understanding the reactions and interdiffusion taking place at the interface is of great interests.

Another interesting phenomenon, as discussed in the previous chapter, is that the substrate doping condition plays a very important role on the device performance, especially for n-channel devices. In order to reveal the kinetics governing the interface growth and Ge diffusion and to investigate the role of the substrate doping in the interface reactions, the electrical properties of the MOS devices built on various substrates with various passivation conditions are compared in this chapter.

## 6.2 EXPERIMENT

In this experiment, both n- and p-type Ge wafers with (100) orientation were used for device fabrication. As listed in Table 6.1, the n-type substrates were doped with Sb at a concentration of $N_d = 5\times10^{16}$ cm$^{-3}$. The p-type substrates were Ga doped with $N_a = 1\times10^{15}$ cm$^{-3}$, $4\times10^{17}$ cm$^{-3}$ and $3\times10^{18}$ cm$^{-3}$, which are referred to "low", "high" and "higher", respectively. Both CVD and PVD techniques were used for $HfO_2$ deposition. In case of CVD, different process conditions, such as with or without SN pretreatment and with or without $O_2$ introduction during deposition, have been attempted. SN pretreatment was carried out by rapid thermal anneal (RTA) in $NH_3$ at 550°C for 2 min prior to $HfO_2$ deposition. ~ 5 nm $HfO_2$ film was *in situ* deposited at 400°C. For PVD $HfO_2$ deposition, a layer of Hf was sputtered on the precleaned substrates, followed by PDA in a $N_2$ furnace at 500°C°, 600°C or 650°C for 5 min or in a rapid thermal process (RTP) chamber at 600°C for 30 sec. The split conditions for dielectric layer deposition are listed in Table 6.2. After $HfO_2$ growth, 1500Å TaN was reactively sputtered on the top of the dielectric layers as the gate electrodes. Si control samples were also prepared with identical $HfO_2$ and TaN deposition processes. SN pretreatment for Si control samples in CVD process was performed at 700°C for 10 sec in $NH_3$. PMA in $N_2$ or forming gas was performed for thermal stability investigation.

In this Chapter, CET values extracted directly from accumulation *C-V*, instead of EOT values, are used in device properties' comparison to avoid the inaccuracy and difficulty in EOT extraction by *C-V* simulation.

## 6.3 DEPENDENCE OF $HfO_2$ AND INTERFACIAL LAYER GROWTH ON SUBSTRATE AND PROCESS CONDITIONS

### 6.3.1 CVD $HfO_2$ on SN-treated Ge substrates

Fig. 6.1 shows the typical high frequency (1 MHz) *C-V* and *I-V* characteristics for the MOS devices built on different types of substrates. Those samples received SN treatment prior to $HfO_2$ deposition and 400°C 30 min forming gas anneal. Note from the *C-V*s that their CET values are not identical. The devices on the highly doped p-type substrates exhibit a thinner CET of 10.5 Å and those on the n-type substrates and low doped p-type substrates have a thicker CET of 11.6 Å. Assuming a 40 Å $HfO_2$ layer (the thickness reduction from the target thickness 5 nm is mainly due to the consumption caused by the plasma sputtering process for gate electrode deposition) and a 3~4 Å $GeO_xN_y$ interfacial layer, taking the dielectric constant of $SiO_2$, $HfO_2$ and $GeO_xN_y$ layer as 3.9, 25 and 4.7 [14][49] respectively, and considering a 2 Å quantum mechanical correction (which is estimated from the previous simulation results, readers may refer to Section 3.3 and 4.3), the CET value is estimated to be $40\cdot(3.9/25) + (3\sim4)\cdot(3.9/4.7) + 2 = 10.7 \sim 11.6$ Å, consistent with the measured results. As displayed in Fig. 6.1(b), all the n-MOS devices display almost identical superior $J_g$, which are around $2\times10^{-6}$ A/cm$^2$ at $V_g = -1$ V. The observed slightly higher $J_g$ of the p-MOS devices, which is $4\times10^{-5}$ A/cm$^2$ at $V_g = 1$ V, can be attributed to the lower barrier height of the substrate injection than that of the gate injection for electrons since the TaN gate electrode has a mid-gap work function. The observed identical $J_g$ characteristics in the n-MOS devices imply that the sight CET variation possibly comes from the difference in the interfacial layer rather than the high-κ dielectric layer. The abnormal *C-V* of the devices on the higher doped p-

substrates could be caused by the impurity diffusion related structural defects near the germanium surface.

Fig. 6.2(a) compares the *C-V* hysteresis ($\Delta V_{fb}$) characteristics. Smaller $\Delta V_{fb}$ is observed in the devices on the highly doped p-substrates, suggesting lower slow trap density ($D_{st}$). The dynamic *I-V* technique [66] was also employed to compare the slow trap density and its distribution in the depletion region. As shown in Fig. 6.2(b), the devices on the highly doped p-substrates exhibit lower slow trap density and larger trap response time constant ($t_0$). The lower $D_{st}$ is consistent with the *C-V* hysteresis result. The larger $t_0$ indicates longer mean trapping/detrapping path from the substrate to the trap centers, implying that the reduced traps are mainly distributed near the substrate. Since most of the traps in Ge devices are near or in the interfacial layer [113], the shrink of the interfacial layer may result in lower $D_{st}$ near the surface.

Fig. 6.3 shows the time-zero dielectric breakdown (TZBD) voltages ($V_{bd}$) of these devices and the dependence on the substrate doping is observed. The significant lower $V_{bd}$ in the n-MOS devices is believed resulting from the asymmetrical band structure of the MOS stack and the significant difference of the electric field across the gate dielectric between positive bias in Ge p-MOS stack and negative bias in Ge n-MOS stack. Detailed study is presented in Chapter 8. The n-MOS on the highly doped substrates exhibit even lower $V_{bd}$ than that on the low-doped as shown in Fig. 6.3, which can be anticipated since it is consistent with the conclusion obtained from the CET and $D_{st}$ results that thinner interfacial layers are

formed on the highly doped substrates so the electrical filed across both the interfacial layer and the high-κ layer increases accordingly.

### 6.3.2 CVD $HfO_2$ directly on Ge substrates (non-SN treatment case)

The devices without SN surface treatment prior to CVD $HfO_2$ deposition were also prepared on various substrates. $J_g$ at $|V_g|$ = 1 V as a function of the CET value, for both the non-SN- and SN- treated devices, are shown in Fig. 6.4. Benefiting from the formation of a nitrided interfacial layer, SN treatment sufficiently reduces CET and $J_g$ for both Ge and Si control devices. It is also noted that the n-type SN-treated, p-type SN-treated, and n-type non-SN-treated Ge MOS devices exhibit lower leakage currents than their Si counterparts at the same CETs, suggesting thinner interfacial layers in those Ge devices compared to the Si control devices.

The CET variations on the different types of substrates for both the SN and non-SN treatment cases are compared in Fig. 6.5. Without a nitrided interfacial layer, CET increase is speculated to be due to the growth of native oxide interfacial layer as well as Ge updiffusion into the dielectric [52][62]. Surprisingly, 6 Å EOT increase is found for the non-SN-treated p-MOS Ge devices compared to their n-type counterparts, indicating that the substrate doping resulted variations in the formation of the interfacial layers are significantly enlarged in the non-SN treatment case.

The hysteresis characteristics and breakdown voltages as a function of the substrate are shown in Fig. 6.6. The larger hysteresis and lower breakdown voltages in those non-SN-treated devices than in the SN-treated devices (Fig. 6.2 and 6.3) clearly illustrate the advantage of SN passivation by forming a $GeO_xN_y$ interfacial

layer, which effectively blocks the inter-diffusion and has a lower trap density and better quality than the native oxide layer. The much thicker $GeO_x$ interfacial layers in the non-SN-treated p-MOS devices, as found from the CET variations in Fig. 6.6, give rise to the much larger hysteresis correspondingly. The significant decrease of the breakdown voltages in the non-SN-treated devices should be caused by the higher gate leakage current as well as the dramatically increased traps in the dielectric introduced by Ge updiffusion.

### 6.3.3 The impact of $O_2$ introduction in CVD $HfO_2$ deposition

Because the hafnium-t-butoxide precursor can release oxygen when dissolving at high temperature, the introduction of $O_2$ is not a requirement for the CVD $HfO_2$ deposition. The experiments based on Si showed similar dielectric quality for the cases with and without the introduction of $O_2$ during deposition. The only difference is that the non-$O_2$ deposition causes thinner interfacial layer growth and thus slightly reduced CET for the non-SN treatment case. However, whether introducing $O_2$ or not shows dramatic impact for the case that $HfO_2$ is directly deposited on Ge substrates. Table 6.3 shows the physical thicknesses of the dielectric films measured by ellipsometry for those different deposition conditions on both Ge and Si substrates. When there is no $O_2$ introduction and no SN treatment, the dielectric thickness is reduced significantly (~ 15 Å) for any type of Ge substrate. The very high $J_g$, which is above 1 A/cm$^2$ at ±1 V as shown in Fig. 6.7(a), confirms the shrink of the dielectric layer. Kita et al. [54] has reported that both interfacial layer and $HfO_2$ formed on Ge are thinner than on Si in PVD $HfO_2$ process. They suggested that

the generation of a volatile reactive product Hf-Ge-O at the interface could be the reason. The shrink of the $HfO_2$ layer in this CVD process is possibly caused by a similar mechanism. The dissolved precursor and Ge react on Ge surface: Hf + O + Ge $\rightarrow$ Hf-Ge-O or Hf + GeO. When there is no sufficient oxygen supply, volatile products like Hf-Ge-O and GeO rather than $HfO_2$ or $GeO_2$ will be more easily generated. Thermal desorption of those volatile reactive products consumes the precursor and retards the formation of the high-κ layer. *C-V* curves (Fig. 6.7(b)) also display the severely degraded interface quality.

### 6.3.4 PVD $HfO_2$ on Ge substrates

In order to further investigate the kinetics at the interface and the impact of the substrate doping, PVD $HfO_2$ passivated devices were fabricated with various PDA conditions. Fig. 6.8(a) shows the typical *C-V*s for the devices with 600°C PDA in furnace. CET variations with the substrate are observed. Fig. 6.8(b) shows the CET values as a function of the substrate under different PDA conditions. It is noted that the CET variation with the substrate is a function of the PDA temperature. At 500°C, the variations in CET are very small. Only the devices on the highly doped p-substrates show slightly lower value. With temperature increasing, both the CETs and the CET variations with different types of substrates increase. It is interesting to notice that at lower temperature, only the highly doped p-substrate devices show lower CETs, which is similar to the SN treatment case in the CVD process. Another noticeable result is that both p-MOS and n-MOS Ge devices exhibit lower CETs compared to Si control devices when the PDA temperature is above 500°C, which is

consistent with the result reported by Kita et al [54]. The leakage currents of the PVD devices are on the same level as the non-SN-treated CVD devices. Also note that PDA in an RTP chamber at 600°C results in the largest CET decrease for the Ge devices as compared to the Si control.

### 6.4 POSSIBLE INTERFACE GROWTH KINETICS

To explain the above results from both the CVD and PVD $HfO_2$ depositions on Ge substrates, a possible mechanism is suggested that two competing processes taking place on the Ge surface determine the interface layer formation and also affect Ge updiffusion. One process is called "oxide growth" process, which leads to the growth of $GeO_x$ layer by reactions of $Ge + O \rightarrow GeO$, $GeO + O \rightarrow GeO_2$. This process increases CET by forming $GeO_x$ interfacial layer. The other process is called "oxide desorption" process, which may include reactions like $Ge + O \rightarrow GeO$, $Ge + GeO_2 \rightarrow GeO$ and $Hf + O + Ge \rightarrow$ Hf-Ge-O. The desorption of those volatile products like GeO and Hf-Ge-O, which can occur at a temperature as low as 390°C [59], tends to impede the interfacial layer growth and even eliminate the interfacial layer. The presence of the second process explains the phenomena observed in many cases that the Ge devices exhibit a thinner interfacial layer than the Si devices. The oxide desorption process may also enhance the updiffusion of Ge atoms into the $HfO_2$ dielectric.

Several factors — temperature, oxygen supply amount, and the substrate doping condition, exhibit the influences on the interface reactions and those two processes, which result in the variations with different process conditions and

different types of substrates. As listed in Table 6.4, increasing temperature and sufficient oxygen supply is believed to enhance both the oxide growth and desorption processes. However, for very limited oxygen supply, the desorption process will dominate over the growth process since the growth process need more complete oxidation.

In case of CVD $HfO_2$ deposition directly on Ge, oxygen supply exhibits its critical role as shown in Section 6.3.3. Without $O_2$ introduction, oxygen is mainly provided by the decomposition of the precursor. Due to the limited oxygen supply, the oxide desorption process dominates. Large amount of volatile products are generated which hampers the formation of interfacial layer and even retard the formation of $HfO_2$ film. With oxygen introduction, we have same $HfO_2$ depositions on Ge as on Si since the oxide growth process is much enhanced. However, due to the impurities' impact, i.e., Ga impurity may tend to help the oxide desorption process while Sb may enhance the oxide growth process, it also leads to large CET variations with the substrate.

For the SN treatment case in the CVD process, SN treatment immunizes the reactions on Ge surface during $HfO_2$ deposition. But the surface treatment process itself is still affected by those two processes so the formed $GeO_xN_y$ interfacial layer also shows slight dependence on the substrate. The high concentration of Ga impurities exhibit more aggressive enhancement effect on the oxide desorption process especially in a limited oxygen ambient and lead to a slightly thinner interfacial layer on the highly doped p-type substrates.

The PVD process has shown us a more subtle picture. The PDA process in PVD $HfO_2$ deposition is generally oxygen-limited since the oxygen for interface reactions has to diffuse through the top Hf layer from the ambient. When the PDA temperature increases, the interface reactions' rates increase and the oxygen amount for interface reactions also increases due to the faster oxygen diffusion rate, which enhances both the oxide growth and desorption processes. Therefore, with increased PDA temperature, the CET increases and the CET variation with the substrates also increases simultaneously. Performing PDA in a RTP chamber at 600°C further enhances the oxide desorption process and causes larger CET reduction for the Ge devices since the amount of $O_2$ in a RTP chamber is much less than that in a $N_2$ furnace.

The mechanism of the doping effect in those two processes needs more investigation. Notice that the much higher diffusivities of the impurity atoms and Ge itself in Ge as compared to those in Si (Fig. 5.9) [21][85], it is believed that the existence of the oxide desorption process and the high diffusivities of Ge and impurity atoms in Ge lead to the substrate doping effect. The structural defects formed near the substrate surface due to the impurity diffusion may play a role, especially when the impurity concentration is high. More defects may provide more broken bonds and then more free Ge atoms available for interface reactions, especially for the oxide desorption process. Fig. 6.9 shows the cross-sectional transmission electron microscopy (XTEM) images of the as-deposited MOS stacks on the n-substrate and on the highly doped p-substrate. Rougher surface is observed

on the highly doped p-substrate, which is possibly caused by the structural defects near surface and/or the desorption process.

## 6.5 *C-V* FREQUENCY DISPERSION

The *C-V* frequency dependence at a range from 10 KHz to 1 MHz is displayed in Fig. 6.10(a)-(d) for the SN-treated CVD $HfO_2$ MOS devices based on the n-type, low doped p-type, highly doped p-type and higher doped p-type substrates, respectively. No much frequency dispersion is observed in the accumulation region for both the n-type and p-type devices, suggesting the similar quality of the $HfO_2$ layers. However, the *C-V*s behave quite differently in the inversion region. The humps in (a) and (c) may be originated from the "slow" traps near the interface [22]. The low-frequency *C-V* shapes in (b) and (d) for the low doped and higher doped p-substrate cases imply the reduced minority carrier response time ($\tau_R$), but the mechanism shortening $\tau_R$ should be different. In case (b), considering the low-doped substrate and the narrow bandgap of Ge, the diffusion-controlled response is dominant since the substrate is able to provide large amount of minority carriers ($\tau_R \propto \frac{N_a^{3/2}}{n_i^2}$) [83], which can follow the high frequency small signals at room temperature. In case (d), the generation-recombination controlled response is dominant due to the high substrate doping ($\tau_R \propto \frac{N_a}{n_i}\tau_T$, where $\tau_T$ is the minority carrier lifetime) [83]. Since normally the minority carrier generation/recombination rate ($R = \frac{1}{\tau_T}$) is proportional to the doping concentration [82], *C-V* should not

depend on the substrate doping, i.e., the *C-V*s in (d) should have a normal high-frequency shape as in (c). Therefore, there must be some other generation/recombination process, which decreases the minority carrier lifetime and the response time as well. It is possible that the structural defects or dislocations near/below the surface induced by the diffusion of the highly doped impurities provide the large amount of traps for minority carrier generation which sufficiently reduce $\tau_T$.

### 6.6 SUMMARY

In this chapter, we have compared the electrical properties of TaN/$HfO_2$/Ge MOS devices built on different types of substrates, including the CET, gate leakage current, hysteresis, slow trap density, *C-V* frequency dispersion and breakdown voltage. The dependence of the device performance on the substrate indicates the crucial role of substrate doping in the reactions at the interface. Two competing processes (oxide growth and oxide desorption) are suggested to determine the formation of interfacial layer and affect Ge updiffusion. The oxide growth process leads to the growth of interfacial layer and the oxide desorption process impedes the growth by generation and desorption of volatile products like GeO or Hf-Ge-O. The oxide growth process is enhanced on the n-substrate and the oxide desorption process is enhanced on the p-substrate, especially when the substrate doping is high. This substrate doping effect may arise from the high diffusivities of atoms in Ge and the induced structural defects near the surface. The abnormal frequency dispersion characteristics and the rough interface of the gate stacks on the high doped Ge p-

substrates are possible caused by this effect. SN treatment, $O_2$ introduction in CVD and PDA temperature in PVD affect those two competing processes occurring at the interface and show significant impact on the electrical properties of the devices as well as the dependence on the substrate doping.

The device properties after PMA treatment also exhibit substrate doping dependence. The details are discussed in the next chapter.

| Ref # | Dopant | Concentration ($cm^{-3}$) |
|---|---|---|
| n | Sb | $5\times10^{16}$ |
| p-low | Ga | $\leq1\times10^{15}$ |
| p-high | Ga | $4\times10^{17}$ |
| p-higher | Ga | $3\times10^{18}$ |

Table 6.1 Doping impurities and doping concentrations in the Ge substrates used in this experiment

| | $NH_3$-based SN treatment (550°C 2min) | $O_2$ introduction in $HfO_2$ deposition (400°C) |
|---|---|---|
| CVD | with / without | with / without |
| | | |
| | Hf layer sputtering | PDA in $N_2$ ambient |
| PVD | ~ 5 nm | 500°C 5 min in furnace |
| | | 600°C 5 min in furnace |
| | | 650°C 5 min in furnace |
| | | 600°C 30 sec in RTP chamber |

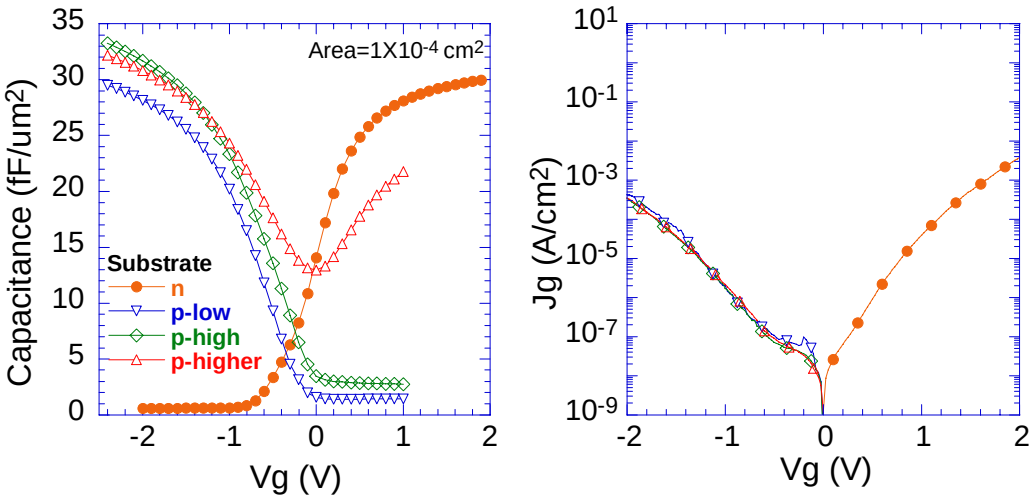
Table 6.2 Split conditions for dielectric deposition in this experiment

| Physical thickness (Å) | w/o SN | w/ SN |
|---|---|---|
| Ge (w/o $O_2$) | 38 | 54 |
| Ge (w/ $O_2$) | 54 | 53 |
| Si (w/o $O_2$) | 48 | 48 |

Table 6.3 Physical thicknesses of the dielectric films deposited on Ge and Si substrates by CVD with different conditions: with or without $O_2$ introduction during CVD processes; with or without SN pretreatment prior to $HfO_2$ deposition. The physical thicknesses were measured by ellipsometry.

| | Oxide growth | Oxide desorption |
|---|---|---|
| Temperature | + | + |
| Oxygen supply | + + | + |
| p-type dopant (Ga) | | + |
| n-type dopant (Sb) | + | |

Table 6.4 Impacts of temperature, oxygen supply amount, and the substrate doping condition on the two processes taking place on Ge surface. "+" indicates the enhancement effect. The oxide growth process needs more oxide supply and for very limited oxygen supply, the oxide desorption process will dominate over the oxide growth process.




(a) (b)

Fig. 6.1 (a) High frequency *C-V* and (b) *I-V* characteristics of CVD $HfO_2$ Ge devices with SN treatment on different types of substrates: n: n-substrate; p-low: low doped p-substrate; p-high: high doped p-substrate; and p-higher: higher doped p-substrate

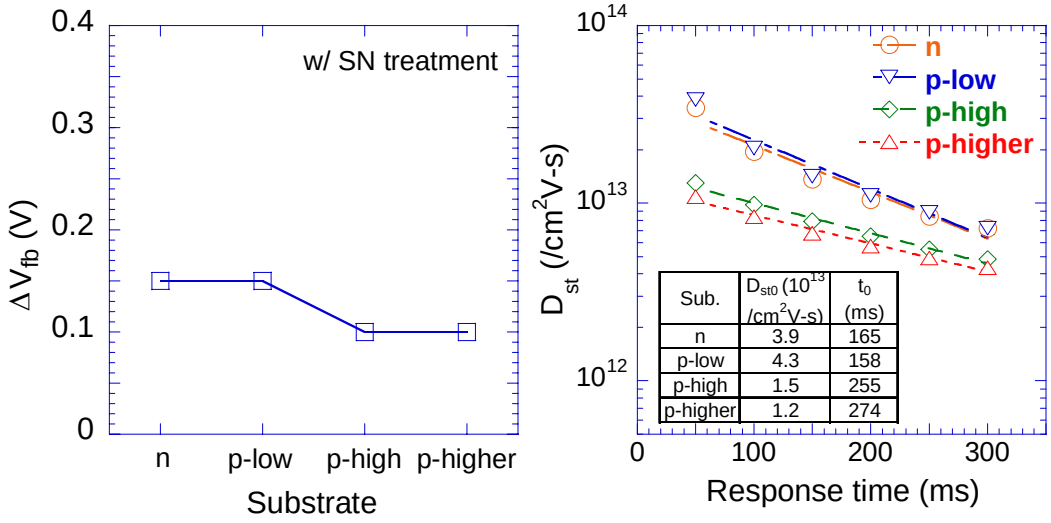



Fig. 6.2 (a) Hysteresis characteristics of CVD $HfO_2$ Ge devices with SN treatment as a function of the Ge substrate. (b) Slow trap densities extracted by dynamic *I-V* technique as a function of the trap response time for the CVD $HfO_2$ Ge devices with SN treatment. $D_{st0}$ and $t_0$ listed in the inset table are the fitting parameters of the curves according to $D_{st} = D_{st0}\, e^{-t/t_0}$.

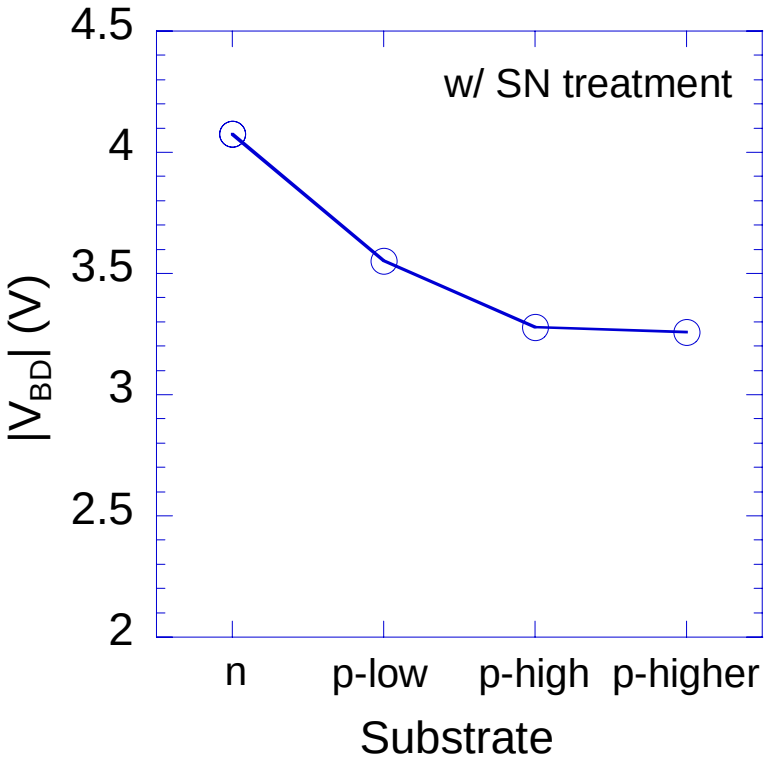



Fig. 6.3 Breakdown voltages as a function of the substrate for the CVD $HfO_2$ Ge devices with SN treatment

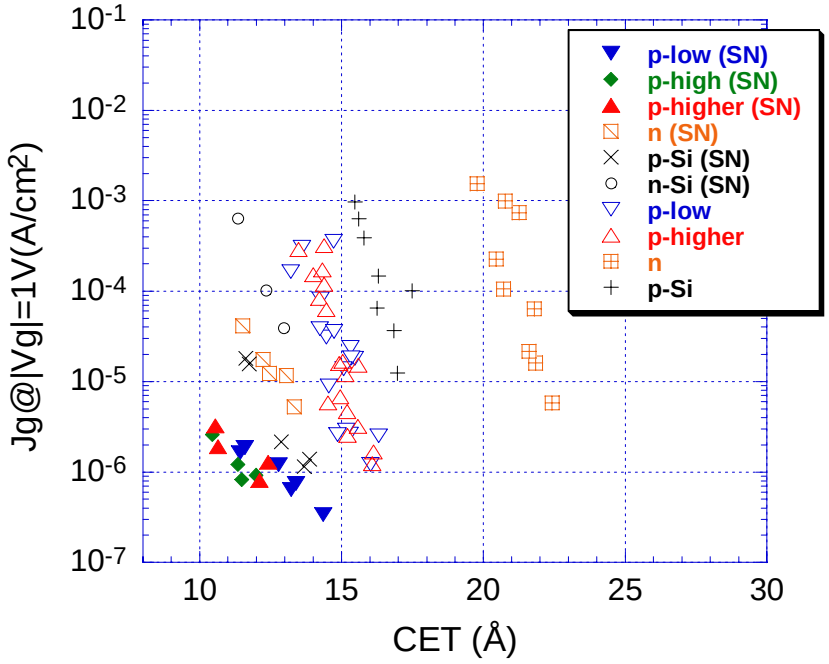



Fig. 6.4 $J_g$ as a function of CET for CVD $HfO_2$ devices on various substrates with or without SN treatment. $J_g$ were taken at $V_g = -1$ V for the n-MOS and $V_g = 1$ V for the p-MOS devices.

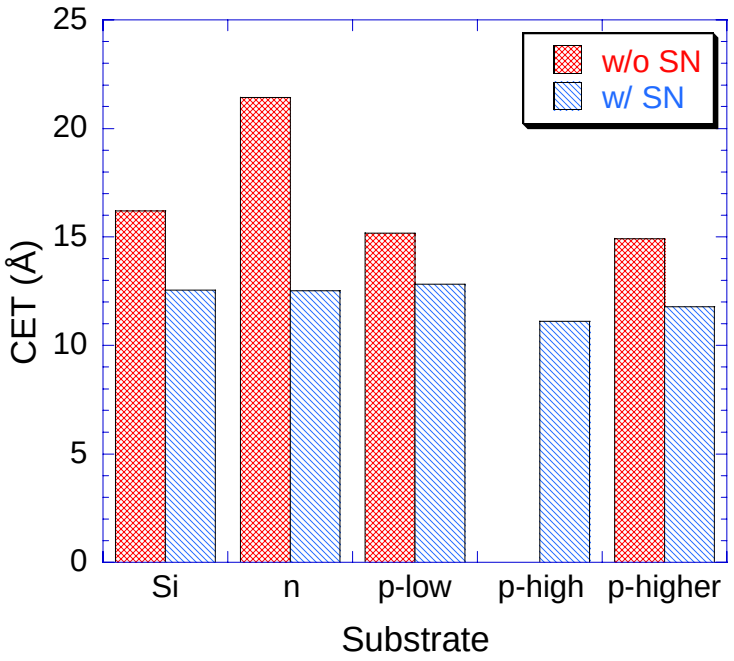



Fig. 6.5 CET variations with the substrate for the CVD $HfO_2$ devices with or without SN treatment

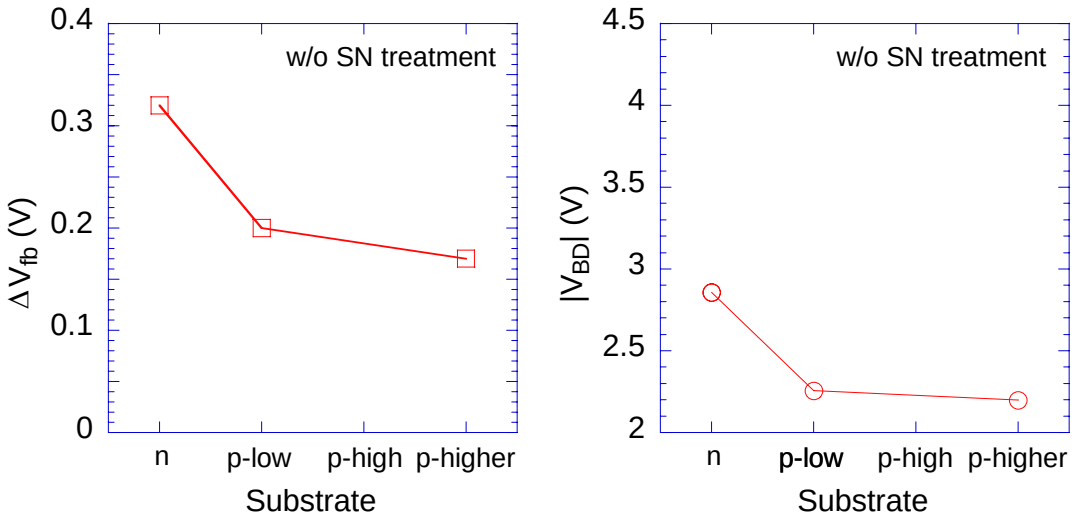
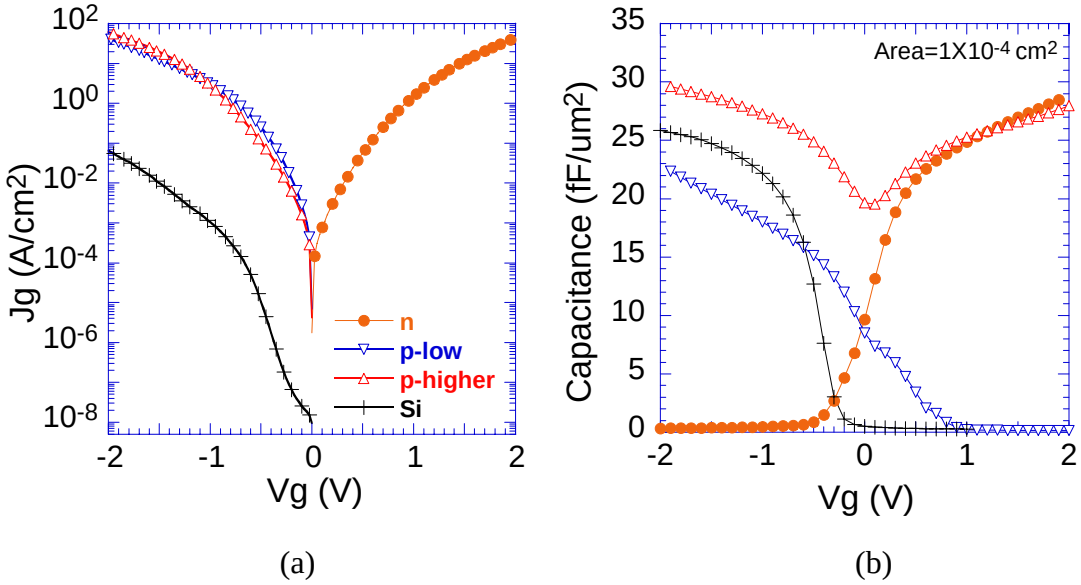
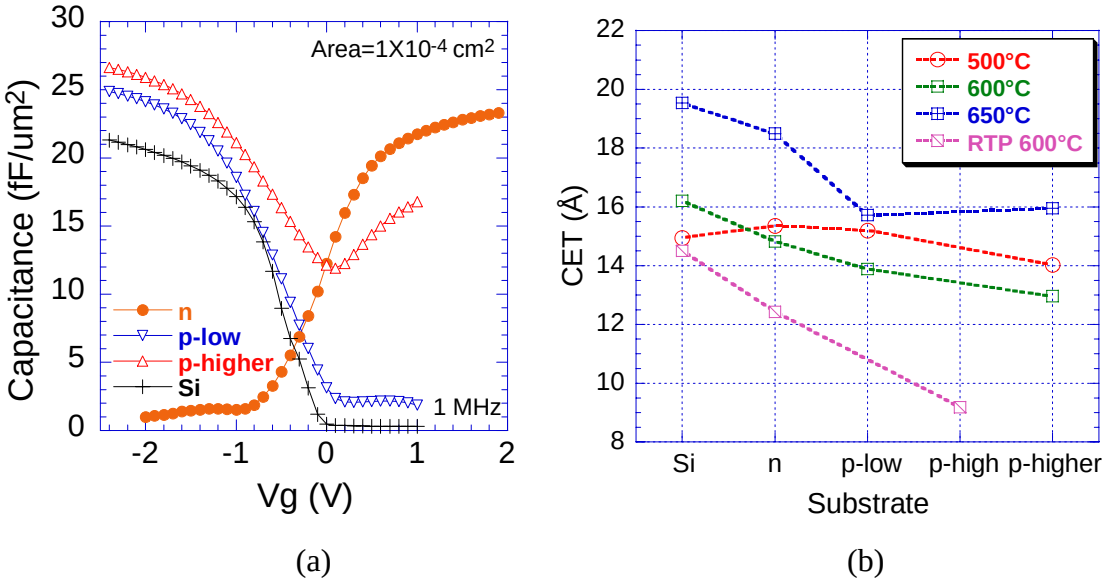



Fig. 6.6 (a) Hysteresis characteristics and (b) breakdown voltages of the CVD $HfO_2$ Ge devices without SN treatment as a function of the Ge substrate



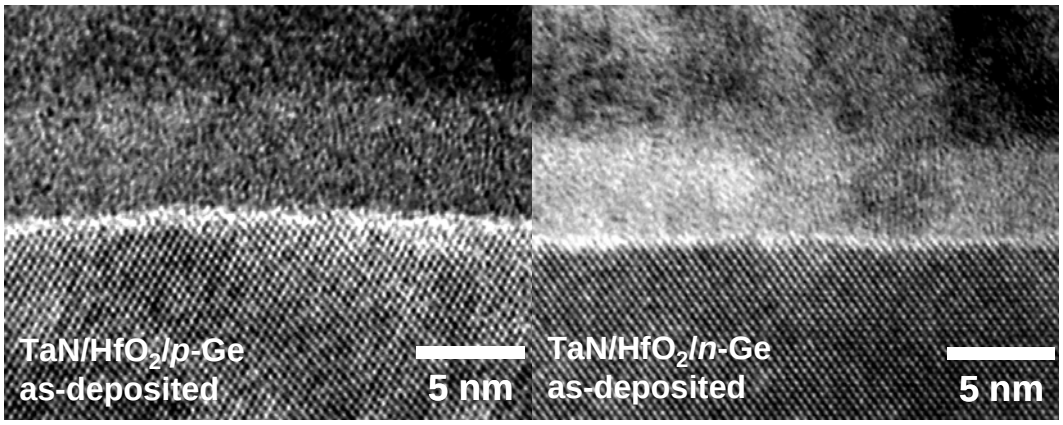

(a) (b)

Fig. 6.7 (a) *I-V* and (b) high frequency *C-V* characteristics for the devices with CVD $HfO_2$ deposited directly on Ge substrates without the introduction of $O_2$ during CVD process




(a) (b)

Fig. 6.8 (a) High frequency *C-V* characteristics for the devices using PVD $HfO_2$ dielectric with 600°C PDA treatment. (b) CET variations with the substrate for the devices with PVD $HfO_2$ as the dielectric. The PDA treatment was performed at 500, 600, or 650°C for 5 min in a $N_2$ furnace or 600°C for 30 sec in a RTP chamber, respectively.




(a) (b)

Fig. 6.9 XTEM images of the as-deposited TaN/CVD $HfO_2$ stacks on SN-treated (a) highly doped p-substrate and (b) n-substrate

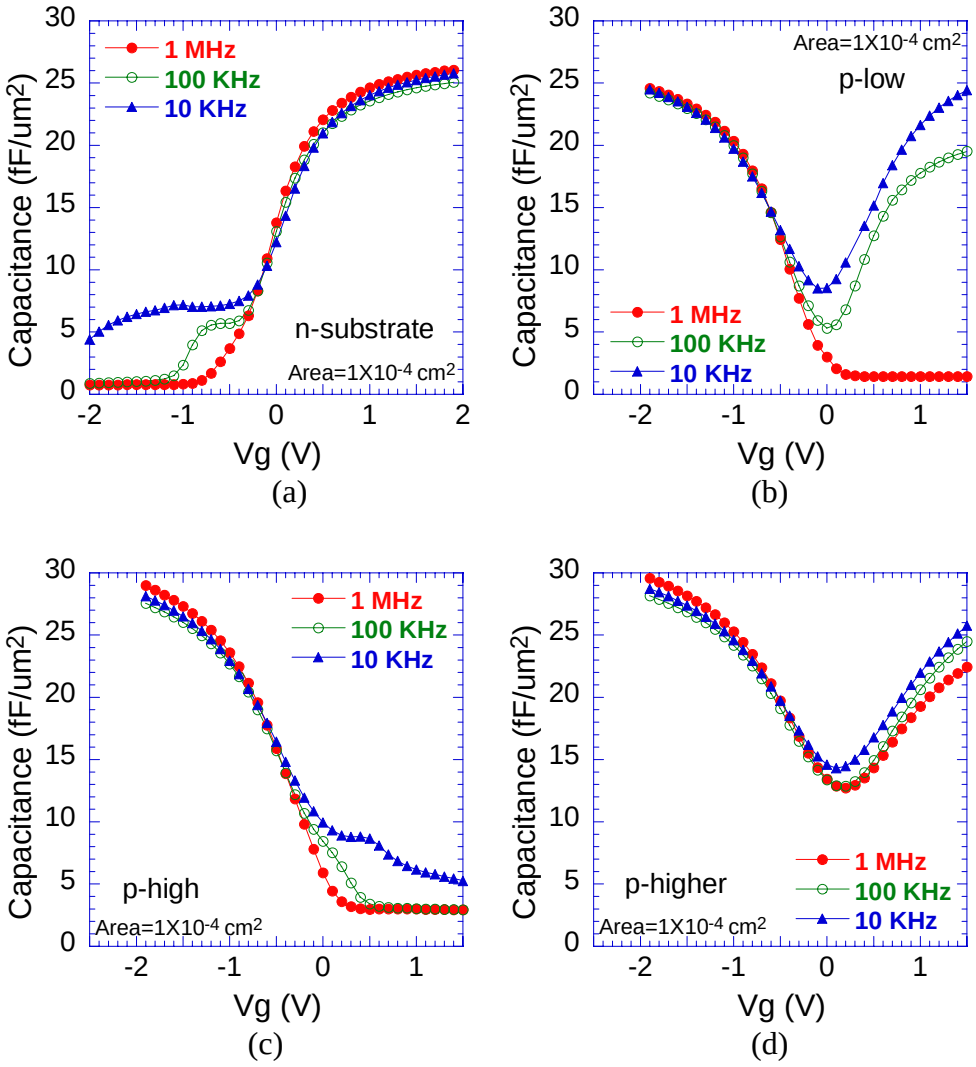



Fig. 6.10 *C-V* characteristics at 10 KHz, 100 KHz and 1 MHz measurement frequencies for the devices on different types of substrates: (a) n-type; (b) low doped p-type; (c) high doped p-type; and (d) higher doped p-type. $HfO_2$ was deposited by CVD with SN pretreatment.

# Chapter 7: Thermal stability (PMA effect)

## 7.1 INTRODUCTION

In semiconductor device fabrication, various thermal processes are needed for various purposes. Thermal budget is always an important issue for a successful fabrication since the diffusion taking place may cause significant influence in electrical properties and performance of a device. For Si-based CMOS devices, high temperature thermal anneal at 900-1000°C is always performed to activate implanted dopants. Thermal anneal is also effective to reduce dielectric defects, trapped charges and interface states, especially for high-κ dielectrics [73][86]. In fact thermal stability is one of the challenging issues for the application of some high-κ materials such as $ZrO_2$ and $Ta_2O_5$ in traditional Si processes [47][87][88][89] due to the relatively poor thermal stability caused by the interdiffusion and the reactions with Si.

The use of metal gate and germanium substrate eliminates the need of very high temperature activation processes. The experiments on ion implantation and activation in germanium by several groups show that 400-700°C process can successfully activate the dopants and achieve low resistivity, especially for p-type devices — it was reported that the as-implanted boron dopants have already been activated even without further thermal anneal [90][91]. Elimination of high temperature process is not only an advantage but also a challenge since relatively low temperature processes are required to realize high quality devices, especially with high-κ materials as the gate dielectric. Considering the high diffusivity in Ge

than in Si and the volatility property of GeO and Hf-Ge-O, the thermal stability of germanium devices at the range of 400-700°C is still a concern.

In this chapter, the thermal stability of germanium based MOS devices is studied. 400-700°C PMA in nitrogen or forming gas were carried out on selected samples for investigation. Considering the dependence on the substrate doping, the PMA effect on p- and n-type devices are introduced separately.

### 7.2 PMA EFFECT ON GERMANIUM P-MOS

Fig. 7.1 shows the high frequency (1 MHz) *C*-*V* and *I*-*V* characteristics for the SN treated TaN/$HfO_2$/n-Ge MOS stacks after 450-700°C PMA treatments. With the increased anneal temperature, two distinguish trends are observed: flat band voltage positive shift and gate leakage current increase. The lower frequency (100 KHz and 10 KHz) *C*-*V* characteristics, as shown in Fig. 7.2, indicate that the trap density also increases significantly after anneal. Fig. 7.3 shows the high frequency *C*-*V* characteristics for the SiIL/SN-treated TaN/$HfO_2$/n-Ge MOS stacks. Same trends are observed as those stacks without SiIL passivation.

400°C anneals have been carried out following a 450°C anneal. Slight $V_{fb}$ shift and *C*-*V* frequency-dispersion degradation are observed (Fig. 7.4), indicating that the degradation after PMA not only depends on the anneal temperature, but also the thermal budget — which implies that the degradation is a diffusion related process. In Fig. 7.5 the $V_{fb}$ shift and $J_g$ increase in Ge p-MOS devices with increased anneal temperatures are summarized.

### 7.3 PMA EFFECT ON GERMANIUM N-MOS

The PMA effect on SN-treated Ge n-MOS devices with different substrate doping concentrations has been investigated. The flatband voltages and the gate leakage currents as a function of the anneal temperature are shown in Fig. 7.6. Same trend of positive $V_{fb}$ shift and $J_g$ increase after PMA is observed in all the devices built on various substrates.

Fig. 7.7 displays the *C-V* characteristics after 600°C PMA treatment. Different from the p-MOS case, the *C-V* curves tend to become flat, indicating the presence of large amount of interface states which cause the Fermi-level pinning effect. The degradation of the *C-V* characteristics depends on the substrate doping concentration and those on the highest doped substrates exhibit the most degraded *C-V*s after PMA.

Fig 7.8 displays the distribution of TZBD voltages, the CET and leakage current after 400-600°C PMA for the Ge n-MOS devices on low doped substrates. In addition to degraded gate leakage and dielectric breakdown strength, n-MOS devices exhibit CET decrease, which is quite different from those p-MOS devices. More decrease of CET is observed in the n-MOS devices on highly doped substrates, as shown in Fig. 7.7.

Another phenomenon needed to note is that the n-MOS devices built on highly doped substrates show a normal high frequency *C-V* in the inversion region when receiving an *in situ* cleaning by Ar anneal. But even after 400°C PMA, those 1 MHz *C-V*s restore to the low-frequency *C-V* shape like that shown in Fig. 5.8(a). This further confirms that those defects causing the abnormal behaviors of highly

doped n-type devices distribute near the Ge surface since they are so sensitive to the surface and thermal treatment.

### 7.4 DISCUSSION

For all the SN-treated devices on various substrates, the same trend with increased anneal temperature, in terms of $V_{fb}$ positive shift and $J_g$ increase, is believed to be caused by the interdiffusion at the interface and Ge updiffusion into the dielectric. However, the p- and n-type devices exhibit quite different *C-V* characteristics after high temperature PMA. The abnormal *C-V* behaviors of n-MOS devices suggest severe degradation near the interface and the increases of the accumulation capacitances indicate the reduction of EOT. These phenomena are able to be understood considering the two competing processes taking placing at the interface. During a high temperature anneal, interdiffusion of Hf and Ge atoms and the desorption of volatile species degrade and shrink the $GeO_xN_y$ interfacial layer. Fig. 7.9 displays the XTEM images for the $Ar/NH_3$ treated $TaN/HfO_2/Ge$ stacks before and after 600°C PMA. The thermal annealing substantially eliminates the $GeO_xN_y$ interfacial layer. The decomposition of the $GeO_xN_y$ interfacial layer partially explains the positive shift of $V_{fb}$ since less N is present at the interface. The reduction of interfacial layer reduces the EOT but the diffusion of Ge into $HfO_2$ may increase the EOT by degrading the dielectric constant. Therefore p-MOS devices exhibit even slightly higher EOT after 600°C PMA. The enhanced oxide growth process may also compensate the EOT loss. But for n-MOS devices, $HfO_2$ may react with Ge and generate large amount of volatile GeO and/or Hf-Ge-O due to the

enhancement effect of Ga impurities especially when the doping concentration is high, which may shrink the $HfO_2$ dielectric layer and severely degrade the interface quality. The higher $J_g$ increase in n-MOS devices shown in Fig. 7.6(b) can be caused by the shrink of $HfO_2$ as well as the more severe Ge updiffusion. Accompanying the more severe interface reactions and inter-diffusion, the generation of large amount of interface states finally leads to the Fermi-level pinning effect.

## 7.5 SUMMARY

In this chapter, we have investigated the thermal stability of Ge MOS devices with 400-700°C PMA treatments. After PMA treatments, a consistent trend with the anneal temperature, in terms of $V_{fb}$ positive shift and $J_g$ increase, has been observed for all the devices on various substrates. It can be attributed to Ge updiffusion into the dielectric as well as the interdiffusion at the interface.

XTEM images show that 600°C PMA treatment sufficiently eliminates the interfacial layer, suggesting that $NH_3$-based nitrided interface is not substantially stable to passivate the Ge surface due to the desorption of volatile species and severe interdiffusion. The inconsistent trend of those devices, in terms of the EOT shrink and the abnormal *C-V* characteristics for n-MOS devices, can be attributed to the more severe desorption process caused by the substrate doping effect which may generate large amount of interface states. In order to improve the thermal stability in high temperature processes, a more stable interface passivation technique is required.

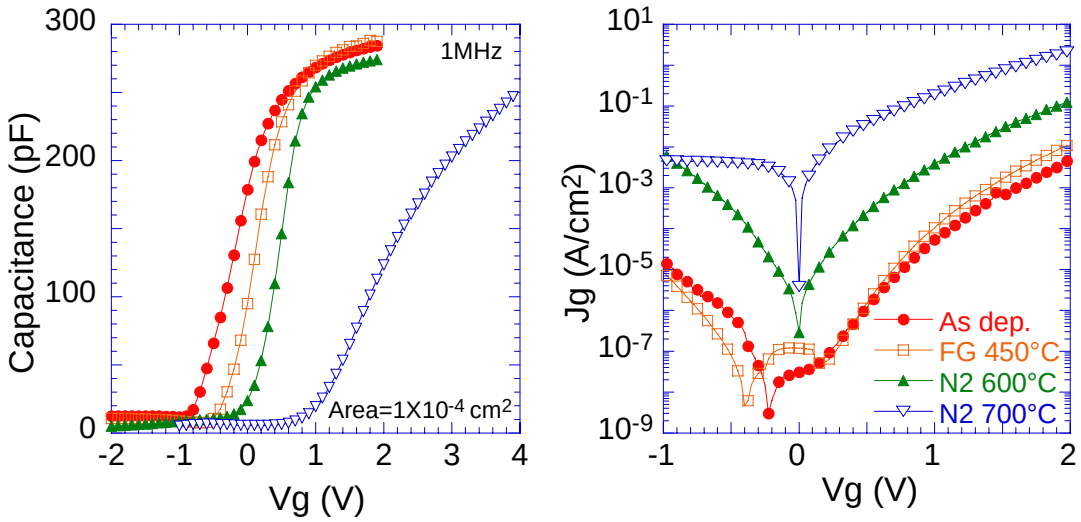



Fig. 7.1 (a) *C-V* and (b) *I-V* characteristics for SN-treated TaN/$HfO_2$/n-Ge stack with forming gas (FG) or $N_2$ anneal at 450°C for 30 min or 600-700°C for 30 sec

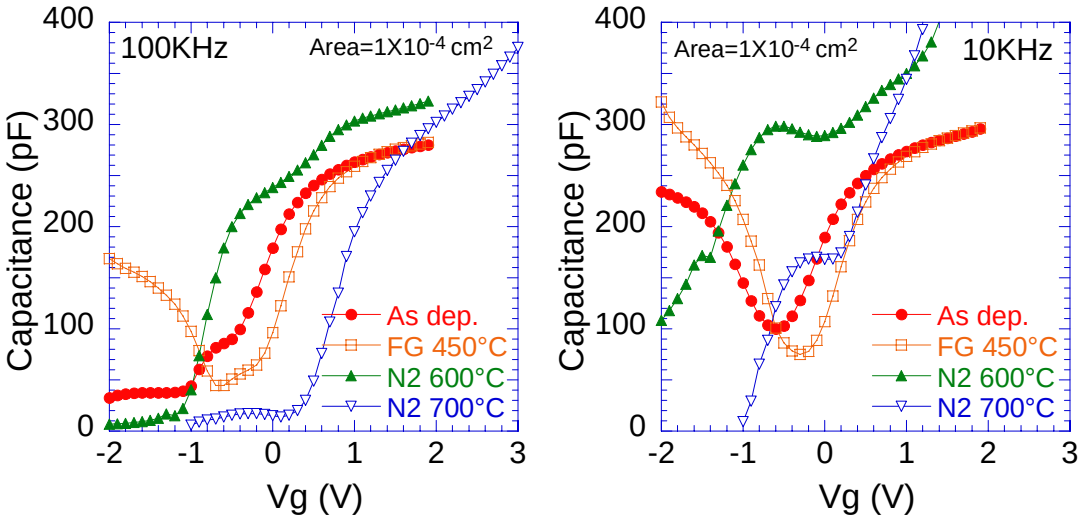



Fig. 7.2 (a) 100KHz and (b) 10KHz *C-V* characteristics for SN-treated TaN/$HfO_2$/n-Ge stack with forming gas (FG) or $N_2$ anneal at 450°C for 30 min or 600-700°C for 30 sec

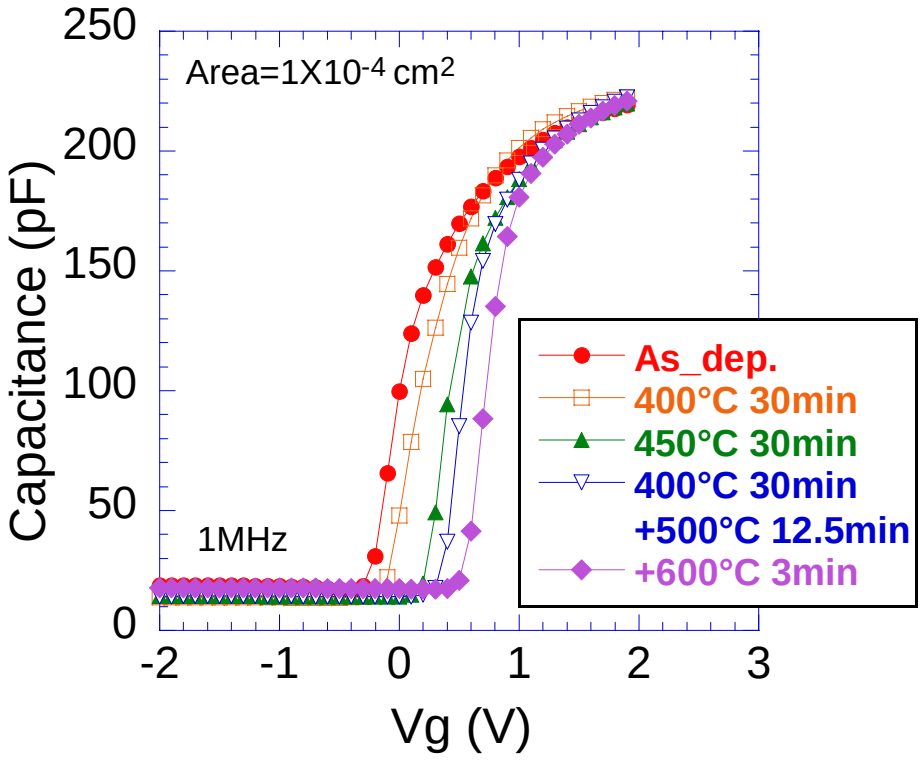



Fig. 7.3 *C-V* characteristics of SiIL/SN-treated TaN/$HfO_2$/n-Ge stack with 400-600°C forming gas anneal

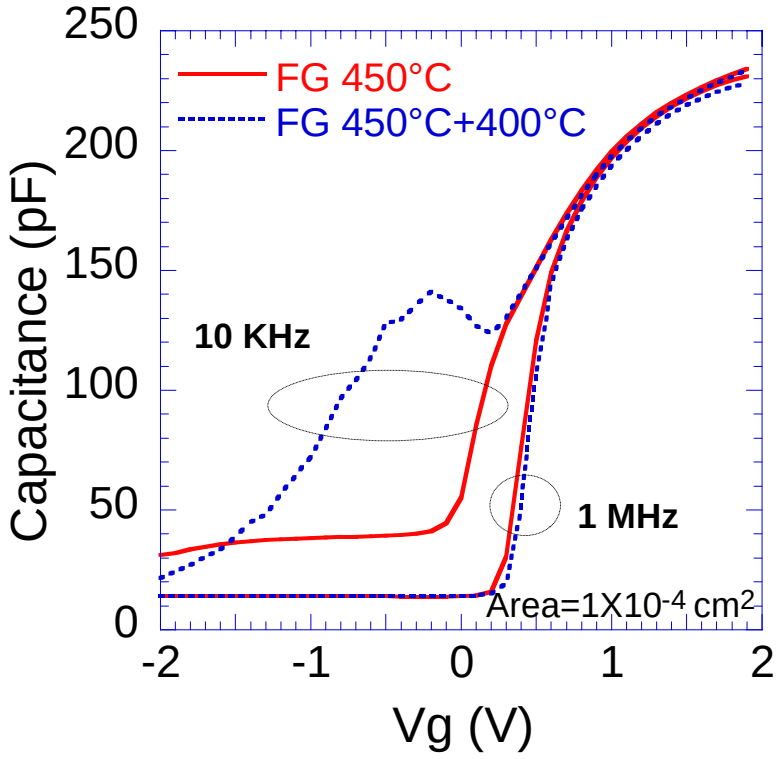



Fig. 7.4 1 MHz and 10 KHz *C-V* characteristics of SiIL/SN-treated TaN/$HfO_2$/n-Ge stack with 450°C 30 min and 450°C 30 min + 400°C 30 min forming gas anneal

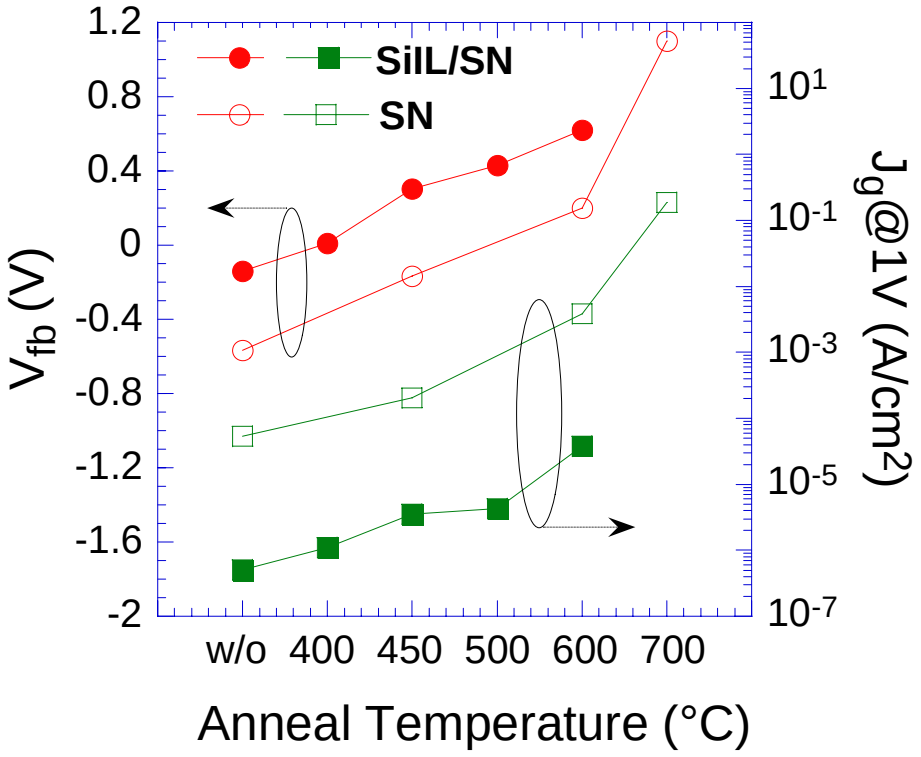
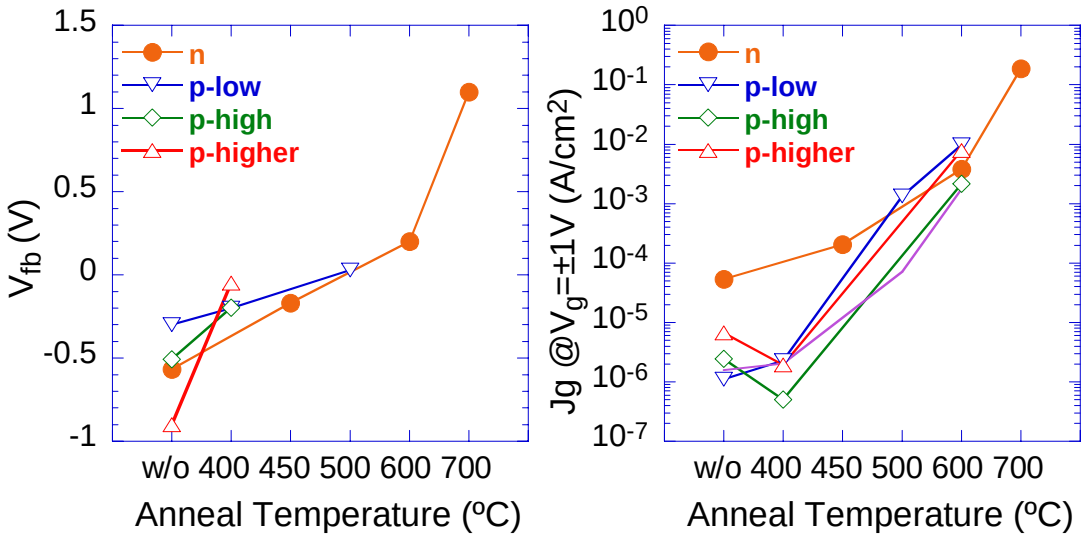



Fig. 7.5 $V_{fb}$ and $J_g$ as a function of the PMA temperature for SN- and SiIL/SN-treated TaN/$HfO_2$/n-Ge stacks




(a) (b)

Fig. 7.6 (a) $V_{fb}$ and (b) $J_g$ as a function of the PMA temperature for Ge MOS devices on different types of substrates. These devices were fabricated with CVD $HfO_2$ and SN treatment. $J_g$ data were taken at $V_g$ = −1 V for n-MOS or 1 V for p-MOS. PMA was carried out at 400°C 30 min, 450°C 30 min, 500°C 1 min, 600°C 30 sec, or 700°C 30 sec in $N_2$ ambient. Due to the abnormal *C-V*s after high-temperature anneal, some $V_{fb}$ data are not extractable.

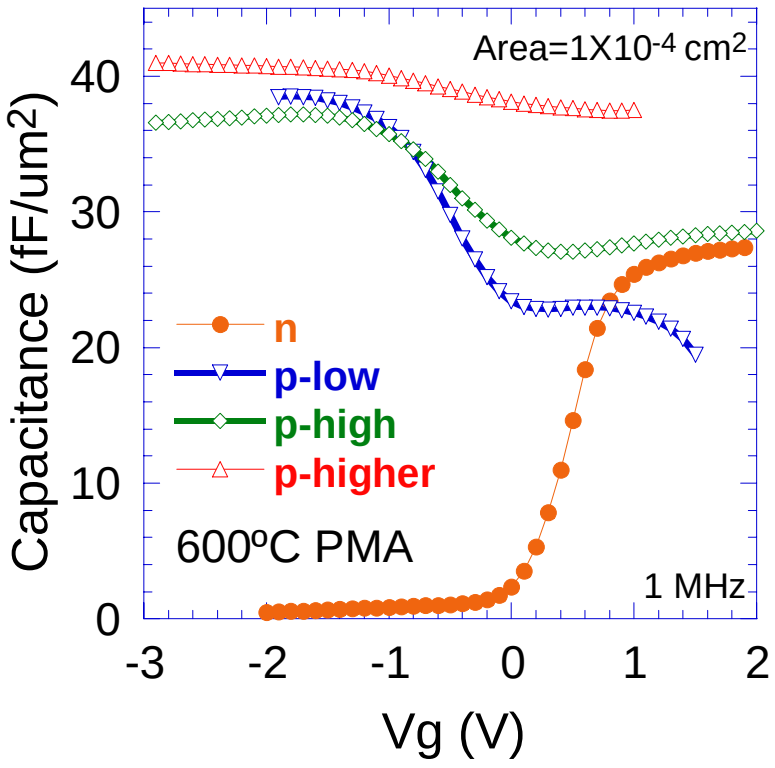
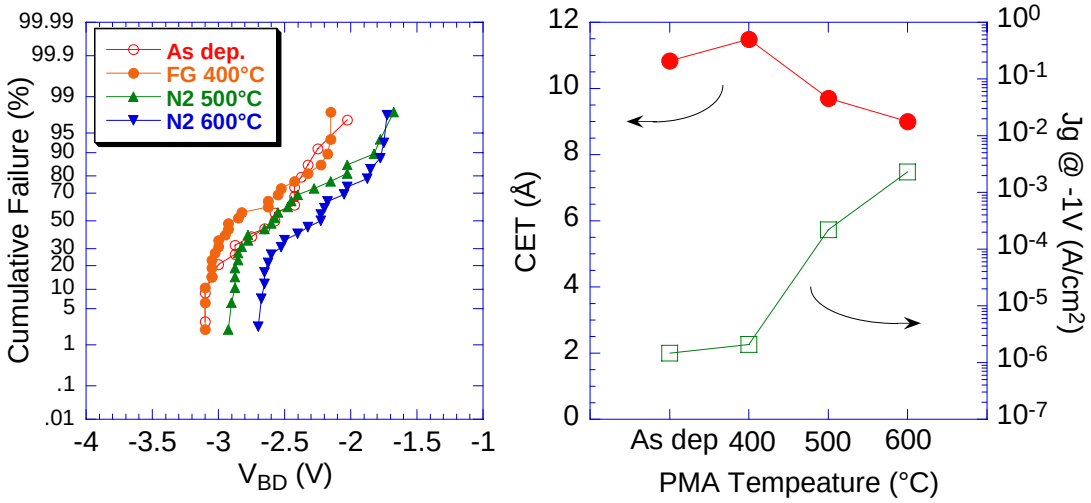



Fig. 7.7 *C-V* characteristics of SN-treated Ge MOS devices on various substrates after 600°C 30 sec PMA treatment




(a) (b)

Fig. 7.8 (a) Distribution of TZBD voltages and (b) CET and $J_g$ at $V_g$ = –1 V after 400-600°C PMA for the SN-treated n-MOS on low doped substrates

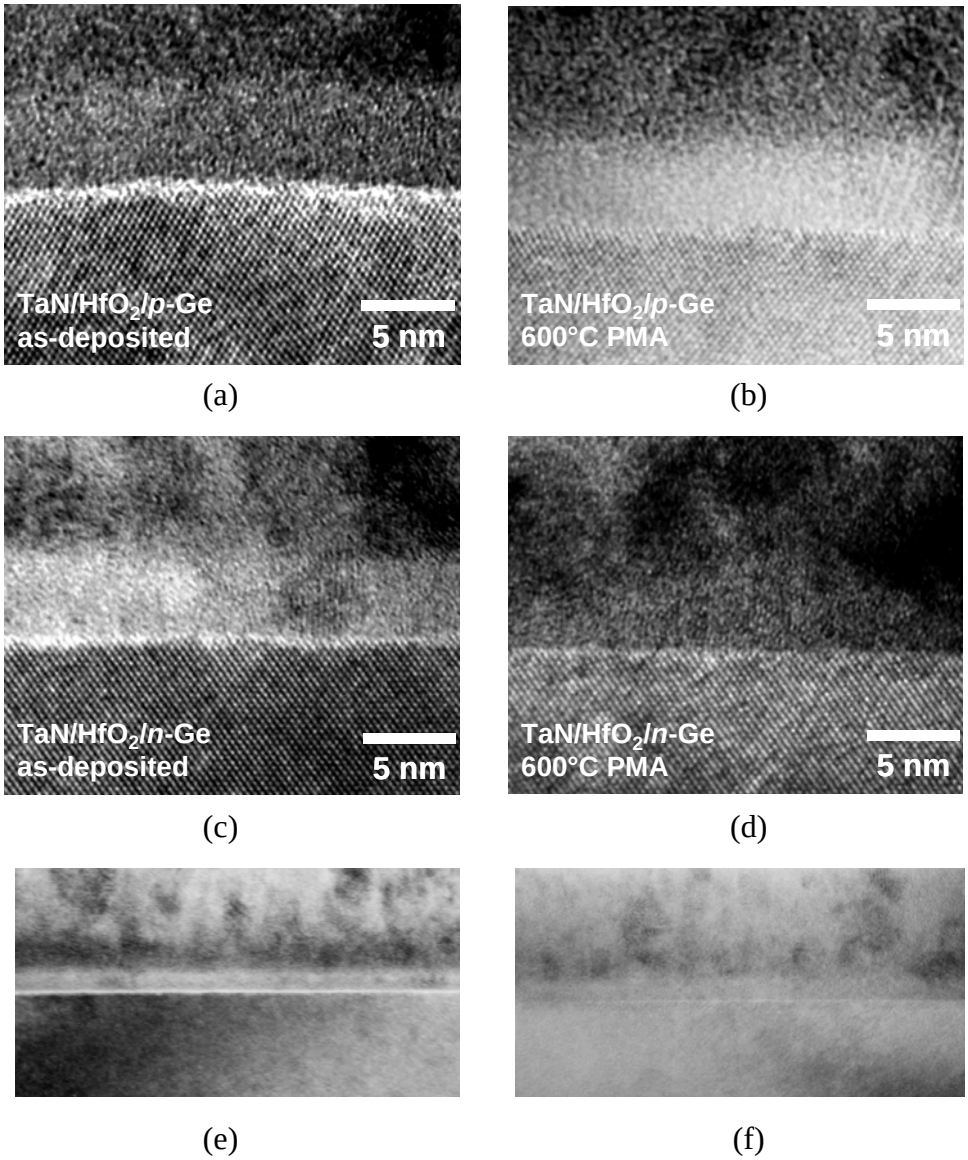



Fig. 7.9 XTEM images of Ar/SN-treated TaN/$HfO_2$ stacks on n- and p- type germanium substrates with and without PMA treatment. (a) and (c): as-deposited; (b) and (d) 600°C PMA annealed; (e) and (f): wide-angle-view images of as-deposited and PMA annealed stacks, respectively

# Chapter 8: Charge trapping and reliability characteristics

## 8.1 INTRODUCTION

Reliability is one of the critical issues for high-κ dielectric applications. There have been a few studies on the reliability characteristics for high-κ gate stacks on germanium (mainly on GOI) substrates [30][92]-[94]. In this work, we investigate the charge trapping and reliability characteristics for the ultra-thin CVD $HfO_2$ gate stack on nitrided germanium for the first time. Both Ge n- and p- MOS have been studied and compared with the Si control devices. Ge substrates with $N_d = 5\times10^{16}$ $cm^{-3}$ and $N_a = 1\times10^{15}$ $cm^{-3}$ were used for p- and n-MOS device fabrication respectively. SN treatment was carried out in $NH_3$ at 550°C for 2 min prior to 5 nm $HfO_2$ deposition. The Si control samples were prepared with 700°C 10 sec anneal in $NH_3$ for effective SN treatment on Si. Finally, all samples received 400°C 30 min forming gas anneal.

## 8.2 COMPARISON OF I-V AND TZBD CHARACTERISTICS

Fig. 8.1 shows the *I-V* characteristics and TZBD voltage distribution for TaN/$HfO_2$ stacks on the nitrided Ge and Si for both the n-MOS and p-MOS devices. The high frequency *C-V* curves (Fig. 8.2) demonstrate an identical EOT of 11 Å for these devices. Both the Ge and Si p-MOS devices exhibit higher gate leakage current than the n-MOS devices since the substrate injection of electrons in p-MOS has a lower barrier height than the gate injection in n-MOS considering the mid-gap work

function of TaN gate electrode. Compared to Si, Ge devices exhibit lower gate leakage current at the same EOT. This can be contributed to the thicker high-κ layer in Ge devices than in Si at the same EOT value since the oxynitride interfacial layer formed on Ge is actually thinner than that on Si due to the desorption of volatile species in the interface reactions on Ge. However, it is found from Fig. 8.1 that Ge n-MOS devices, different from the p-MOS case, do not show significantly lower leakage than Si n-MOS under relatively high gate bias. This is due to the asymmetrical energy band alignment and can be explained by the difference of the electric field across the gate dielectric in Ge/Si n-/p- type devices. Considering a device biased in the strong accumulation regime, the electric field in the dielectric is

$$E_{\mathrm{i}} = \frac{V_{\mathrm{ox}}}{t_{\mathrm{ox}}} = \frac{|V_{\mathrm{g}}| - (\phi_{\mathrm{m}} - \chi_{\mathrm{c/v}})|}{t_{\mathrm{ox}}} \quad (\chi_{\mathrm{c}} \text{ for p-MOS and } \chi_{\mathrm{v}} \text{ for n-MOS}) \qquad (8.1)$$

where $V_{\mathrm{ox}}$ is the voltage across the dielectric stack, , $t_{\mathrm{ox}}$ is the physical thickness of the dielectric, $\phi_{\mathrm{m}}$ is the work function of the gate electrode, $\chi_{\mathrm{c}}$ and $\chi_{\mathrm{v}}$ is the energy level of the conduction and valence band edge of the substrate respectively. For a stacked dielectric structure (e.g., high-κ/interfacial layer) the electric fields in the high-κ layer and in the interfacial layer (IL) are

$$E_{\mathrm{high-k}} = \frac{V_{\mathrm{ox}}}{\mathrm{EOT}} \frac{\varepsilon_{\mathrm{SiO2}}}{\varepsilon_{\mathrm{high-k}}} \quad \text{and} \quad E_{\mathrm{IL}} = \frac{V_{\mathrm{ox}}}{\mathrm{EOT}} \frac{\varepsilon_{\mathrm{SiO2}}}{\varepsilon_{\mathrm{IL}}}, \qquad (8.2)$$

where $\varepsilon_{SiO2}$, $\varepsilon_{high\text{-}\kappa}$, and $\varepsilon_{IL}$ is the dielectric constant of $SiO_2$, high-κ and interfacial layer, respectively. Taking $\phi_m$ = 4.6 V for TaN gate electrode (extrapolated from the $V_{fb}$-EOT plot as shown in Fig. 8.3), $\chi_c$ = 4.0 V for Ge and 4.05 V for Si, $\chi_v$ = 4.66 V for Ge and 5.17 V for Si [11], we have the effective electric field

$$\begin{aligned} E_{eff} &= \frac{V_{ox}}{EOT} = \frac{(|V_g| - 0.6 \text{ or } 0.55\,V)}{EOT} \quad \text{for Ge or Si p-MOS} \\ E_{eff} &= \frac{V_{ox}}{EOT} = \frac{(|V_g| - 0.06 \text{ or } 0.57\,V)}{EOT} \quad \text{for Ge or Si n-MOS} \end{aligned} \tag{8.3}$$

Therefore, with a same gate voltage applied, for p-MOS, Ge or Si device has a similar electric field but for n-MOS Ge device has a higher electric field — which may offset the advantage from its thicker $HfO_2$/thinner IL structure (with the same EOT) when the impact of the electric field on gate leakage becomes significant under relatively high gate bias.

It is also noticed that in Ge p-MOS devices, when the gate voltage is higher than 3.25 V, Fowler-Nordheim (FN) tunneling is the dominant mechanism, and a sudden increase of the slope of the *I-V* curve can be found. A local peak at $V_g$ = –0.4 V is observed in the *I-V* of Ge n-MOS, which is believed to be caused by defects in the bandgap of the interfacial layer.

Fig. 8.1 also shows the different TZBD voltages ($V_{bd}$) for Ge and Si devices. For n-MOS, Ge devices exhibit lower breakdown voltages than Si devices, which can be attributed to the higher electric field in Ge n-type devices. The slow trap densities ($D_{st}$) in those n-MOS devices were extracted by dynamic *I-V* method [66]

and are shown in Fig. 8.4 (a). Similar $D_{st}$ levels were found in both the Ge and Si devices. Interface state densities ($D_{it}$) extracted by Hill-Coleman method [95], are shown in Fig. 8.4 (b). Ge devices exhibit much higher $D_{it}$ (~ $5\times10^{12}$ /cm$^2$-eV) than Si devices (~ $5\times10^{11}$ /cm$^2$-eV). Although the interface quality is worse in the Ge devices, it is believed that this is not a major factor affecting the breakdown strength since the Ge p-MOS devices exhibit a relatively higher $V_{bd}$ than the Si p-MOS, which should be contributed to the lower tunneling current in Ge devices benefiting from the thicker high-κ layer.

### 8.3 TDDB CHARACTERISTICS

The typical time-dependent dielectric breakdown (TDDB) characteristics under constant-voltage-stress (CVS) for the Ge n-MOS devices are shown in Fig. 8.5. Hard breakdown is observed, and there is no significant charge trapping during stress. The stress-induced leakage current (SILC) characteristics of Ge n-MOS at a stress voltage of –2.0 V and –2.7 V ($E_{eff}$ = 18 MV/cm and 24 MV/cm respectively) are displayed in Fig. 8.6 and only slight leakage current increase is observed for the –2.7 V stress. The TDDB characteristics for the Ge p-MOS devices are shown in Fig. 8.7. Significant charge trapping is presented when stressing the p-MOS. To investigate the mechanism of this trapping, a p-MOS device was stressed under various gate voltages from 2.0 to 3.4 V, as shown in Fig. 8.8. *I-V* characteristics after each stress were monitored and are displayed in Fig. 8.9. No significant charge trapping is found for stresses below 3.0 V. Above 3.0 V, the trapping becomes significant. However, the gate leakage currents measured immediately after every stress (up to 3.2 V) keep

almost constant, as shown in Fig. 8.9. This indicates that no significant trap generation is accompanied. The presence of a trapping level in $HfO_2$ dielectric near the conduction band edge may explain this phenomenon. As shown in Fig. 8.10, when the gate bias is sufficiently high (near or above the FN tunneling region) and the Fermi level sweeps across this trapping level, it will be charged with electrons and causes the gate leakage to increase. Due to its high energy level, the trapping level can be decharged quickly as the gate bias drops. The fast decharging can be observed from the 3.3-V-stress curve in Fig. 8.7 — the leakage current decreased dramatically as the stress process was interrupted. This charge trapping phenomenon has also been observed in the Si p-type devices, confirming that it's resulting from the defects in the high-κ dielectric layer.

The critical defect densities ($N_{bd}$) were extracted from the stress-induced leakage current ($\Delta J_g/J_{g0}$) just prior to breakdown. Si and Ge n-MOS show similar $N_{bd}$ around 0.4. $N_{bd}$ of the p-MOS device is much higher than that of the n-MOS by a factor of $10^2$, mainly due to the severe trapping observed.

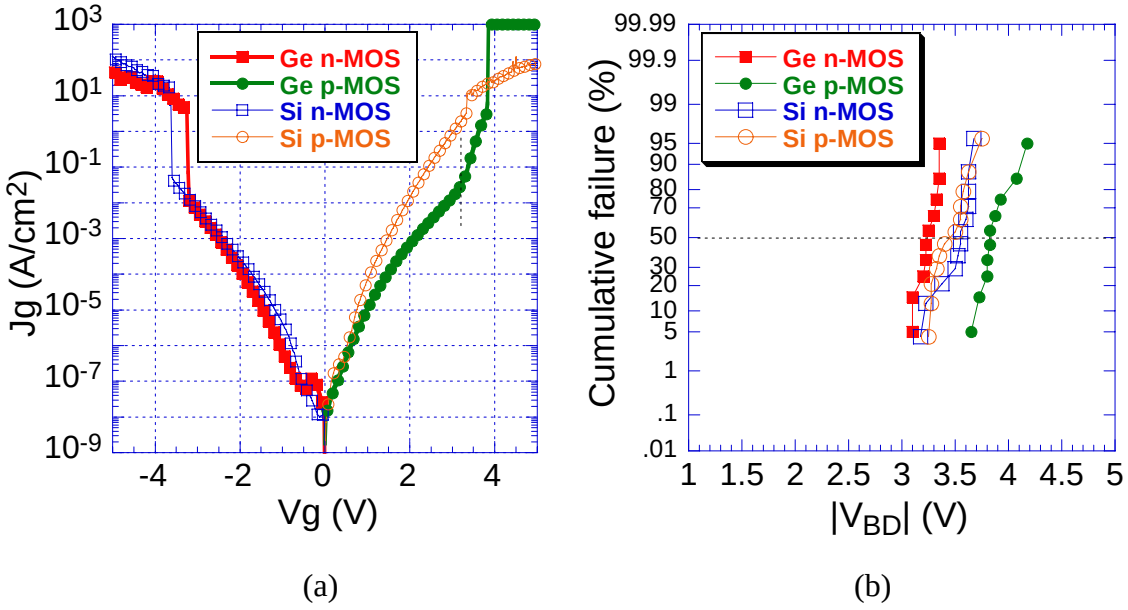
The distributions of the time-to-breakdown ($T_{bd}$) of the Ge n- and p-MOS devices are shown in Fig. 8.11. TDDB lifetime is accelerated to low voltage following $V_g$ model, which claims that breakdown of ultra-thin oxide is determined by the maximum electron energy driven by gate voltage [96]. As shown in Fig. 8.12, the maximum allowed operating voltage at room temperature with a ten-year lifetime are projected to be 2.1 V for Ge n-MOS with an EOT of 11 Å. Considering the higher electric field across the insulator layer in the Ge n-MOS devices under the same stress voltage, this result is comparable to that of the Si n-MOS devices, which

is projected to be 2.3 V for a ten-year lifetime. The operating voltage for the Ge p-MOS is projected to be 2.8 V, which is much higher than for the Ge n-MOS. However, we may not conclude that there is stress polarity-dependence in the break-down strength or breakdown mode since the bias across the whole dielectric layer is actually similar under their negative or positive CVS conditions (e.g., |3.3–0.6| V for positive stress and |2.7–0.06| V for negative stress). A much higher voltage-acceleration coefficient ($\gamma$) (11 dec/V) was found in Ge p-MOS than in Ge n-MOS (8 dec/V), which is attributed to the significant charge trapping and dramatically increased leakage under a stress in the FN tunneling region. Considering this effect, the long term reliability should be even more optimistic for the Ge p-MOS devices when the devices are operated at a much lower voltage in the direct tunneling region. Finally, we have to note here that the breakdown characteristics of the Si p-type control devices could not be reliably obtained in this experiment because under high voltage stress, the relatively high $J_g$ in the Si p-MOS device causes the impedance of the MOS device comparable to the series resistance of the substrate. It can be seen in Fig. 8.1 that the gate leakage current of the Si p-MOS device after breakdown is comparable to that before breakdown. This reduces the actual bias applied on the gate stack, especially for this p-MOS case that the trapping becomes significant and leakage continually increases during stress.

## 8.4. SUMMARY

Long term reliability is investigated for the Ge n- and p-MOS devices with ultra-thin MOCVD $HfO_2$ dielectric and $GeO_xN_y$ interfacial layer formed by $NH_3$-

based SN treatment. The projected operation voltage for a ten-year lifetime is 2.1 V at room temperature in the Ge n-MOS with EOT = 11 Å, comparable to the control Si n-MOS with SiON interfacial layer. The Ge p-MOS exhibits a much higher projected operation voltage of 2.8 V with 11 Å EOT. No significant charge trapping and SILC is observed in the Ge n-MOS. Significant charge trapping is observed in both the Ge and Si p-MOS when the stress voltage is near the FN tunneling region and the voltage acceleration factor increases to 11 accordingly. A trap level near the conduction band edge of the $HfO_2$ dielectric is believed to be responsible for this significant trapping. Considering this effect, the long term reliability for the Ge p-MOS will be even more optimistic at the normal operation condition. The CVD $HfO_2$ with SN treatment on Ge has been proved robust against TDDB stress.




(a) (b)

Fig. 8.1 (a) *I-V* characteristics and (b) TZBD voltage distribution for Ge and Si n- and p- MOS devices

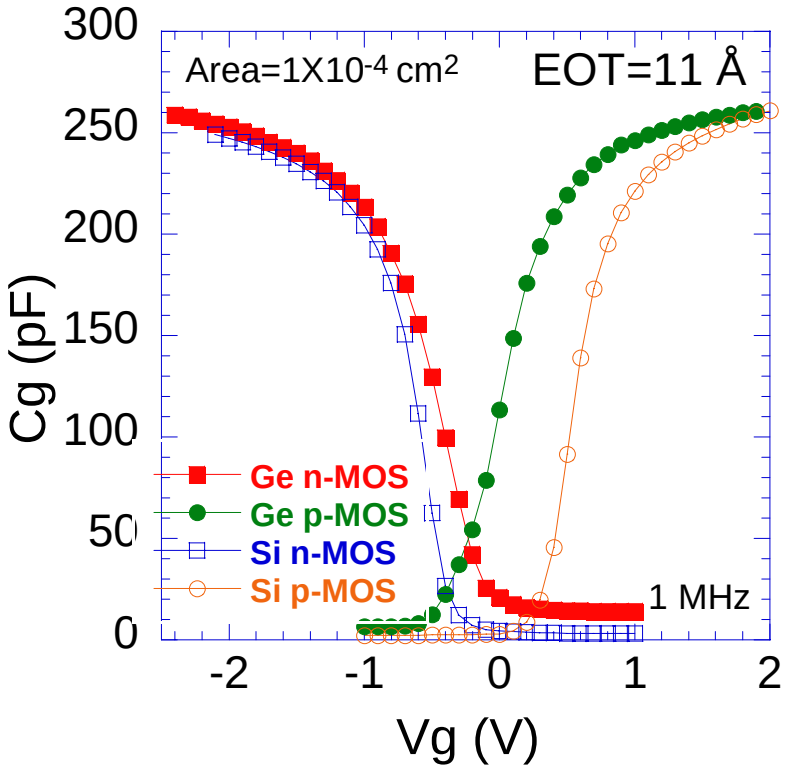
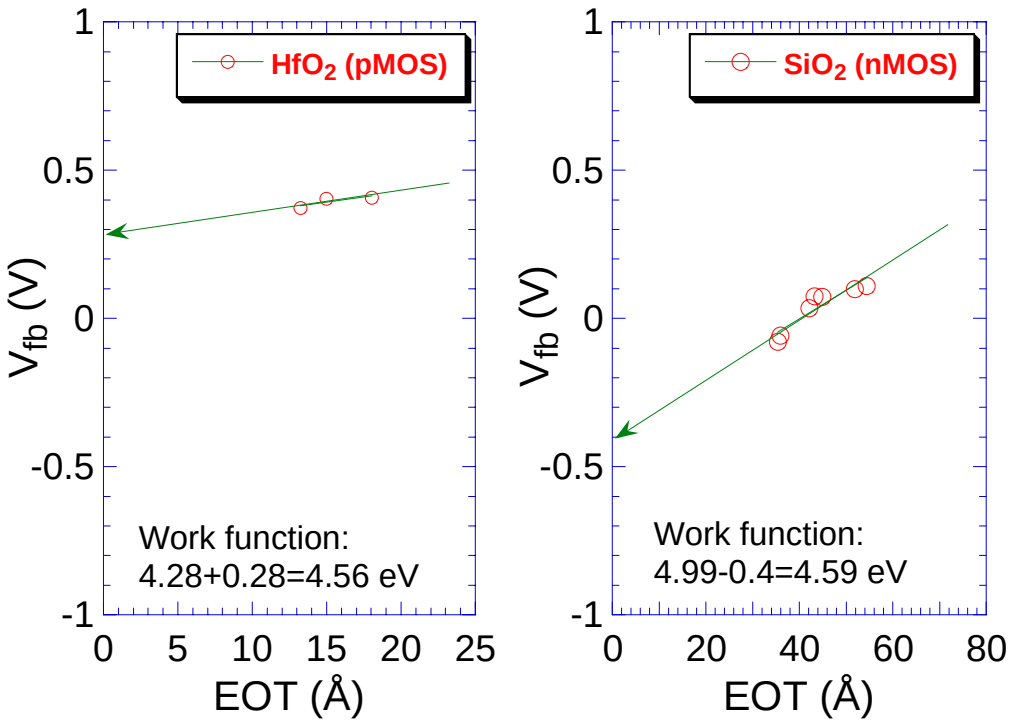
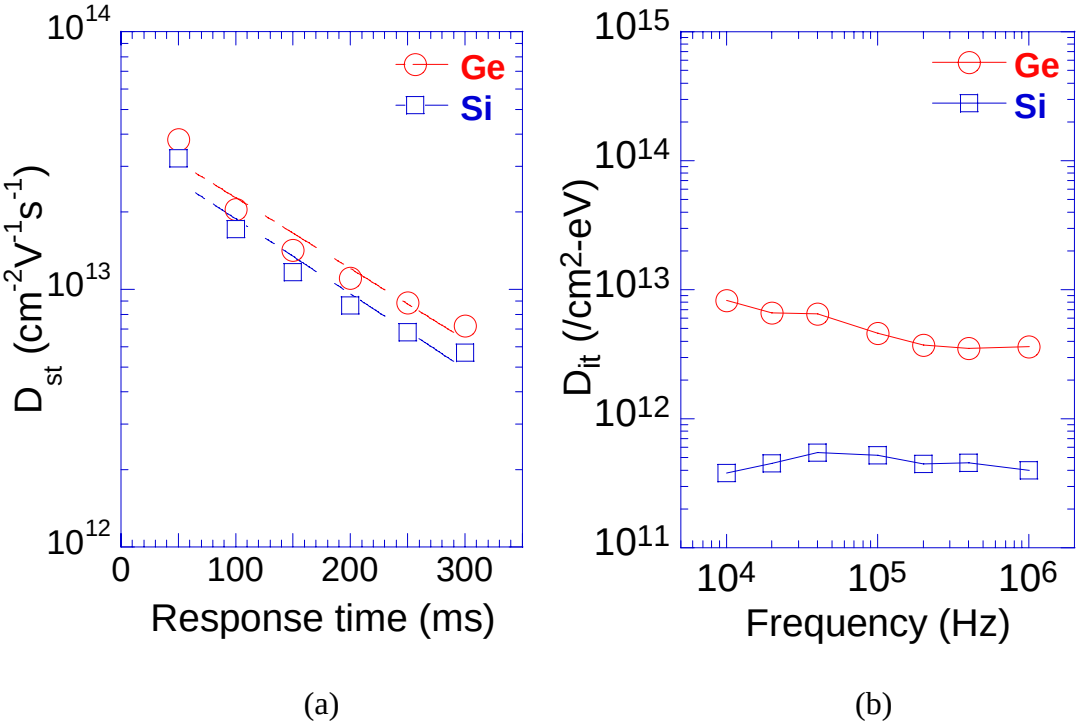



Fig. 8.2 High frequency *C-V* characteristics for Ge and Si n- and p- MOS devices




(a) (b)

Fig. 8.3 $V_{fb}$-EOT plots for PVD TaN gated (a) Si p-MOS devices with $HfO_2$ as the dielectric and (b) Si n-MOS devices with $SiO_2$ as the dielectric




(a) (b)

Fig. 8.4 (a) Slow trap densities and (b) interface state densities (right) for Ge and Si MOS devices

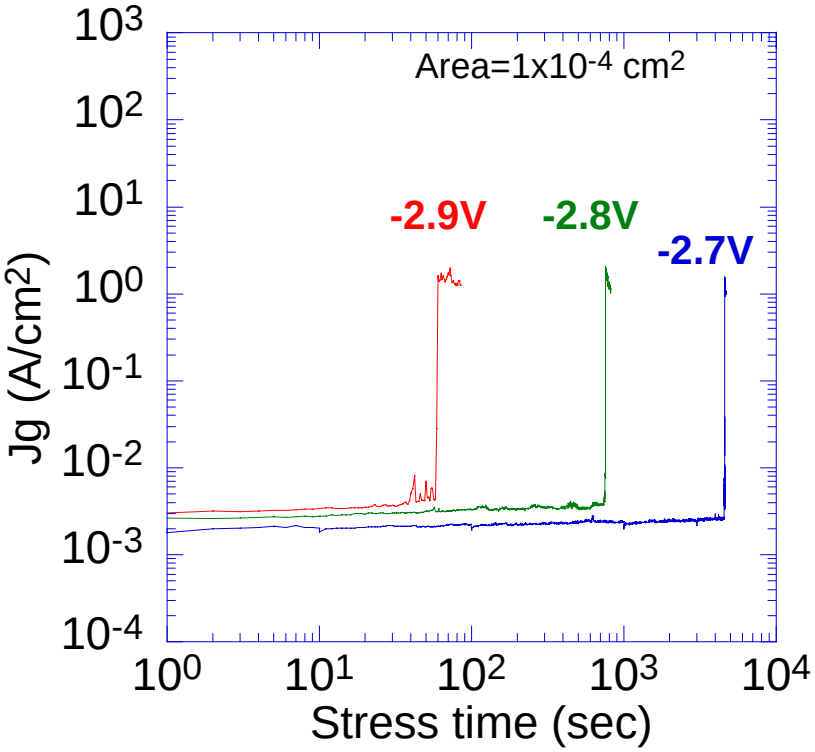



Fig. 8.5 Charge trapping and breakdown characteristics for Ge n-MOS devices under negative CVS

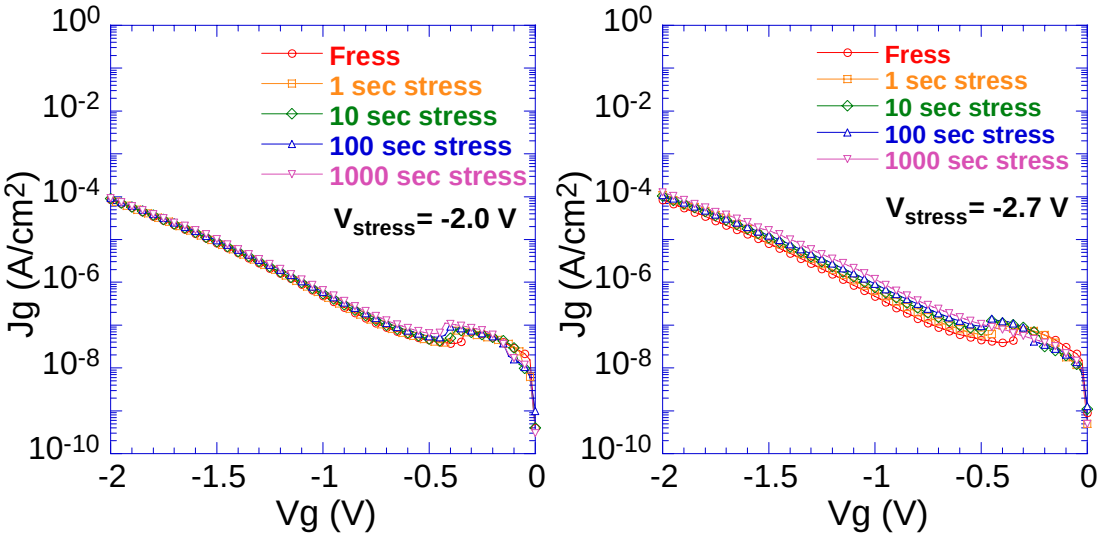



Fig. 8.6 SILC characteristics for Ge n-MOS devices under –2.0 V and –2.7 V stresses

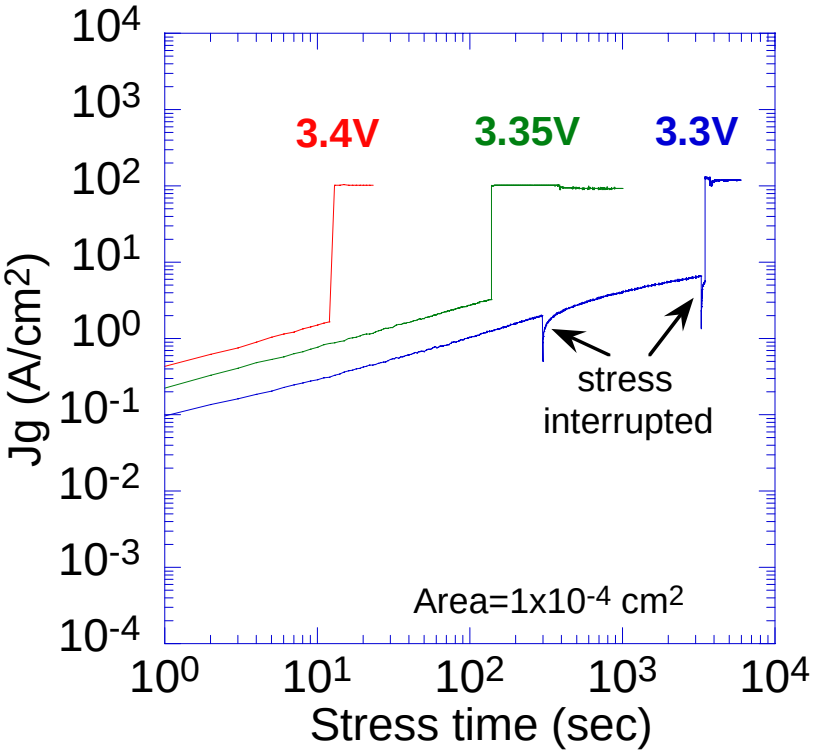



Fig. 8.7 Charge trapping and breakdown characteristics for Ge p-MOS devices under positive CVS. The sharp drops of the gate leakage current under 3.3 V stress occurred after the stress was interrupted.

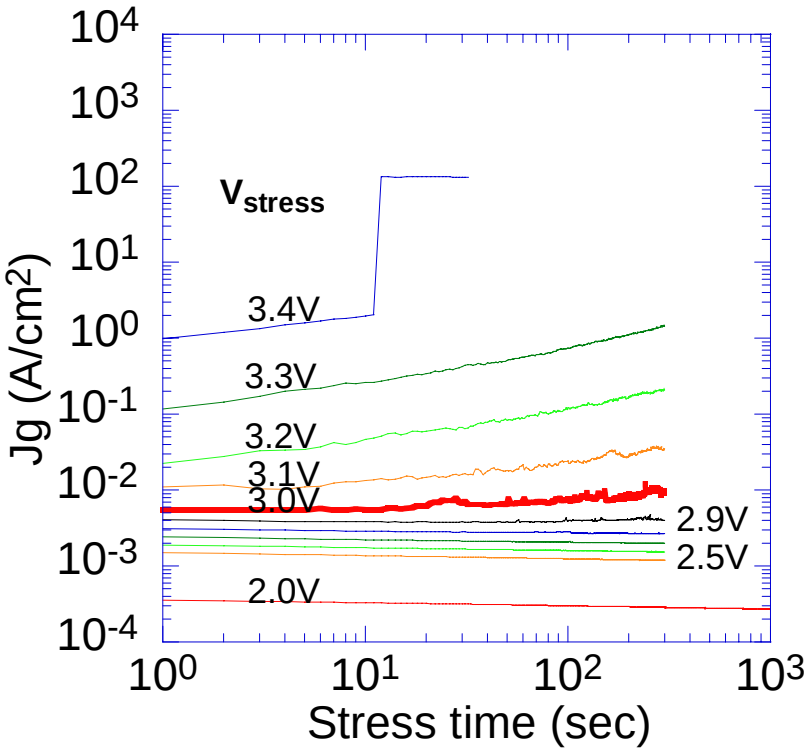



Fig. 8.8 Gate leakage currents for Ge p-MOS device under positive CVS from 2.0 V to 3.4 V

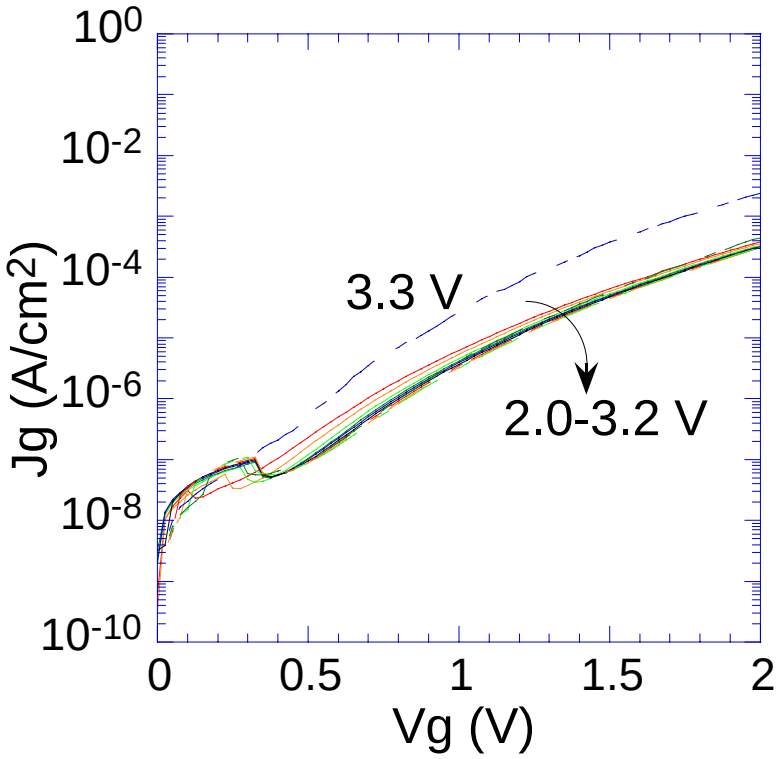



Fig. 8.9 *I-V* characteristics of Ge p-MOS device measured immediately after the stresses from 2.0 V to 3.3 V

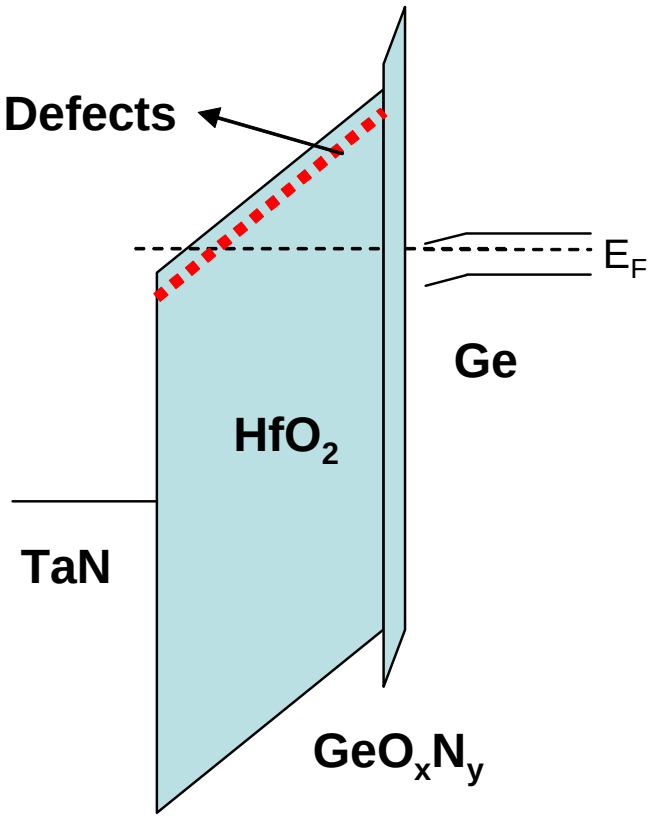



Fig. 8.10 Band diagram of the TaN/$HfO_2$/$GeO_xN_y$/n-Ge stack at a voltage in FN tunneling regime. The presence of a defect level near the conduction band of $HfO_2$ is believed resulting in the significant charge trapping under stress

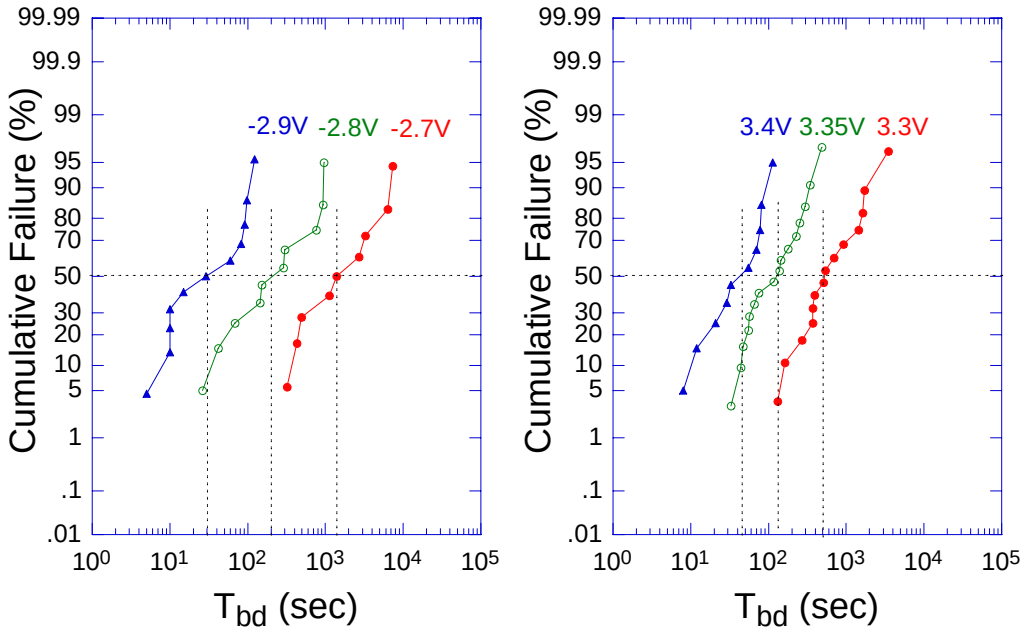



Fig. 8.11 Distributions of the time-to-breakdown ($T_{bd}$) for (a) Ge n-MOS and (b) Ge p-MOS devices

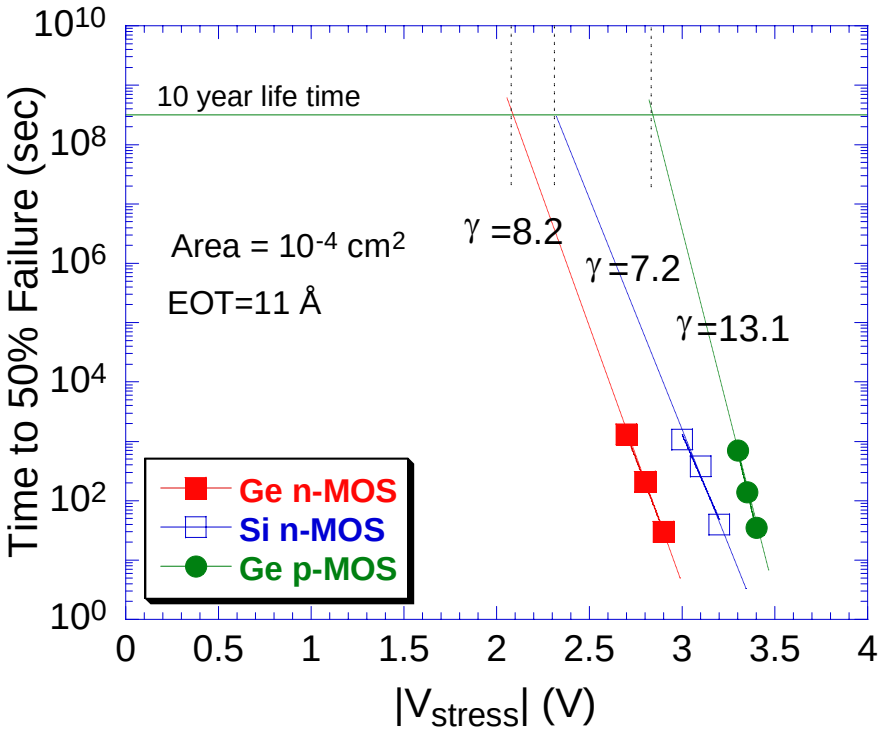



Fig. 8.12 TDDB lifetime projection for Ge n- and p- MOS devices and Si n-MOS devices

# Chapter 9: Conclusion

## 9.1. CONCLUSIONS OF THIS RESEARCH

This dissertation investigates the fabrication and characteristics of MOS devices built on germanium substrates, with $HfO_2$ as the gate dielectric and TaN as the gate electrode. Taking advantage of the high carrier mobility in germanium channel and sub-nm EOT scaling ability of high-κ/metal gate stack, it offers a possible solution for future advanced CMOS applications to further boast the driving current for faster operations. Successful fabrication for both p- and n-channel germanium MOSFET devices has been developed and 1.8X enhancement of peak mobility in p-channel and 2.5X enhancement in n-channel over silicon control devices have been demonstrated in this study.

This study shows that the surface treatment is critical in germanium device fabrication, which is mainly resulting from the unstable and poor quality native germanium oxide. Inappropriate surface cleaning methods may cause rough surface and leaky gate stack. Cyclical HF-dip method has been demonstrated a good method which produces smooth surface and good electrical properties.

Proper surface passivations prior to dielectric layer deposition have been proved indispensable in order to prevent the growth of native germanium oxide and germanium updiffusion into the dielectric layer. $NH_3$-based surface nitridation, which forms a more stable $GeO_xN_y$ layer, is an effective passivation technique. Compared to direct deposition of high-κ dielectric on germanium, using this

technique has led to dramatically improved device performance, in terms of thinner EOT, lower gate leakage and lower trap densities. MOSFETs based on this technique have been successfully fabricated.

Other surface treatment techniques have also been investigated. *In situ* cleaning by Ar anneal, which intends to remove the residual native oxide grown immediately after wet-cleaning, can reduce the interface state density and slow trap density. Silicon interlayer passivation, by forming a thin (several monolayer) silicon layer between the high-κ dielectric and the substrate, improves devices' electrical properties with better interface quality, smaller hysteresis and reduced *C-V* frequency dispersion.

Successful fabrication of n-channel MOSFETs on lightly doped germanium substrates and the analysis based on the work by other groups have shown that high substrate doping level is possibly responsible for the reported poor performance in bulk germanium n-MOSFETs. The relatively fast diffusion of dopants and germanium atoms in bulk germanium may form structural defects near the surface, which may enhance the channel scattering and reduce the lifetime of minority carriers and finally cause significantly degraded channel mobility and abnormal low frequency *C-V* shape in high frequency measurements.

By studying the electrical properties of the devices built on different types of germanium substrates and processed with different growth methods and surface treatments, it is concluded that two competing processes occurring at the interface, named "oxide growth" and "oxide desorption", determine the formation of interfacial layer and also affect Ge updiffusion. Temperature, oxygen supply, and substrate

dopant type and concentration play important roles in the two processes, which finally affect the electrical properties of germanium devices. Doped p-type (Ga) and n-type (Sb) impurities may enhance the different process and cause the variations in the interfacial layer formation and so on in electrical properties.

Thermal stability has been investigated. $V_{fb}$ positive shift and gate leakage increase with increased PMA temperature have been observed in both n- and p-type devices. This degradation should be caused by germanium updiffusion into the dielectric layer. N-MOS devices exhibit EOT shrink and much degraded *C-V* characteristics after PMA, which is believed caused by the substrate doping effect. The shrink of $GeO_xN_y$ interfacial layer after 600°C PMA indicates that SN passivation is not sufficiently stable in high temperature processes.

Charge trapping and long term reliability study indicates that $HfO_2$ dielectric with SN treatment on germanium is robust against TDDB stress and the long term reliability (TDDB) is not a concern for germanium MOS devices.

## 9.2 SUGGESTIONS FOR FUTURE RESEARCH

- **Alternative high-κ dielectrics (higher-k) on germanium**

Most of the recent work in the area of high-κ/Ge MOSFETs is focused on $HfO_2$/Ge structure. However, one disadvantage of $HfO_2$ dielectric is the crystallized structure. $HfO_2$ on Ge shows polycrystalline phase in either CVD [51][52][97], ALD [98][99][100] or PVD [54] processes. The grain boundaries in the crystalline stacks often act as an oxygen diffusion route [101], which may help Ge updiffusion and desorption and weaken the stacks' thermal stability. Zr-silicate/Ge stack was recently

reported having improved thermal stability due to the amorphous phase of the dielectric [102]. However, the EOT scalability may be impaired due to the lower dielectric constant of high-κ-silicate materials. Higher-κ dielectrics like HfTiO and HfTaTiO on Si have been studied recently [103][104]. Not only having a higher dielectric constant than that of the traditional high-κ materials like $HfO_2$ and $ZrO_2$ (~ 25), these materials also showed superior thermal stability with crystallization temperature above 900°C. Improved channel mobility and trapping characteristics have also been reported.

Based on the above, higher-κ materials on Ge can possibly offer better performance, including thermal stability, channel mobility and the EOT scalability as well. Higher-κ/Ge stacks are worth to be investigated in the future.

- **Optimize IL passivation techniques and S/D activation**

Several surface passivation techniques have been demonstrated in this dissertation. The efficiency of surface passivation not only depends on the technique itself, but also the post thermal budget. Recent study shows that it is easy to well activate of p-type dopants (boron) in Ge at or below 400°C [90][91]. However, it is challenging to activate n-type dopants (As and P) very well. 500-600°C annealing cannot sufficiently activate the dopants and obtain satisfactory low S/D sheet resistance, partially due to dopant loss and solid solubility limits [78][105][106][107]. It is also argued that the reported unsatisfactory performance of n-channel devices might be related to the poor S/D implantation and activation [106]. Gate-last approach is able to alleviate this issue, but the additional process steps will increase

the complexity and difficulties in fabrication and results in additional fabrication costs and yield issues. S/D techniques also include novel metal-germanide Schottky S/D which is assumed to reduce S/D resistance. Successful fabrications of Ge p-MOSFET with Pt- or Ni- germanide S/D have been demonstrated, though the performance needs further improvement. However, for Ge n-MOSFET, schottky S/D may not be a solution due to work function pinning of metal/germanium contact [111][112].

As a development of the SiIL technique [113], high-κ/Si/Ge and high-κ/Si/Ge/Si stacks have been investigated with a layer of Si (from several monolayers to 5 nm) on top of Ge channel in order to take advantage of high-mobility Ge channel but with less degraded interface [114][115][116][117]. The results show that the optimal thickness of the Si layer depends on each process and more investigations are needed to find out the optimal stacks.

Therefore, combining those factors and finding out the optimal passivation technique and process temperature, especially for n-type devices, still need lots of efforts.

- **Strained germanium and GOI**

Similar to strained silicon, strained germanium is able to boost surface channel mobility and improve transistors' driving current. In MOSFETs with a 10-nm order gate length, moreover, thin-body Ge-on-insulator (GOI) channels can provide further high-speed operation under ballistic transport [118] as well as the advantages inherent to thin-body structures, such as low parasitic capacitance and

immunity for short channel effects. The suppression of the junction leakage current by thin-body structure is another benefit for channel materials with smaller bandgap like Ge. Fully depleted structures using an intrinsic channel also contribute to the enhancement of carrier mobilities. Strained GOI devices have been developed with much enhanced mobility [116][117][119]. Optimized gate stack engineering in strained GOI in the future may lead to the final realization of Ge channel devices in advanced VLSI applications.

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# Vita

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