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Effects of Scaling and Grain Structure on Electromigration Reliability of Cu Interconnects

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Effects of Scaling and Grain Structure on Electromigration Reliability of Cu Interconnects

by

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Dissertation

Presented to the Faculty of the Graduate School of
The University of Texas at Austin
in Partial Fulfillment
of the Requirements
for the Degree of

Doctor of Philosophy

The University of Texas at Austin
December, 2010

Dedication

To my family

Acknowledgements

First of all, I would like to thank Professor Paul S. Ho for his guidence and support for my research in the Laboratory for Interconnect and Packaging. His vision and encouragement are the most cirtical drving force for me to explore in the exciting field of semiconductor interconnects reliability. I am deeply indebted to him and truly appricate his teaching and advising during the past five years. I also want to thank Dr. Jack Lee, Dr. Paulo J. Ferreira, Dr. Emanuel Tutuc and Dr. Martin Gall, for serving as my committee members.

I would like to thank Dr. Oliver Aubel and Dr. Christian Hennesthal from GLOBALFOUNDRIES at Dresden Germany for providing the test samples as well as fruitful discussions, otherwise this work would have been impossible.

I want to thank Dr. Jang-Hi Im for his help and suggestions to my reaserch. Special thanks to Ms. Jo Ann Smith for her help and support in the past few years. I also want to thank Dr. Jiping Zhou for his valuable help in my transmission electron microscopy work.

I want to extend my thanks to my colleagues and friends in the Laboratory of Interconnect and Packaging for their advices and discussion of my research, for their friendship, and for providing me such a friendly and collaborative working environment, making my graduate life enjoyable.

Finally, I want to deeply appreciate my parents, Peixin Zhang and Qiulian Wang, for their endless support and understanding. I would like to thank my husband Feng Zhou for his love, sacrifice and encouragement, and my little son Anthony Zhou for bringing so much fun in my life.

Effects of Scaling and Grain Structure on Electromigration Reliability of Cu Interconnects

Publication No._____________

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The University of Texas at Austin, 2010

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Electromigration (EM) remains a major reliability concern for on-chip Cu interconnects due to the continuing scaling and the introduction of new materials and processes. In Cu interconnects, the atomic diffusion along the Cu/SiCN cap interface dominates the mass transport and thus controls EM reliability. The EM lifetime degrades by half for each new generation due to the scaling of the critical void volume which induces the EM failure. To improve the EM performance, a metal cap such as CoWP was applied to the Cu surface to suppress the interfacial diffusion. By this approach, two orders of magnitude improvement in the EM lifetime was demonstrated. For Cu lines narrower than 90 nm, the Cu grain structure degraded from bamboo-like grains to polycrystalline grains due to the insufficient grain growth in the trench. Such a change in Cu grain structures can increase the mass transport through grain boundaries and thus degrade the EM performance. The objective of this study is to investigate the scaling effect on EM lifetime and Cu microstructure, and more importantly, the grain structure effect on EM behaviors of Cu interconnects with the CoWP cap compared to those with the SiCN cap only.

This thesis is organized into three parts. In the first part, the effect of via scaling on EM reliability was studied by examining two types of specially designed test structures. The EM lifetime degraded with the via size scaling because the critical void size that causes the EM failure is the same with the via size. The line scaling effect on Cu grain structures were identified by examining Cu lines down to 60 nm in width using both plan-view and cross-sectional view transmission electron microscopy.

In the second part, the effect of grain structure was investigated by examining the EM lifetime, statistics and failure modes for Cu interconnects with different caps. A more significant effect of the grain structure on EM characteristics was observed for the CoWP cap compared to the SiCN cap. For the CoWP cap, the grain structure not only affected the mass transport rate along the Cu line, but also impacted the flux divergence site distribution which determined the voiding location and the lifetime statistics.

Finally, the effect of grain structure on EM characteristics of CoWP capped Cu interconnects was examined using a microstructure-based statistical model. In this model, the microstructure of Cu interconnects was simplified as cluster and bamboo grains connected in series. Based on the weakest-link approximation, it was shown that the EM lifetime and statistics could be adequately modeled by combining the measured cluster length distribution with the EM lifetime-cluster length correlation for each individual failure unit.

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Chapter 1: Introduction

During the past decade, the dimensions of the silicon devices and the on-chip interconnects have been progressively decreasing to increase the signal propagation speed and the device density. The signal delay of an integrated circuit is composed of two parts: the gate delay of the active front-end devices and the wiring delay of the back-end of line interconnects. As scaling continues, the gate delay is reduced due to the reduction in the gate length (device size). On the contrary, the interconnect delay (known as the RC delay) continues to increase and becomes the bottleneck for the overall chip performance. To reduce the RC delay, Cu was proposed and first implemented by IBM in 1998 [Rosenberg 2000, Edelstein 1997] to replace the Al-based interconnects for reducing the interconnect wiring resistance. To further reduce the RC delay, low-*k* dielectric materials were introduced to reduce the intra- and inter- layer capacitance. In addition to having a lower electrical resistivity than Al, Cu interconnects also have a higher resistance to electromigration (EM). This comes about because Cu has a higher melting point of 1083 ^{o}C than Al, which is of 660 ^{o}C. At the same temperature, Cu possesses a much lower diffusivity, resulting in a significant increase in EM reliability.

The implementation of the Cu/low-*k* interconnects requires the development of a new process for fabricating the interconnect structure. This is the “damascene” process or the “in-laid” process where new materials and integration methods have to be implemented. The new fabrication process together with the requirement of continuous device scaling raises serious material and reliability concerns for the development of the Cu/low-*k* interconnects. The material concerns come primarily from the low-*k* dielectrics, which in comparison with the silicon dioxide, have much weaker thermomechanical properties and are often subjected to process-induced damages. The reliability concerns can be attributed to the Cu/low-*k* integrated structure as well as to the stringent scaling requirements. This has raised new reliability issues regarding EM, stress migration (SM), and time dependent dielectric breakdown (TDDB) as continuing scaling requires higher current densities, smaller interconnect dimensions and porous low-*k* dielectric materials. As we move forward beyond the 45 nm and the 32 nm technology nodes, the reliability of the Cu/low-*k* interconnects has to be carefully examined and constantly re-evaluated. This research work will focus on EM reliability issues of Cu/low-*k* interconnects for sub-100 nm technology nodes.

1.1 THE DAMASCENE PROCESS

The introduction of Cu brings significant challenges to the BEOL processing. First of all, Cu cannot be patterned using the conventional reactive ion etching (RIE) process due to the lack of volatile Cu compounds at low temperatures [Howard 1991]. Neither can wet etching be used because Cu wet etching is isotropic, making it difficult to yield uniform submicron wiring trenches. Unlike Al, which has a native stable Al_2O_3 layer to passivate the surface, Cu can easily get oxidized and the unstable oxidization layer lacks the passivation function. Cu can also diffuse easily in the dielectrics to degrade the device performance. To overcome these challenges, a new process scheme, the so-called "damascene" process, was introduced for Cu/low-*k* integration. This process is fundamentally different from the subtractive RIE process for Al. These two patterning processes are compared in Figure 1.1(a-b). In the subtractive RIE process, a thin Al film is first deposited then patterned using a photolithographic and RIE process to form the wiring patterns. This is followed by a dielectric deposition step, forming an insulating dielectric in between and on top of the Al wires. Afterwards, a chemical mechanical polishing (CMP) process is applied to planarize the top dielectric layer. Then the whole processing sequence is repeated until the multilayered interconnect structure is completed. By comparison, in the damascene process, a thin layer of dielectric is first deposited and patterned to form wiring trenches by photolithography and RIE process. This is followed by the Cu metallization process to fill in the wiring trench openings. The Cu metallization process starts with a deposition of a very thin Ta-based barrier layer in the trench by physical vapor deposition (PVD). The barrier layer is implemented to prevent Cu from out-diffusion, and it also acts as a base layer for the subsequent process. This is followed by a deposition of a PVD Cu seed layer and then a complete filling of the trench by Cu electroplating. Afterwards, the Cu microstructure in the trench is stabilized by a low-temperature annealing (150~250 ^{o}C). Finally, a CMP process is applied to remove the Cu overburden and the excessive barrier layer on the top surface. A SiN_x or SiC_xN_y layer is then deposited to passivate the wiring structure for one level of the Cu interconnects. The process is repeated until all the required levels are formed to complete the wiring structure.

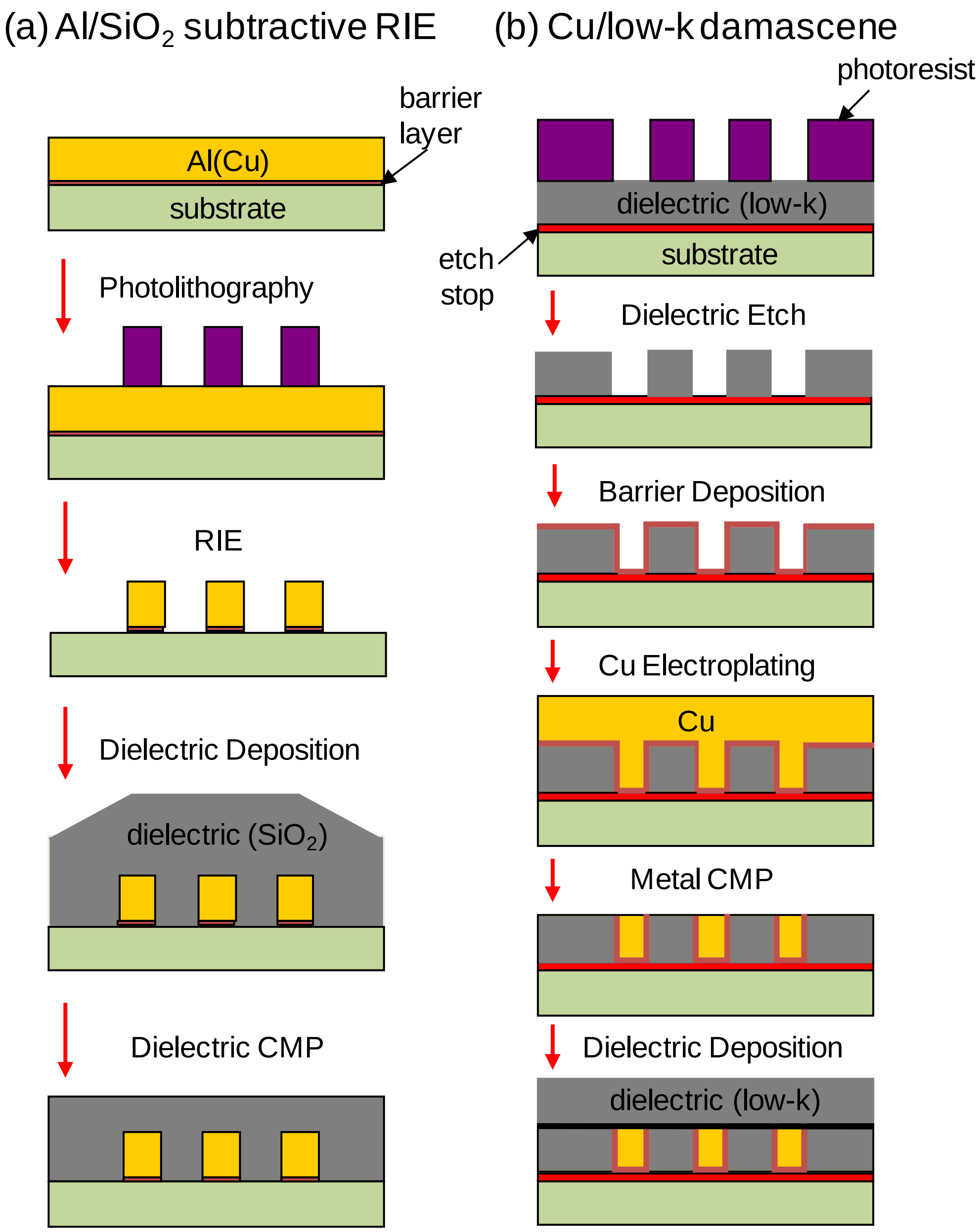


Figure 1.1 Schematic diagrams of (a) conventional RIE process for Al interconnects and (b) damascene process for Cu interconnects.

There are basically two damascene process schemes: single damascene process and dual damascene process. In the single damascene process, the via and trench are patterned in two separate steps, whereas in the dual damascene process, the via and trench are processed simultaneously. In most of the advanced integrated circuits, the dual damascene process is widely used. The advantage of this process is that only one metal filling step is required for both the via and trench structures in each level of the interconnect. This can reduce the via resistance and improve EM reliability in comparison to the single damascene process. The disadvantage of this process is the high aspect ratio of the via and trench structure, making etching, cleaning, and Cu filling processes more difficult. This gives rise to more challenges for material and process integration and cause more reliability issues.

1.2 EM PHENOMENON

The EM phenomenon has been known for over 100 years, with initial observations reported by Geradin in 1861 [Ho 1989]. EM is a diffusion-controlled mass transport process driven by the "electron wind" force, which results from the momentum transfer through the collisions of the metal ions with moving electrons [Huntington 1962]. Under EM, the metal ions diffuse along the metal line, leaving a void at the cathode end or accumulating a "hillock" at the anode end to induce EM failure. During EM, the atomic flux J in the metal line is expressed as:

$$J = nv_d \tag{1.1}$$

where n is the atomic density and v_{d} is the drift velocity of the moving ion driven by the EM force, which is given by:

$$v_{\mathrm{d}} = \mu F = \frac{D_{\mathrm{eff}}}{k_B T} Z^{*} e \rho j \tag{1.2}$$

where μ is the effective mobility of the metal ions, F is the EM driving force, D_{eff} is the effective diffusivity, k_{B} is the Boltzmann constant, T is the absolute temperature, ρ is the metal resistivity, j is the current density and Z^{*} is the effective charge number. This number is usually negative because the "electron wind" force is opposite to the electric field direction. During EM, metal ions can diffuse along various pathways, including the top interface, grain boundary, barrier interface, bulk, and the dislocation cores. Therefore, the effective diffusivity, D_{eff}, is a combination of contributions from each of the above pathways. Accordingly, D_{eff} can be written as:

$$D_{\mathrm{eff}} = \frac{\delta_{\mathrm{N}}}{h} D_{\mathrm{N}} + \frac{\delta_{\mathrm{GB}}}{d}(1 - d/w) D_{\mathrm{GB}} + \delta_{\mathrm{BN}}\left(\frac{2}{w} + \frac{1}{d}\right) + n_{\mathrm{B}} D_{\mathrm{B}} + \rho_{disl} d^2 D_{disl} \tag{1.3}$$

where D is the diffusivity and δ is the effective width for corresponding diffusion pathways. The subscripts N, GB, BN, B and disl refer to the cap interface, grain boundary, barrier interface, bulk and the dislocation cores, respectively. The parameter h is the line thickness, d is the average grain size, w is the line width, ρ_{disl} is the dislocation density, and n_{B} is the fraction of ions diffusing through the bulk of the line. Due to the small dislocation core density, the mass transport through dislocations can be neglected. The relative contributions from these diffusion pathways can be compared based on their activation energies. For Cu interconnects, those activation energies have been measured to be 0.8-1.1 eV for the Cu/SiCN interface [Hu 2002a, Fischer 2002a, Tokogawa 2002], 0.7-0.95 eV for grain boundaries [Surholt 1997, Surholt 1994, Gupta 1988], 1.1-1.8e V for Cu/Ta liner interface [Lin 2002, Demuynck 2004, Hu 2003a, Hu 2004], and ~2.2 eV for the bulk [Rothman 1969]. In comparison, diffusion through the bulk and Ta liner interface is small and can be ignored. Therefore, the dominant diffusion pathways for Cu interconnects are the Cu/SiCN interface and the Cu grain boundaries. Accordingly, the effective diffusivity term can be simplified as:

$$D_{\mathrm{eff}} = \frac{\delta_{\mathrm{N}}}{h} D_{\mathrm{N}} + \frac{\delta_{\mathrm{GB}}}{d} D_{\mathrm{GB}} \tag{1.4}$$

The EM-induced atomic flux itself does not necessarily create voids in the interconnect lines unless there are sites of flux divergence where an unbalanced mass flow rate is present. According to the continuity equation

$$\frac{dC}{dt} = -\nabla J \tag{1.5}$$

where C is the metal atomic density and J is the atomic flux. The divergence of the atomic flux for a given volume is equal to the atomic density change rate within that volume. In Cu interconnects, flux divergence sites are commonly located at the grain boundary triple points, grain boundary/interface triple points, or the geometric discontinuity points. Under the "electron wind" force, voids nucleate at flux divergence sites and then grow larger to cause the EM failure.

1.3 EM CHALLENGES RAISED BY INTERCONNECT SCALING

The interconnect scaling continues aggressively including the continuous reduction in via/line dimension and barrier thickness, and the increase in the current density. Figure 1.2 shows the metal-1(M1) pitch size and the barrier thickness scaling; Figure 1.3 illustrates the required maximum current density $J_{\max}$ scaling for the intermediate level at the operating conditions according to the 2009 International Technology Roadmap for Semiconductors (ITRS) [http://www.itrs.net/]. It is clear that the Cu line width and barrier thickness continue to be scaled down while $J_{\max}$ is scaled up. These trends can raise significant reliability concerns.

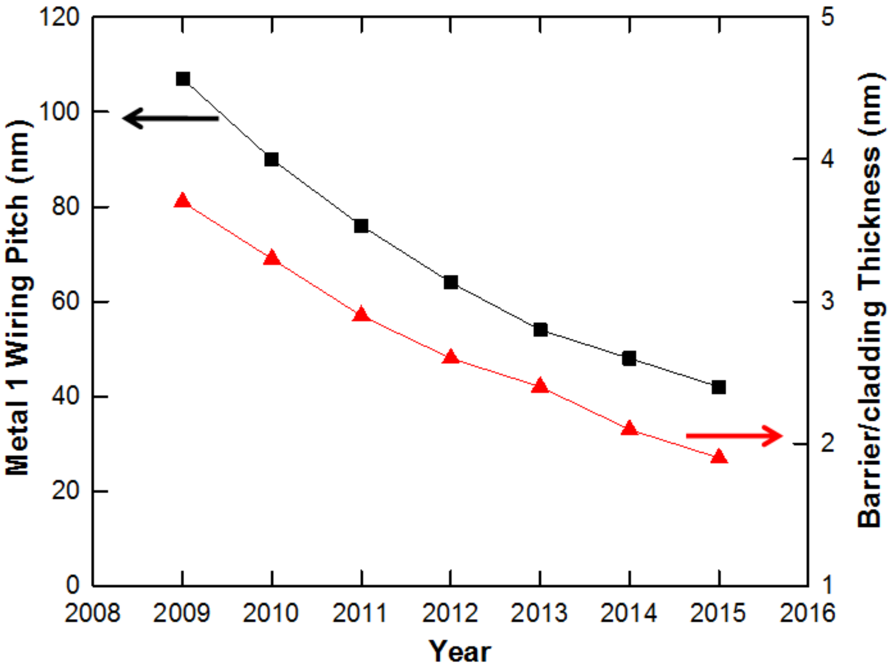


Figure 1.2 Metal-1(M1) pitch size and barrier thickness scaling as depicted by the ITRS, 2009 update [http://www.itrs.net/].

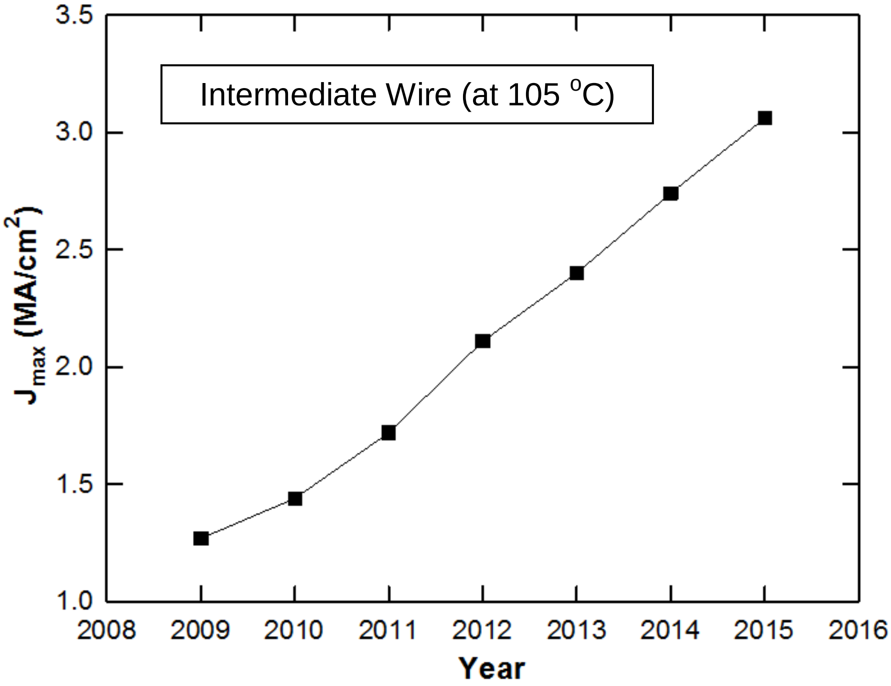


Figure 1.3 The required maximum current density scaling at the intermediate level at operation conditions as depicted by the ITRS, 2009 update [http://www.itrs.net/].

For sub-micron damascene Cu interconnects prior to the 65 nm technology node, the Cu grain structures were commonly observed to be bamboo-like. With most of the grain boundaries aligned perpendicular to the current flow direction, the mass transport through the grain boundaries can be ignored and thus does not contribute to the EM damage formation. Therefore, the atomic diffusion through the Cu/SiCN interface dominates the mass transport and controls EM reliability. Previous studies indicated that the EM lifetime decreased by half for each new technology node, even at the same current density [Hu 2004, Hu 2006]. Hu *et al*. proposed a simple model to predict the lifetime degradation by taking into account the reduction of the critical void size and the line dimension [Hu 2004, Hu 2006] . Figure 1.4 shows the EM lifetime as a function of the cross-sectional area of the line for each technology node depicted in Reference [Hu 2006]. The open circles are the experimental data points and the solid line is the modeling prediction. It shows that the observed EM lifetime degradation is well predicted by the scaling model. Furthermore, given the fact that the current density continues to scale up for each technology node as shown in Figure 1.3, the EM lifetime would be further degraded.

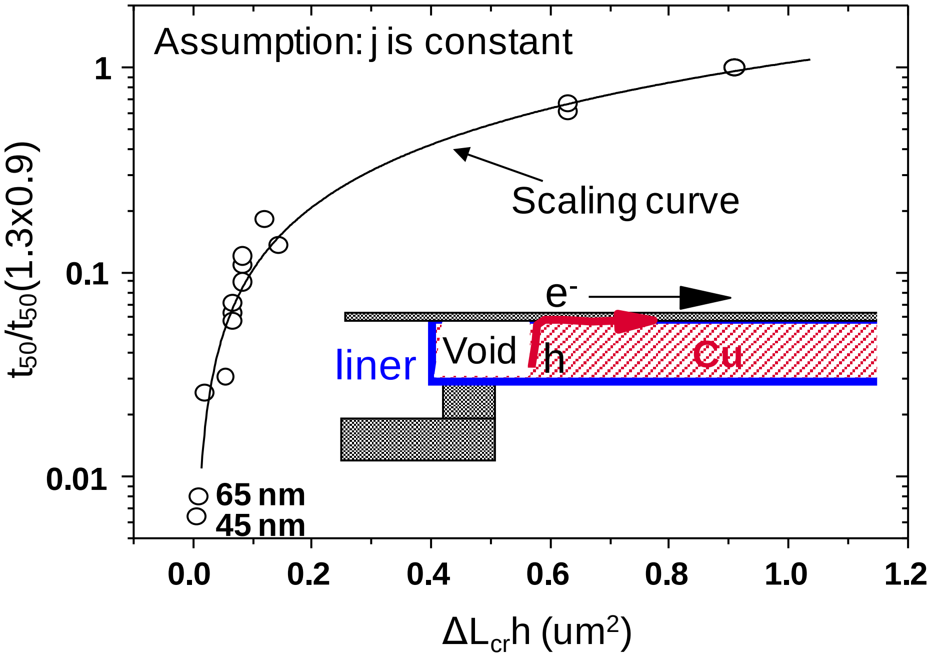


Figure 1.4 Normalized EM lifetime as a function of $\Delta L_{cr}h$ (cross-sectional area wh) for various Cu interconnect generations. [Hu 2006]

At the 65 nm node and beyond when the Cu line width is scaled down to 90 nm or less, a polycrystalline grain structure or a mixture of bamboo and polycrystalline grain structures was reported [Steinhogl 2005, Zhang 2007, Hinode 2001, Hu 2007]. Random line sections of polycrystalline grains were observed, especially at the trench bottom. In such Cu lines, the additional mass transport from the grain boundaries was reported to further degrade the EM performance [Hu 2007]. As scaling continues, the aspect ratio and the surface to volume ratio of the Cu via and trench continue to increase, making it increasingly difficult to completely fill the Cu trench and to retain the bamboo-like grain structures. Therefore more small grains are expected to be present in the Cu interconnects for future technology nodes. Consequently, it becomes more important to investigate and understand the scaling impact of grain structures on EM reliability of Cu interconnects.

1.4 REVIEW OF RECENT EM STUDIES

1.4.1 Cap Layer Effects on EM

To improve the EM performance, significant research efforts have been put in developing new materials and structures to suppress the atomic diffusion along the top cap interface for improving the EM performance. These methods include inserting a metal cap layer, alloying the top Cu surface using Al, or siliciding the top Cu surface prior to the SiCN passivation layer deposition. The most effective method is to apply a metal cap, e.g. CoWP, CuSnP, Pd, Ta, Ru, on top of the Cu line [Hu 2002b, Hu 2004, Hu 2003a, Hu 2003b, Gambino 2006, Aubel 2008, Meyer 2007, Zschech 2005a]. Remarkable improvement in the EM lifetime up to two orders of magnitude was reported. In addition, the activation energies increased from ~1.0 eV for the SiCN cap to ~ 1.4 eV for the Ta-based cap and to ~2.0 eV for the CoWP cap [Hu 2004]. As the EM lifetime improved, the standard deviation σ of the EM lifetime distribution for the CoWP capped structures was reported to increase as well, up to ~ 1.3 compared with the much smaller sigma of ~0.3 for the SiCN-capped Cu lines [Gall 2006]. While the improvement in the

EM lifetime for the CoWP cap has been attributed to the increased interface bond strength and suppressed interface diffusion, the root cause of the large σ is not as well understood.

The effect of cap layer and grain structure on EM damage formation was further investigated by Zschech *et al.* using in-situ EM experiments to observe the void formation and evolution for SiN_x capped and CoWP capped Cu interconnects [Zschech 2005b, Zschech 2009, Meyer 2002, Meyer 2007, Vairagar 2004]. The rate of void nucleation and evolution was found to be significantly slower for test structures with the CoWP cap than those with the SiN_x cap. In test structures with the SiCN cap, voids were mostly nucleated at the top interface where the interface and grain boundary intersects. However, for test structures with the CoWP cap, in addition to the top interface, voids were also observed at the bottom Ta barrier interface. This suggests that the top interface was suppressed to the extent that the contributions from grain boundaries and the Cu/liner interfaces can no longer be neglected. The Cu microstructure and the grain boundary morphology seem to play a more important role in EM damage formation for the CoWP cap.

1.4.2 Microstructure Effects on EM

The effect of metal microstructure on EM behaviors has long been investigated. Most of the research was focused on Al interconnects. For Al interconnects with polycrystalline grain structures, the grain boundary diffusion was found to be the dominant diffusion path and the grain boundary triple points provided the flux divergence sites leading to EM failure. It was also observed that large grain size and strong (111) texture in Al interconnects resulted in a longer lifetime with a tighter standard deviation due to the reduction in flux divergence sites and fast diffusion paths [Attardo 1970, Ryu 1998].

However, the microstructure effect on EM reliability of Cu interconnects has been less studied. The dominant diffusion path in Cu interconnects was found to be mainly at the weak Cu/cap interface resulting from the CMP damage and contamination. Therefore, the impact of microstructure on EM was less influential. Hau-Riege *et al.* [Hau-Riege 2001] reported that for a very weak Cu/cap interface, Cu microstructure did not affect the EM performance significantly. Thus, Cu lines with bamboo-like and polycrystalline structures showed a similar EM lifetime distribution. However, when the Cu/cap interface was improved by process optimization, the effect of Cu microstructure on the EM lifetime was pronounced [Hu 2007]. Cu interconnects with bamboo grains were found to possess a longer EM lifetime than those with the polycrystalline grains. This raises an interesting question regarding the microstructure effect on EM performance when the Cu cap interface is further improved by a metal cap.

1.5 SCOPE OF THIS WORK

The objective of this work is to investigate the impact of scaling and microstructure on EM lifetime, statistics, and damage formation in Cu/low-*k* interconnects. Specifically, the effects of geometrical scaling, scaling-induced microstructure changes, new capping materials, and grain structures are to be examined.

This dissertation is arranged as follows:

First, details of the experimental procedures including the experimental setup, EM test structures, data analysis approaches, and failure analysis methodologies are described in Chapter 2.

Chapter 3 focuses on the geometrical scaling effect on EM performance and Cu grain structures. Via scaling effects on EM lifetime distribution are first examined by performing upstream EM tests on two types of test structures. Type I structures have the same via size and M2 line width, with sizes of 90 nm, 125 nm, and 175 nm. Type II structures have a fixed via size and a varied M2 line width. The impact of via scaling can be demonstrated by comparing the EM results of these two types of test structures. Then, the line scaling effect on Cu microstructures is investigated. Both plane-view and cross-sectional view transmission electron microscopy (TEM) techniques are applied to study the Cu grain structures. Specifically, the grain size distributions obtained from the plane-view TEM observations for different line widths are compared to illustrate the line scaling effect on Cu microstructure. The TEM observation is supplemented by a grain growth simulation based on the Monte Carlo method to study the line scaling effect on the Cu grain structure.

The cap layer and grain structure effects are investigated in Chapters 4 and 5. Chapter 4 focuses on the experimental results and Chapter 5 focuses on the EM simulation results.

In Chapter 4, four sets of Cu lines are fabricated at the M2 level by changing the capping materials and Cu grain structures: large/small grains with CoWP/SiCN caps. These test structures are fabricated using the 45 nm technology node process. Longitudinal TEM and high resolution TEM are applied to characterize the grain structure of the test line and examine the Cu/cap interface. Downstream EM tests are carried out on these structures. To better understand the EM results, the effect of failure criteria on EM lifetime distribution and failure mechanism is reviewed. This is followed with a discussion on the correlation between resistance traces and void formation/evolution processes. By comparing the EM data of the four sets of test structures, the effects of cap layer and grain structure on EM lifetime and statistics are determined. Their effects on failure modes are examined by failure analysis using TEM and focused ion beam (FIB) techniques. This chapter is concluded with an analysis of the cap layer and grain structure effects on EM lifetime scaling for future technology nodes.

In Chapter 5, a statistical model is developed to investigate the effect of grain structure on EM lifetime and statistics for Cu interconnects with the CoWP cap. The model is essentially an extension of the microstructure-based model formulated by Korhonen et al. [Korhonen 1993a] to study the microstructure effect on EM lifetime and statistics of Al interconnects. In this model, the microstructure of the Cu interconnects is simplified as cluster grains and bamboo grains connected in series and statistically distributed in the line. The actual grain structures are examined by TEM to obtain the cluster segment length distributions. Under EM, the stress evolution and void formation can be calculated in the cluster grain and bamboo grain section for each individual structural unit (failure unit). This establishes a direct correlation between the EM lifetime and the cluster length in an individual failure unit. Then the weakest-link model is applied to simulate the EM lifetime and statistics based on the measured cluster length distribution in Cu interconnects and the simulation results are compared with the measured EM data. At the end of this chapter, the general trend due to the effect of bamboo and cluster segment diffusivity on the EM lifetime is discussed.

Finally, a summary of this work and proposed future studies are presented in Chapter 6.

Chapter 2: Electromigration Experimental Details

2.1 EM TEST SYSTEM CONFIGURATION

The EM tests were performed in a high vacuum chamber test system as shown in Figure 2.1. During the EM test, the chamber was back filled with pure N_2 up to 20 Torr to improve the temperature uniformity of test samples. The chamber is equipped with two sets of heating coils, with each set having a separate temperature controller. The primarily heating coils are located at the top and bottom plates to control the test temperature and the second heating coils are mounted at the chamber sidewall to reduce the temperature gradient from the center to the edge. The constant-current source power supply can support output up to 80 V and 10 mA. A Keithley 7002 switch system is employed to switch between the test structures. A Keithley 196 digital multimeter (DMM) is used to measure the voltage drop across each test structure. The data acquisition is controlled by a computer equipped with a LabVIEW program developed in our laboratory.

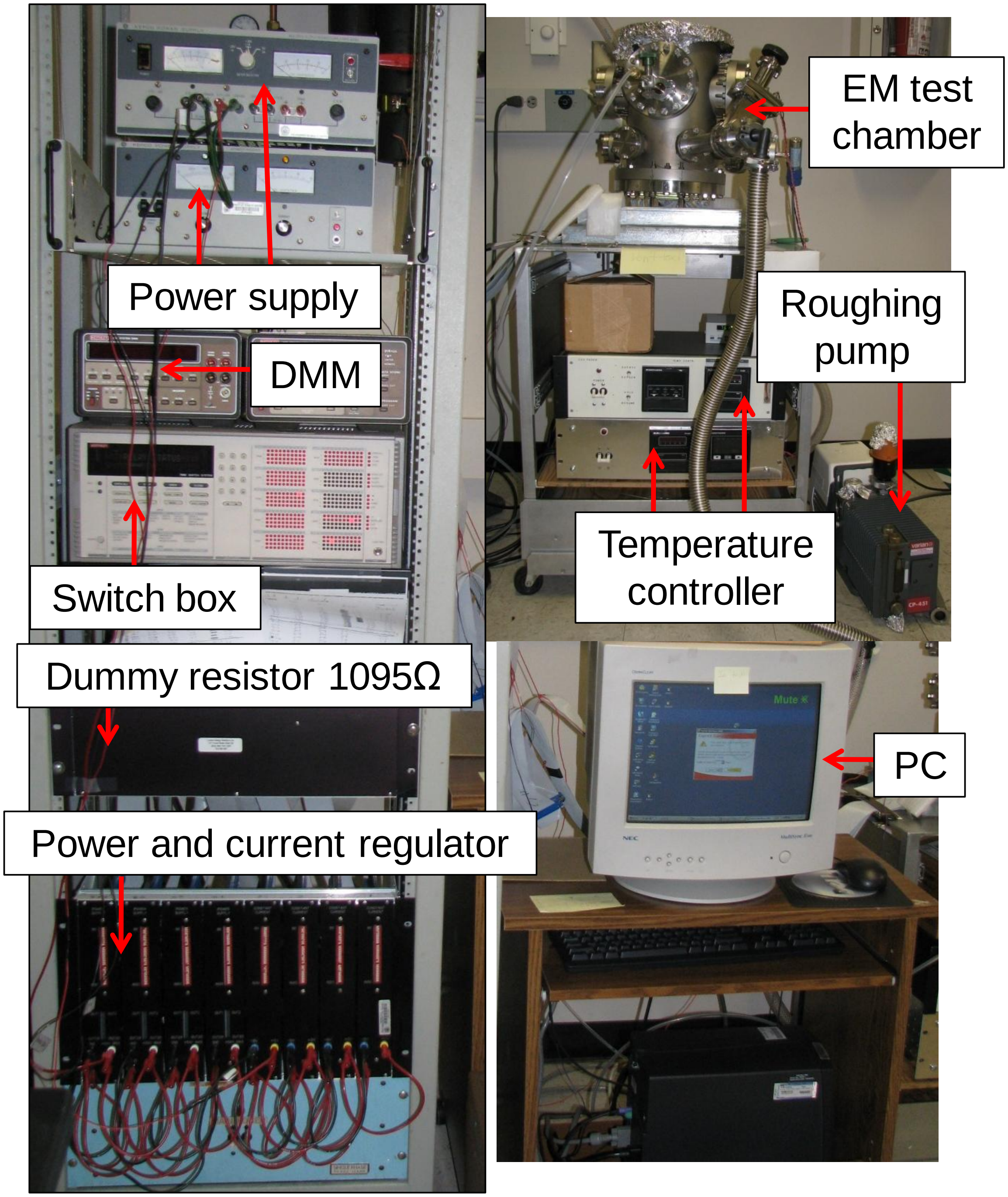


Figure 2.1 Package-level EM test system.

2.2 EM EXPERIMENTAL PROCEDURE

Some of the test structures used for this study were designed by UT-Austin and fabricated by Sematech, which came in as whole 300 mm wafers. Other structures were designed and fabricated by GLOBALFOUNDRIES at Dresden Germany, which arrived as individually packaged samples and ready for EM test immediately.

The following describes the sample preparation for samples from Sematech and the basic test sequence for both Sematech and GLOBALFOUNDRIES samples.

Sample Preparation:

1. International Sematech provided the 300 mm wafers containing the designed EM test structures.
2. The wafers were diced into small pieces with the test module of interest in the die by using a Kulicke&Soffa Model 982-10 dicing saw or an ADT Model 7100 dicing saw.
3. Two test dies were mounted to a 16-pin ceramic dual-in-line package (DIP) using QMI 3555 Low Temp Ag/Glass die attach paste. The packages were then cured in a vacuum oven at 350 ^{o}C for 40 minutes for die attach.
4. Electrical connectivity between the package and the test die was made through a Kulicke&Soffa Model 4123 Wedge Bonder or a West Bond Model 7400A Ultrasonic Wire Bonder. The pin to pin resistance of each package was measured and recorded to make sure that proper wire bonding had been performed. The test packages were then ready to be assembled into the test chamber.

Test Sequence:

5. The current of each test channel in the test chamber was set at the pre-set value according to the experimental test design.
6. All test packages were assembled into the vacuum chamber with proper electrical contact between the DIP pin and the socket. The room-temperature resistances of all test samples were measured and recorded to ensure a proper electrical contact.
7. The chamber was evacuated to less than 10 mTorr using a mechanical pump and the chamber temperature slowly was ramped up to target temperature at the ramping rate of 2 ^{o}C/min.
8. The chamber was backfilled with N_2 to 20 Torr to increase the thermal conductivity in the chamber and to improve the temperature uniformity. After the target temperature was reached and stabilized, the current flowing in the test structure was gradually increased to the target value.
9. The resistance of the test structure was recorded continuously during the EM test and the EM lifetime was determined after a certain proportion of resistance increase was reached. The EM test was usually terminated upon the failure of all test structures.
10. Selected failure structures with distinct resistance traces or failure times were analyzed using the FEI dual beam focused ion beam/scanning electron microscopy (FIB/SEM). Due to the small dimension of the test structures, some samples were inspected by using transmission electron microscope (TEM). Either a JEOL 2010F TEM or an FEI TECNAI G2 F20 TEM was used in this study. The failure analysis can correlate the physical EM damage

formation with the resistance increase and the EM lifetime of the Cu interconnects.

2.3 EM TEST STRUCTURE DESCRIPTION

For each test die, there are five terminals for the current flow and voltage measurements: V^+, V^-, I^+, I^-, and V^{ext}. Figure 2.2 shows a schematic view of one test package with two dies attached. The constant current flows in and out of the test die through I^+ and I^- pins. The voltage drop across the test structure is measured through V^+ and V^- pins to deduce its resistance change. Meanwhile, the voltage change across V^{ext} and V^- pins is monitored to detect the EM failure due to anode extrusion. In this study, all the EM structures failed due to the void formation at the cathode end of the line.

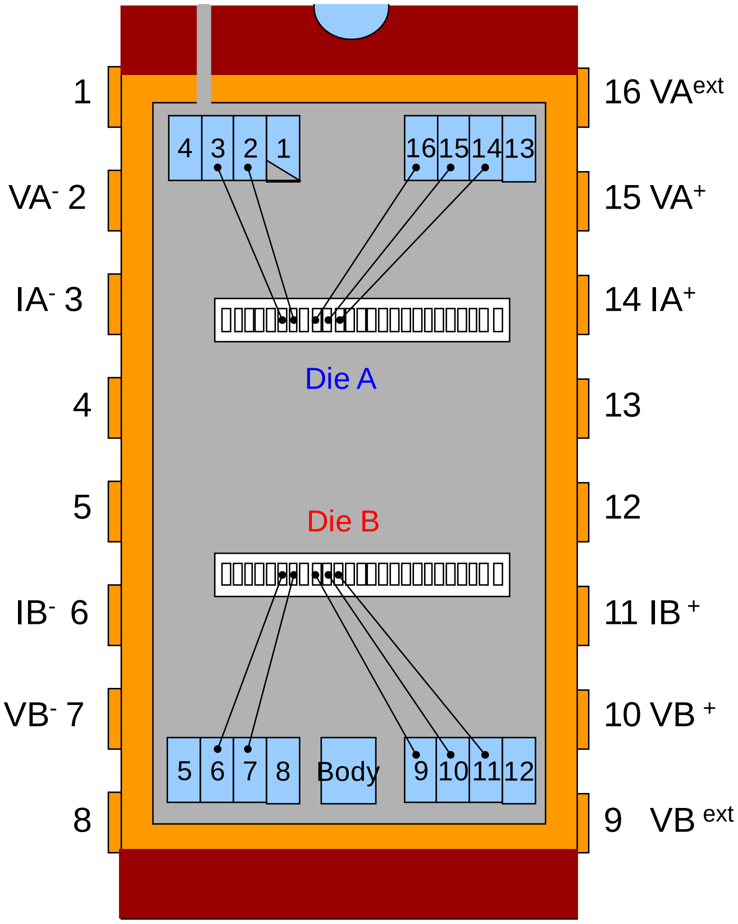


Figure 2.2 Schematic diagram of 16 pin DIP package with two test dies attached.

The EM test structures used in this study were single-linked structures. Depending on the current flow direction, two test schemes were performed. Figure 2.3 shows the schematic diagram of the two types of test structures. In the upstream structure, the metal-2 (M2) line is the test line which is designed long and narrow; the metal-1 (M1) line is the feeder line which is designed short and wide so that the EM failure only occurs in the M2 test line. Under this circumstance, the EM failure usually occurs either within the via or at the cathode end of the M2 line close to the via. The downstream EM structure is identical to the upstream structure except that the M1 line is test line, which is long and narrow. In this case, the EM failure typically occurs at the cathode end of the M1 line.

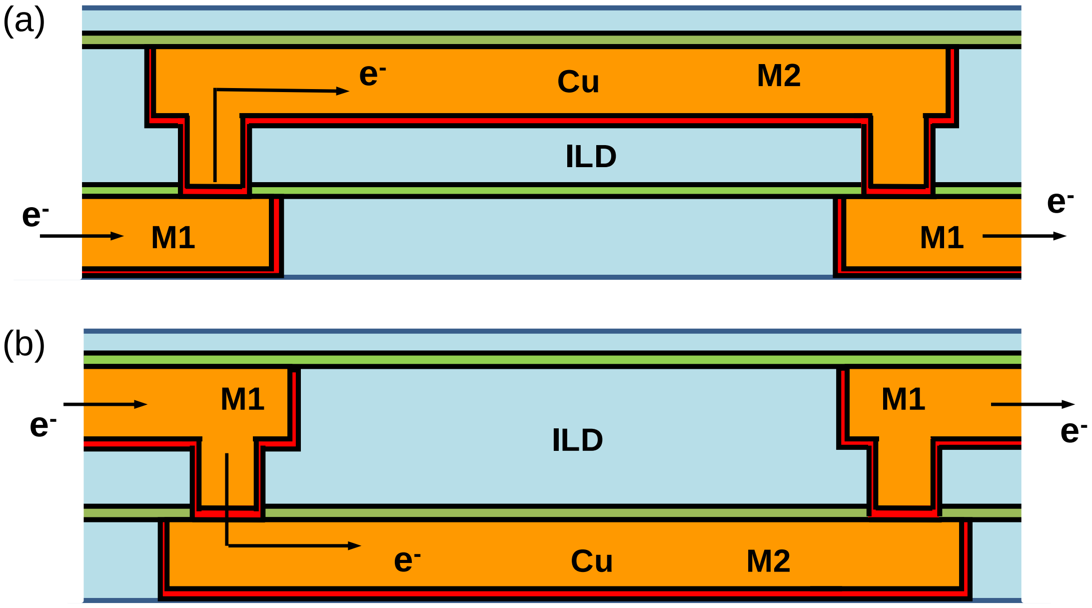


Figure 2.3 Schematics of the two types of EM test structures: (a) upstream and (b) downstream.

2.4 RESISTANCE TRACE

The resistance change of the test structure was monitored during the EM test to help determine the EM lifetime and the failure mechanism. Two typical resistance changes are observed as illustrated in Figures 2.4(a-b). An abrupt resistance increase followed by a gradual resistance increase, as shown in Figure 2.4(a), is a typical resistance change with void formation at the cathode end of the line with the presence of a redundant Ta barrier. Such an abrupt resistance increase occurs then Cu of the whole cross section of the line is depleted, forcing the current to flow through the highly resistive Ta barrier. Then the void grows further causing a gradual resistance increase. The EM lifetime (t) was determined at the time when either the abrupt resistance increase occurs or a fixed proportion of resistance increase is reached, e.g. 10% resistance increase in most cases in this study.

The second type of resistance change is the abrupt resistance increase to infinity as shown in Figure 2.4(b). Such an abrupt resistance change usually indicates a premature extrinsic failure caused by process-induced defects. It could occur when a slit-like void forms underneath the via bottom for the downstream test, or when a void forms inside the via for the upstream test. It could also be caused by a process-induced defect in the line or an ultrathin Ta barrier which burns instantly when a void fully occupies the cross-section of the Cu line. The real voiding mechanism can be identified with the assistance of physical failure analysis using FIB or TEM. The EM lifetime in this case is determined at the onset of the abrupt resistance increase.

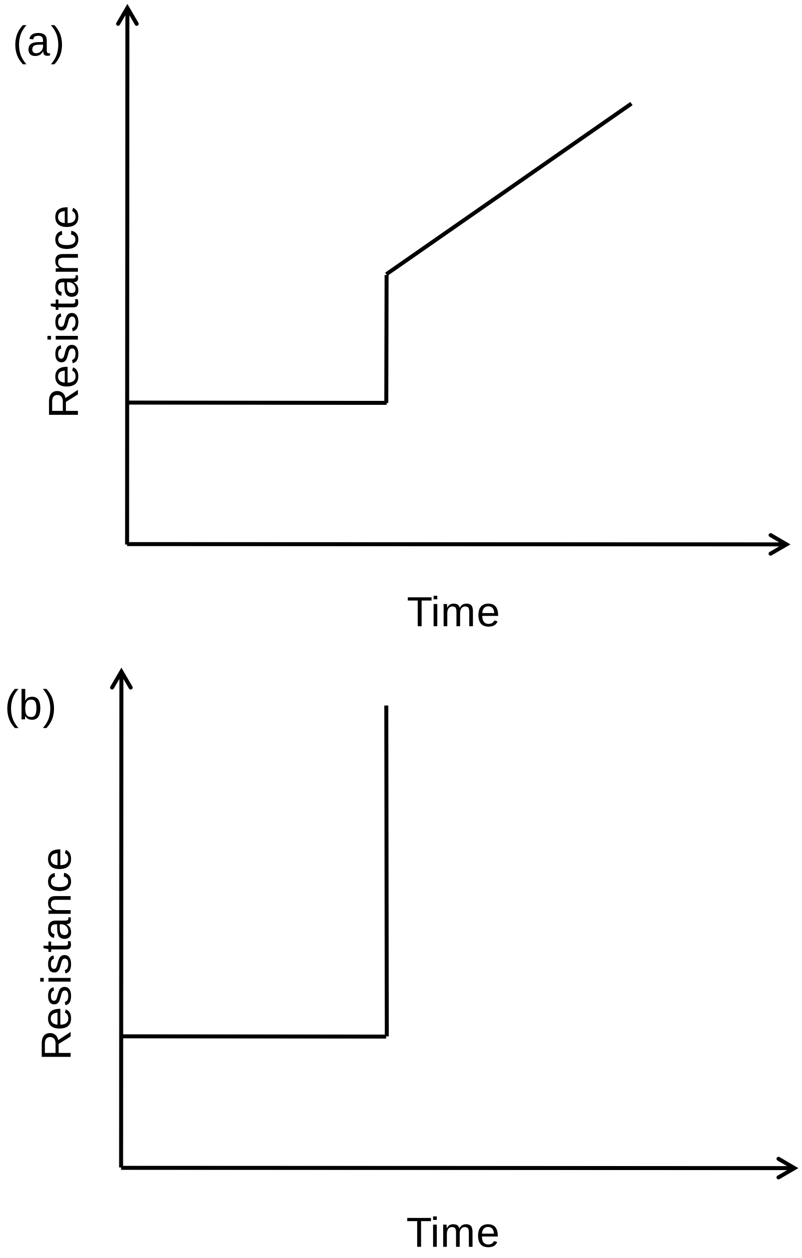


Figure 2.4 Two typical resistance traces as a function of time: (a) abrupt resistance increase followed by a gradual resistance increase and (b) abrupt resistance increase.

2.5 FAILURE ANALYSIS

After the EM test, failure analysis was conducted on selected samples using FIB cross sectioning and SEM or TEM imaging. A FEI dual beam FIB/SEM system was used in this study. This system is equipped with a thermal emission tip for high resolution SEM imaging and a FIB with the Ga ion source for cutting with an angle of 52° in between, as shown in Figure 2.5. The major advantage of this system is the simultaneous imaging and cutting of the test structure, enabling us to stop at the desired position. Figure 2.6 displays a typical SEM image after the FIB cut showing a void formation in the M2 trench close to the cathode end of the line.

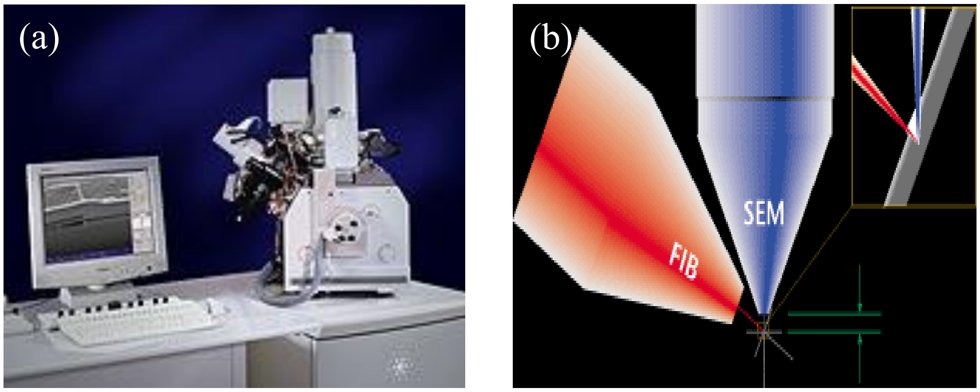


Figure 2.5 (a) The FEI Strata™ DB235 dual beam FIB/SEM system and (b) the schematic illustration of the configuration of the two beams (52° in between).

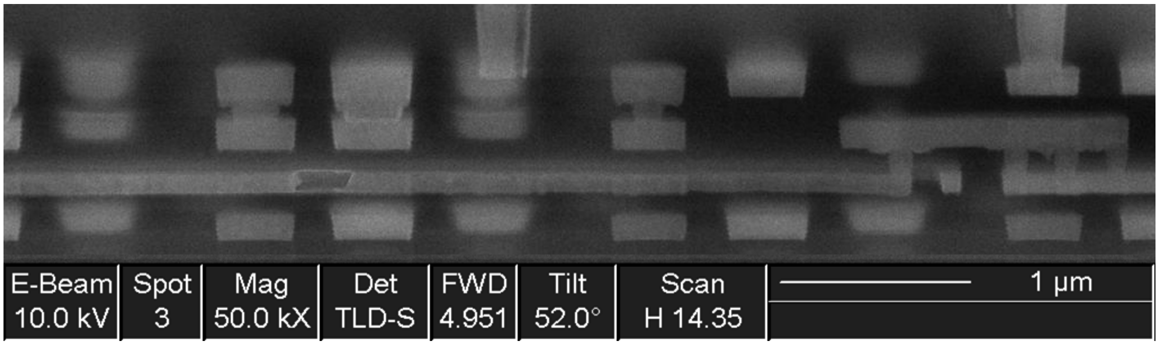


Figure 2.6 A typical SEM image showing a void formation in the M2 trench several microns away from the cathode via.

Cross-sectional TEM was also employed for the failure analysis. Details of the cross-sectional TEM sample preparation will be discussed in Chapter 3.

Chapter 3: The Scaling Effect on Electromigration Reliability and Grain Structure of Cu Interconnects

3.1 INTRODUCTION

As stated in Chapter 1, the scaling has caused serious reliability concerns in modern Cu interconnects. In this chapter, the scaling effects will be further studied. The first part covers the via scaling effect on EM reliability of Cu interconnects, and the second part covers the line scaling effect on grain structures of Cu interconnects.

Vias in interconnects connect the lower metal line to the upper metal line to achieve the complex logic functions and play a key role in influencing the lifetime of stress induced voiding (SIB) and EM. As illustrated in Chapter 1, Cu interconnects in modern integrated circuits (ICs) are fabricated using the dual damascene process where the via and trench in each level are patterned simultaneously. The high-aspect-ratio via, which comes with the dual damascene processing, has been recognized as the most complicated location for process integration. Different from the robust W via in Al interconnects, the Cu via in Cu interconnects is vulnerable to process-induced defects and is reported to be the weakest link for reliability. Any defect at the via bottom can pose a reliability weak point and limit the overall EM performance of ICs. In upstream EM tests, it is common to observe a bimodal EM lifetime distribution, in which the early failure mode (weak mode) is caused by a void formation inside the via or at the via bottom [Gill 2002, Fischer 2002b, Li 2004, Lee 2006a, Oates 2006, Lee 2006b]. This failure mode is directly related to the via bottom processing, such as via etching, cleaning and barrier layer deposition. Similarly, a slit-like void was also reported to form directly under the via bottom, resulting in an order of magnitude reduction in EM lifetime [Li 2004, Oates 2006, Lee 2006b].

As the device scaling continues, the via shrinks in every dimension including the Cu via cross-sectional area and the surrounding barrier layer thickness. Processing difficulty in achieving thin and conformal barrier formation in via can result in more reliability issues arising from the barrier adhesion, integrity, and uniformity. Whereas the extrinsic failures in via reliability have been studied extensively, the intrinsic failure of via is not well understood. In this chapter, the impact of geometrical via scaling on EM reliability for Cu interconnects is investigated. Two types of upstream EM structures are tested and their EM behaviors are compared to emphasize the effect of via scaling. In addition, EM tests are conducted at higher current densities in order to extract an important parameter related the intrinsic via reliability: the maximum current density that a single via can support.

The second part of this chapter is to investigate the impact of line scaling on microstructure of damascene Cu interconnects. The microstructure of Cu interconnects is important because the grain size and texture not only affects the Cu line resistivity, but also impacts the mechanical stress and the resistance to EM damage. So far, extensive data have been published [Lee 1996, Gangulee 1972, Lingk 1999, Besser 2001] on the microstructure of damascene Cu lines regarding the grain texture and size distribution and their variations with different line widths. However, only few results have been reported recently [Steinhogl 2005, Khoo 2007a, Khoo 2006, Khoo 2007b, Khoo 2007c] on the microstructures of Cu lines narrower than 100 nm. For ultra-narrow Cu lines less than 100 nm wide, the resistivity was found to increase as the line width scales down. This effect was attributed to the increase in electron scattering caused by the surface, the interface, and the grain boundary when the line width approaches the electron mean free path in Cu (45 nm at room temperature). For ultra-narrow Cu lines, there is a serious reliability concern arising from insufficient grain growth [Khoo 2007c]. This can increase the grain boundaries for additional fast mass transport and thus lead to a degradation of EM reliability, which was indeed observed recently for Cu lines at 90 nm line width [Hu 2007]. Therefore, it is important to study how Cu grain structures will evolve as line scaling continues, particularly for sub-100 nm Cu lines. The line scaling effect on the grain structure of Cu lines will be investigated further using TEM. The study is performed on Cu damascene lines of 60 nm line width fabricated by using a trench filling technique, together with Cu lines with the width of 185 nm and 850 nm. Microstructures of Cu lines will be examined by using both plan-view and cross-sectional TEM techniques. Furthermore, a Monte Carlo method based on the modified Potts model will be applied to simulate the grain growth in damascene Cu interconnects.

3.2 VIA SCALING EFFECT ON EM RELIABILITY OF CU INTERCONNECTS

3.2.1 Experimental Details

Two metal layer test structures were fabricated at SEMATECH using a standard damascene process at 65 nm technology node. A Chemical Vapor Deposition (CVD) based porous organosilicate material with the effective permittivity *k* of 2.3 was used as the interlayer dielectrics. The Cu damascene interconnects were encapsulated with Ta-based barrier at the sidewalls and trench bottom, and capped with a SiN_x cap layer on the top interface. Two types of single-linked upstream EM test structures were designed for the via scaling study, as shown in Figure 3.1. In the type I structure, the M2 line widths varied from 90, 125, to 175 nm. The via width and the end reservoir length were scaled to be the same as the M2 line width. In the type II structure, while the M2 line width increased from 90 nm to 175 nm, the via width remained constant at 90 nm. All the test lines at the M2 level had the same line thicknesses of 135 nm and line length of 150 μm. The cross sections of the vias were of square shape.

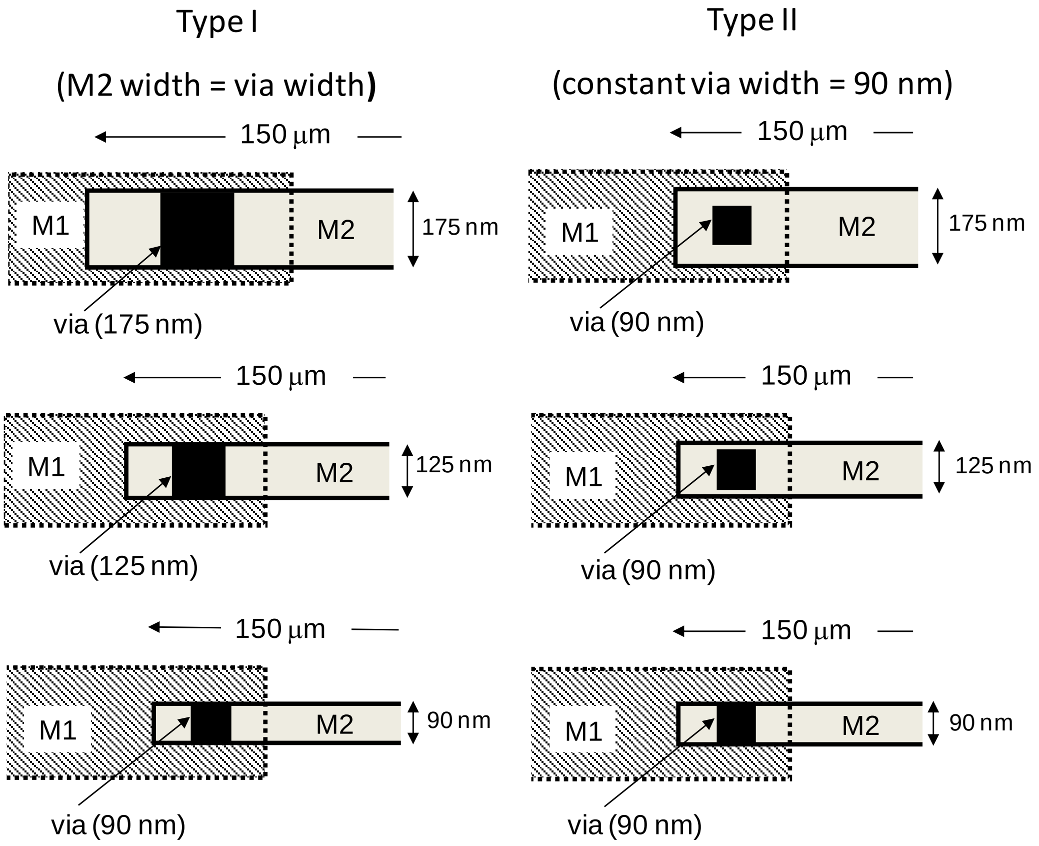


Figure 3.1 Schematics of two level (M1/via/M2) interconnect. The stressed line (M2 line) was long (150 μm) and narrow, while the connecting line (M1 line) was short and wide to minimize the EM damage.

Upstream EM experiments were performed at 330 °C with the current density in the M2 lines constant at 1.0, 2.0 or 4.0 MA/cm^2. The tests were performed in a high vacuum chamber with back filled pure nitrogen at 20 torr. The resistance change was recorded during EM tests, and the first resistance increase of 10% was set as the failure criterion. Failure analysis was performed using dual-beam FIB/SEM to examine the EM-induced void formation.

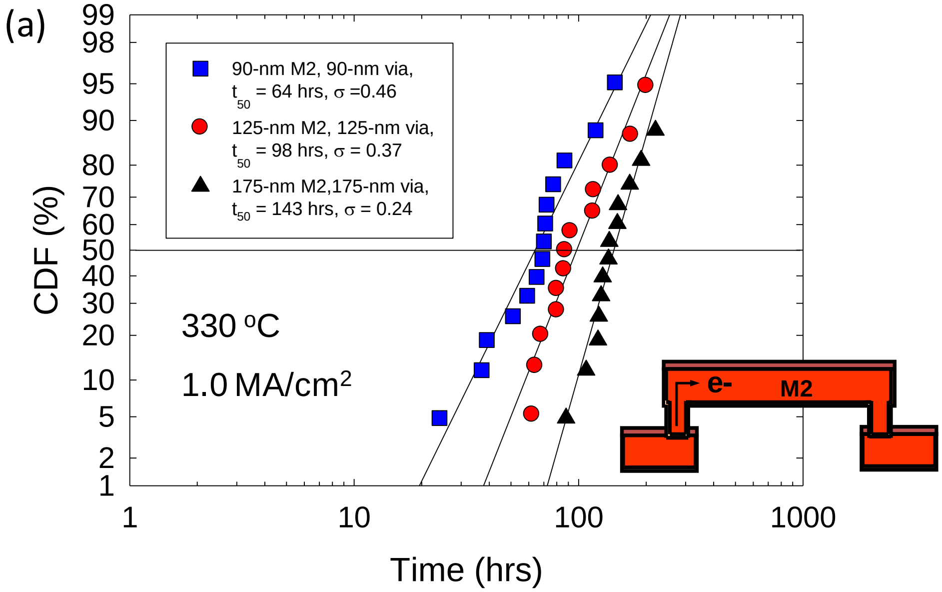
3.2.2 EM Lifetime Distribution for Type I and Type II Structures at $j = 1.0$ MA/cm^2

Figure 3.2 shows the cumulative distribution function (CDF) plots for both type I and type II structures tested at 330 ^{o}C with the current density of 1.0 MA/cm^2. For the type I structure where the via size scaled with the M2 line width, the EM lifetime was found to decease in proportional to the M2 line width and the via size, as shown in Figure 3.2(a). However, for the type II structure with fixed via size and varied M2 line width, the EM lifetime and statistics were found to be similar regardless of M2 line widths, as shown in Figure 3.2(b). The difference in the EM behavior for the two types of structures can be explained based on the following EM lifetime model proposed by Hu *et al*. [Hu 2004]:

$$\tau = \Delta L_{cr}/v_d = \Delta L_{cr} h k_B T/(\delta_i D_i F_i) \qquad (3.1)$$

where ΔL_{cr} is the critical void length required for the line failure, v_d is the net drift velocity, h is the line thickness, k_B is Boltzmann constant, T is the absolute temperature, and δ_i is the effective thickness of the interface region, D_i is the interface diffusivity, and $F_i = eZ^*\rho j/\Omega$ is the EM driving force.

This model assumes an intrinsic failure mechanism where mass transport is dominated by the diffusion at the Cu/cap interface with a diffusivity D_i. In this study, all the line structures have the identical SiN$_x$ cap layer process and line thickness h, and are tested under the same temperature and current density. Therefore, the EM lifetime is expected to be directly correlated to ΔL_{cr}. For the upstream EM test, the Cu line fails due to void growth starting from the cathode end of the trench to cover the whole via. Therefore, ΔL_{cr} and thus the EM lifetime should be in direct proportion to the via size. For the type I structure, the via size was scaled with the M2 line width, thus the EM lifetime decreased as the via size and the M2 line width deceased from 175 nm to 90 nm, as shown in Figure 3.2(a). However, for the type II structure, the via size was fixed at 90 nm while the M2 line width varied. The critical void size ΔL_{cr} for the three different line widths was the same, leading to a similar lifetime and EM statistics, independent of the line width. This confirms the experimental results as illustrated in Figure 3.2(b).



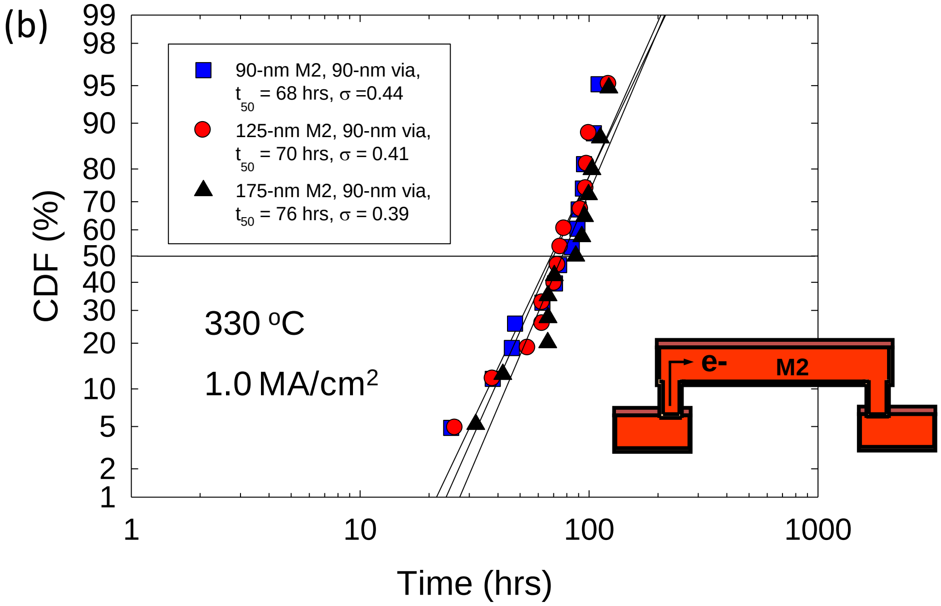


Figure 3.2 Cumulative distribution function (CDF) plots of type I (a), and type II (b) structures for upstream electron flow. EM tests were performed at T = 330 °C, with a current density of j = 1.0 MA/cm^2.

In terms of the EM statistics, the type I structure shows a scaling of the statistical variation. The 90 nm Cu lines demonstrated a larger lifetime variation with σ of 0.46 compared to the 125 nm (σ = 0.37) and 175 nm (σ = 0.24) structures. In comparison, the type II structure shows a similar lifetime variation for Cu lines with different line widths and identical via sizes. The combination of EM lifetime and statistics analysis indicates that the EM performance is directly controlled by the via size. The geometrical scaling of the via size triggers a corresponding scaling in the EM lifetime.

3.2.3 Failure Analysis

The resistance traces were analyzed for the type I structure to determine the root cause of the statistics scaling. Figure 3.3 plots the resistance traces of the 125 nm and 90 nm Cu lines for the type I structure. For the 125 nm Cu lines, all test samples showed a progressive resistance change, a typical intrinsic EM failure behavior where the first abrupt resistance increase occurred when a void which grew from the cathode end completely empty up the space above the whole via. The current was then shunted to the redundant Ta barrier, causing resistance to jump up [Hu 2003a]. The subsequent gradual increase in resistance was due to the continuous void growth in the M2 trench. When the Ta barrier could no longer sustain the current density, the barrier burned out, causing an abrupt resistance increase and an open failure.

However, the resistance traces for the 90 nm Cu lines showed both progressive and abrupt resistance behaviors, as shown in Figure 3.3(b). This bimodality in upstream EM failure has been reported before [Li 2004, Oates 2006, Gill 2002]. The abrupt resistance increase is attributed to the void formation at the via bottom. This extrinsic failure mode is directly correlated to the via bottom process and is strongly process-dependent. The abrupt resistance increase could also be caused by the unstable Ta barrier layer [Hu 2006]. Without a uniform and stable redundant Ta barrier carrying the electrical current after the void forms in the trench, the resistance of the EM test line can instantly reach infinity once a void fully occupies the line cross section. This failure mode reduces the EM lifetime significantly and introduces bimodality in the EM lifetime distribution. The combination of two different failure modes accounts for the larger lifetime variation for the 90 nm Cu lines in the type I structure.

Additionally, due to the scaling of the critical void size ΔL_{cr} for the type I structure, a smaller void is required to form for the failure of the 90 nm lines compared to the 125 and 175 nm lines. Given the assumption that all other parameters are identical, the same amount of variation in the void shape and size can induce a larger standard variation in the 90 nm lines than in the 175 nm lines. This also accounts for the larger lifetime variations for the 90 nm Cu lines.

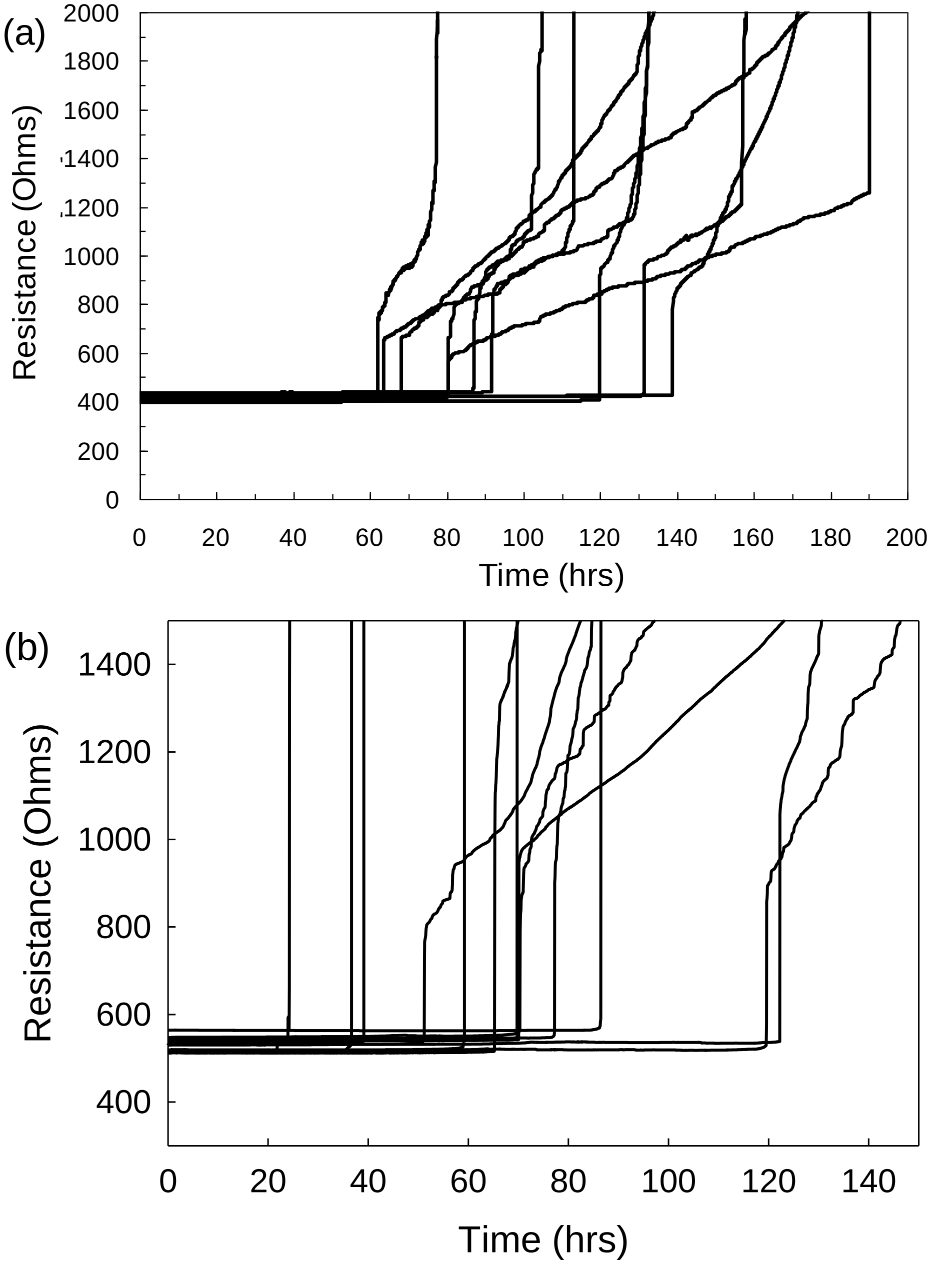


Figure 3.3 (a) Resistance traces of the type I structures: (a) 125 nm wide M2 and via, (b) 90 nm wide M2 and via.

To further identify the failure mechanism, physical failure analysis was performed on the EM failed samples. Figure 3.4 shows the FIB image of one failed 125 nm Cu line for the type I structure. Even though the via structure above the M2 trench was not clearly identified due to the severe joule heating induced damage, a large trench void at the cathode end was evident. This damage mode supports the intrinsic failure mechanism due to void formation at the cathode end driven by the Cu/cap interfacial mass transport. However, for the extrinsic failure in 90 nm lines with an abrupt resistance increase, EM damage occurred in the trench close to the cathode via with severe joule heating damage, as shown in Figure 3.5. It is suspected that this failure mode is due to the non-uniformity of the Ta barrier layer. Once a void is formed in the Cu line, the thin and unstable Ta barrier cannot support the high current density and burns out immediately, yielding an instant open failure and an abrupt resistance jump.

Figure 3.4 SEM image showing a large cathode void in the M2 trench for an EM failed sample with 125 nm via and M2, type I structure.

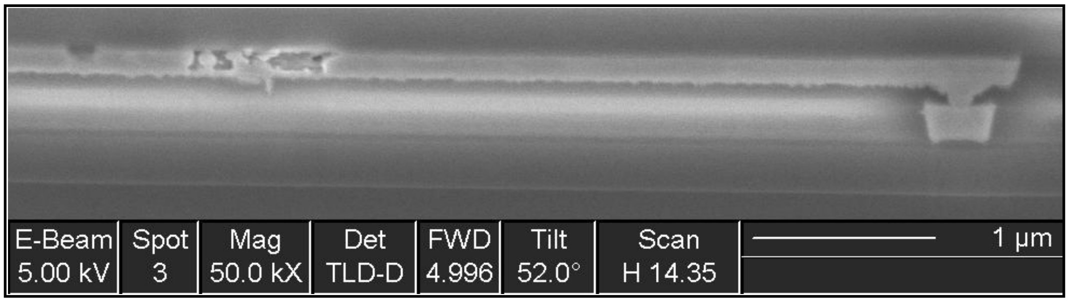


Figure 3.5 SEM image showing multiple void formation in the M2 trench for an EM failed sample with 90 nm via and M2, type I structure.

It is important to point out that, for the above EM tests, the test condition was set to keep the current density in the M2 line constant at 1.0 MA/cm^2. Under the circumstances, for the type I structure, the current density in the via and the M2 line were the same since the via width scaled with the M2 line width. However, for the type II structure, while the current density in the M2 line was fixed at 1.0 MA/cm^2, the current density in the via increased from 1.5 to 2.9 MA/cm^2 as the M2 line width increased from 90 nm to 175 nm. The previous discussion focused on EM reliability by considering the current density in the M2 lines. If the current density in the via is considered instead, it is interesting to find out that, for the type II structures, even though the current density in the via is scaled, the EM lifetime and statistics remain the same. This indicates that the higher via current density for the wider M2 line does not cause degradation of the overall EM reliability. In actual ICs, it is common to have such configurations as a small via is connected to a much wider metal line. Therefore, it is of practical interest to determine the maximum line width that can be connected to a single via or the maximum current density a single via can support without degrading the overall EM performance. It is also an important parameter for the layout designers.

3.2.4 EM Lifetime Distribution for Type II Structures at *j* = 2.0, 4.0 MA/cm^2

It is of industrial significance to test the type II structures with the 90 nm via but wider M2 line width. However, the testability of this study is limited by the available maximum M2 line width, which was designed as 175 nm in the type II structure. An alternative approach is to apply a higher current density through the M2 line, which would, in turn increase the current density through the via. Therefore, current densities of 2.0 and 4.0 MA/cm^2 were applied to the type II structures with M2 line widths of 90 nm and 175 nm, and the temperature was maintained constant at 330 ^{o}C. EM lifetime data under these test conditions are shown in Figures 3.6 and 3.7 for current densities of 2.0 MA/cm^2 and 4.0 MA/cm^2, respectively. It was found that, tested at a higher current density, the wider Cu line possessed a longer EM lifetime. Such an observation appeared to be inconsistent with the EM results in Figure 3.2(b) where the Cu line width did not affect the EM lifetime distribution.

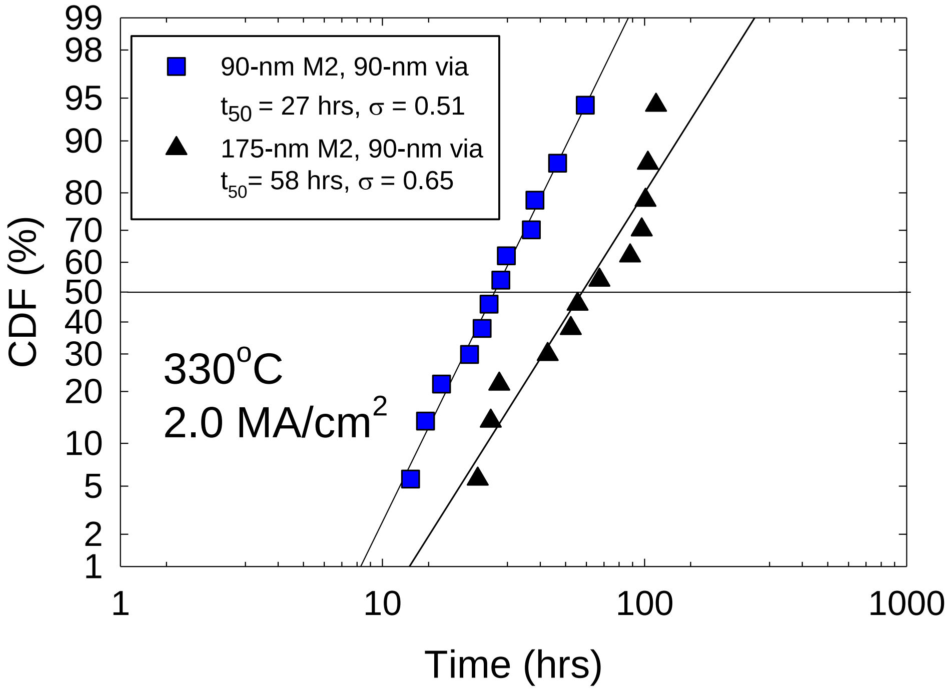


Figure 3.6 CDF plots of the type II structures with the M2 line widths of 90 nm and 175 nm. The upstream EM tests were performed at T = 330 ^{o}C, with a current density of *j* = 2.0 MA/cm^2.

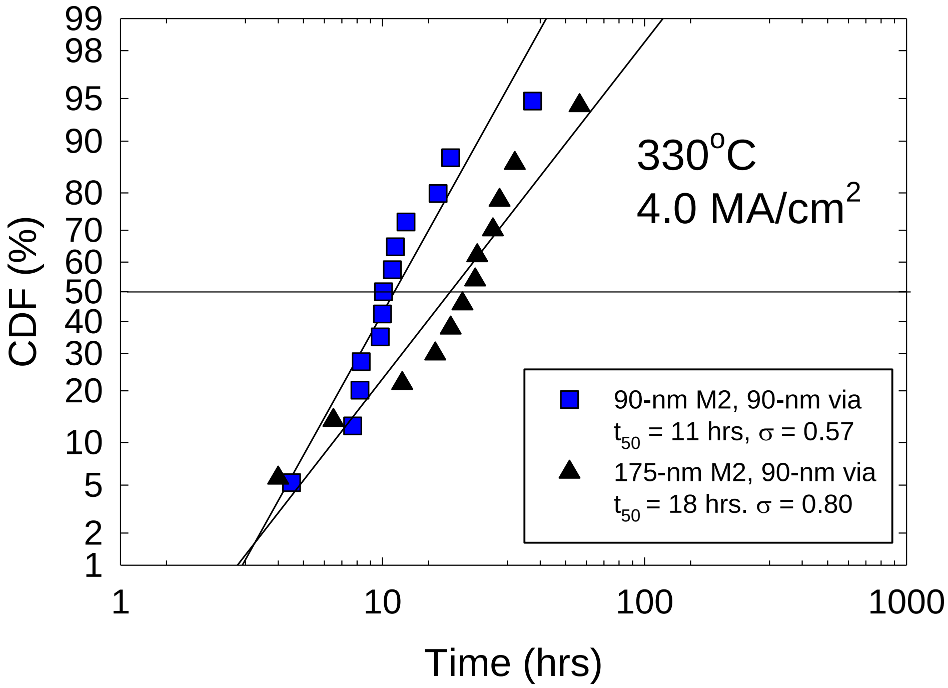


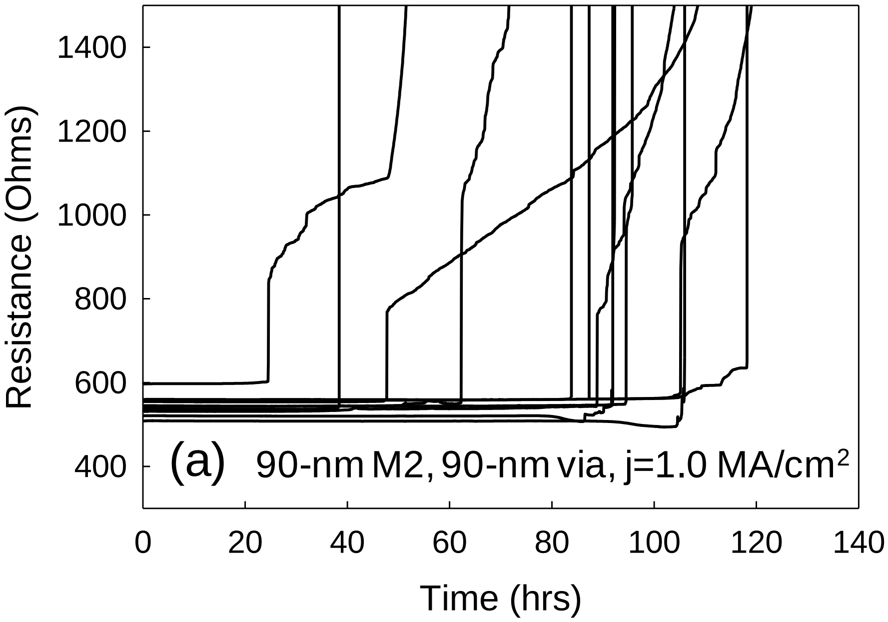
Figure 3.7 CDF plots of the type II structures with the M2 line widths of 90 nm and 175 nm. The upstream EM tests were performed at T = 330 ^{o}C, with a current density of *j* = 4.0 MA/cm^2.

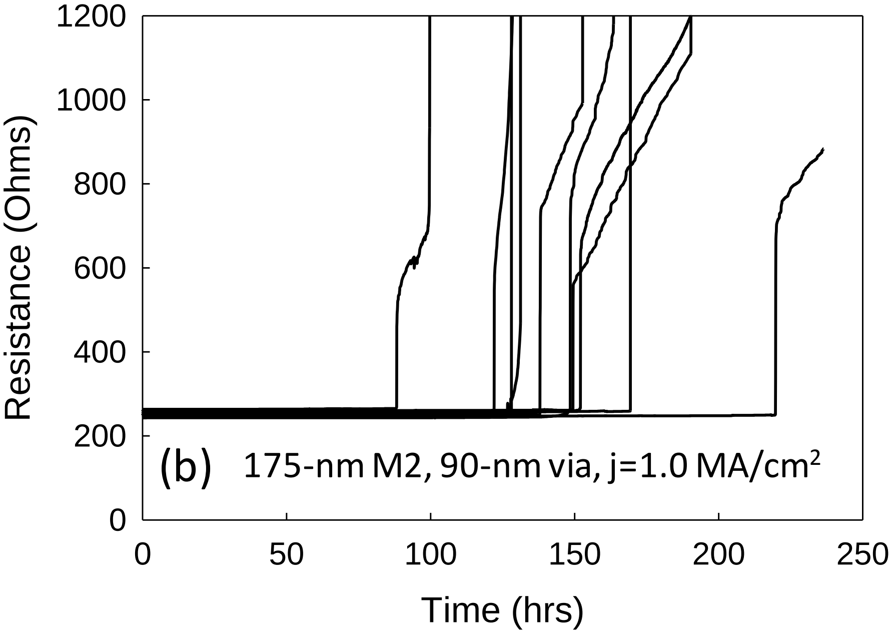
In order to probe the root cause of the discrepancy, detailed failure analysis was carried out on EM failed structures. Resistance traces of samples tested at *j* = 1.0, and 2.0 MA/cm^2 were compared in Figure 3.8. At a low current density of *j* = 1.0 MA/cm^2, the resistance traces of the test samples were dominated by the progressive resistance increases, which corresponded to the intrinsic trench voiding failure mechanism. However, at a high current density of *j* = 2.0 MA/cm^2, the resistance traces were predominantly step-like abrupt resistance increases, which corresponded to the extrinsic failure mechanism caused by process-induced defects. These defects may be caused by several factors.

First of all, the manufacturing process of the test structures might not have been mature, hence there are relatively large thickness variations in the Ta barrier layer which encapsulates the Cu lines. When a high current density, e.g. 2~4 MA/cm^2, was applied during the EM test, the unstable Ta barrier with uneven thickness could barely support the current. Consequently, an open failure occurred instantly after the void span over the whole via, resulting in a step-like resistance increase.

Second, due to the unrefined process control of the Cu dual damascene process, the via bottom could be exposed to process-induced defects during the via etching, cleaning, and barrier deposition process. Thus, due to the reduced adhesion strength, the via bottom interface can serve as 'weak points' during EM, and voids can readily form there.

One more thing to point out is that the EM samples used for high current density tests had been exposed to the air for more than one year before the EM tests were actually carried out. Even though a SiN_x passivation layer was on the top for protection, there might have been some degradation already present in the test structures before the test, such as the moisture uptake in the low-*k* dielectrics, oxidization or degradation of the Ta barrier layer, and degradation of the SiN_x cap interface.


1400
1200
1000
800
600
400
Resistance (Ohms)
(a) 90-nm M2, 90-nm via, j=1.0 MA/cm^2
0
20
40
60
80
100
120
140
Time (hrs)


1200
1000
800
600
400
200
0
Resistance (Ohms)
(b) 175-nm M2, 90-nm via, j=1.0 MA/cm^2
0
50
100
150
200
250
Time (hrs)

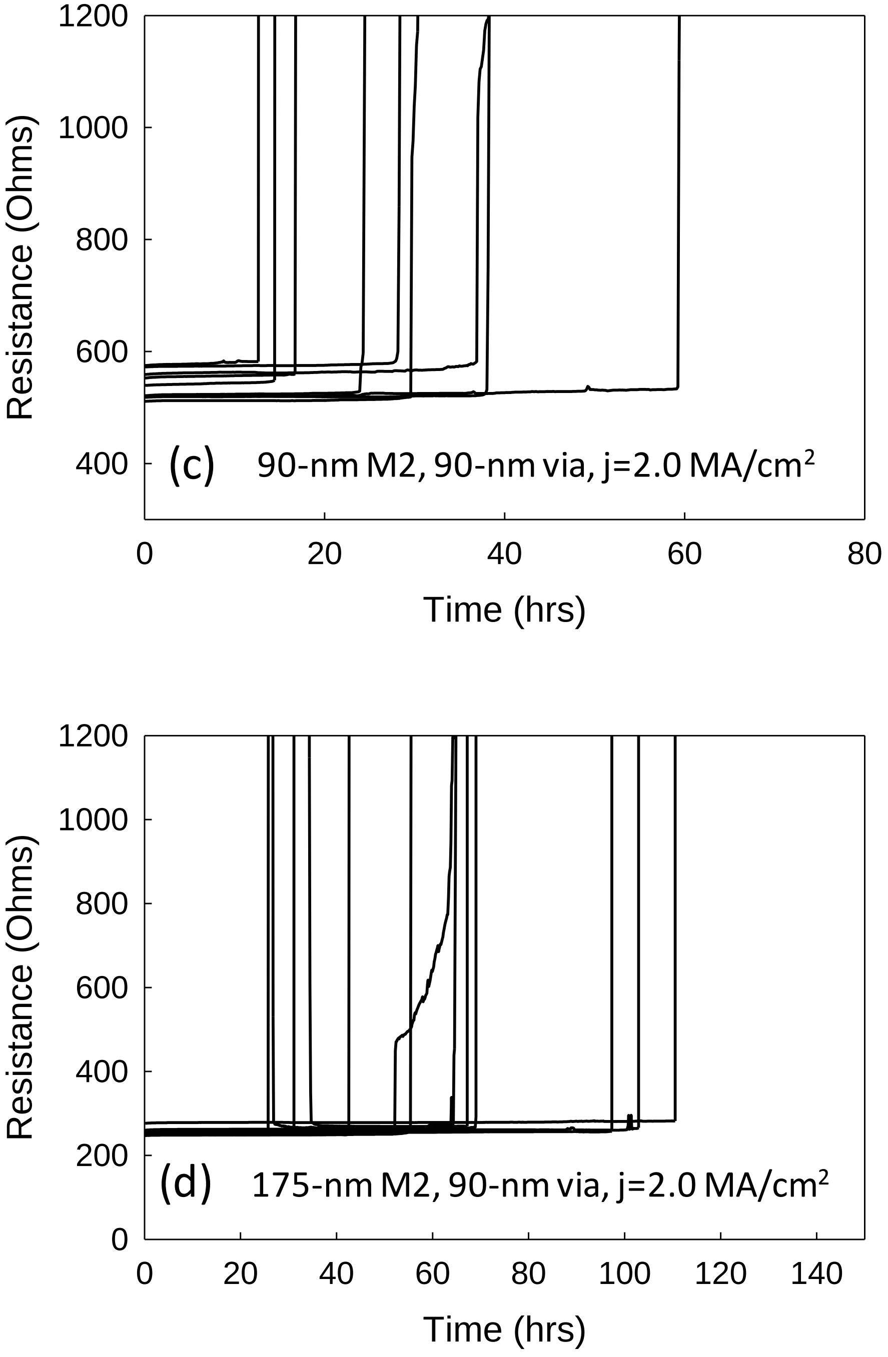
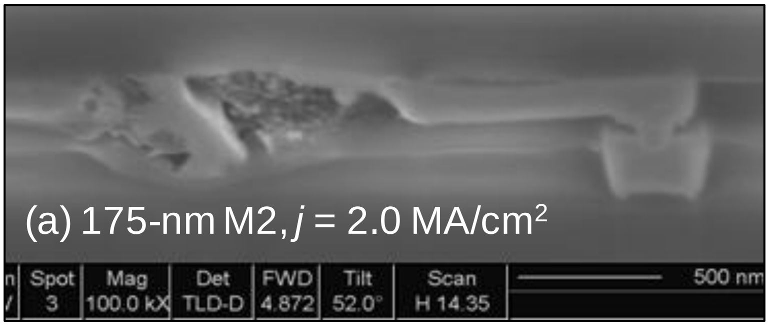


Figure 3.8 Resistance traces of the type II structures tested at different current densities: (a) 90 nm M2 line, *j* = 1.0 MA/cm^2, (b) 175 nm M2 line, *j* = 1.0 MA/cm^2, (c) 90 nm M2 line, *j* = 2.0 MA/cm^2, (d) 175 nm M2 line, *j* = 2.0 MA/cm^2.

The two different failure mechanisms result in different EM behaviors. For intrinsic failures at the low current density, the EM lifetime distribution is the same for different line widths. However, for extrinsic failures at the high current densities, the EM lifetime is controlled by the defect level. The higher defect level in the 90 nm M2 lines results in a shorter EM lifetime compared with the 175 nm lines. In this case, the EM data obtained at higher current densities could no longer be used to extract the maximum current density that a single via can support. To obtain more meaningful results, test structures with better process control are required.

Some of the failed samples tested at high current densities were examined at the cathode end to confirm the failure mechanism. Two typical examples are shown in Figure 3.9. The failure location is close to the cathode end but not right above the via. Figure 3.9(a) shows a severe burn-out of the Ta barrier and Cu out-diffusion at the void position for the 175 nm M2 line tested at j = 2.0 MA/cm^2. Figure 3.9(b) shows a long void in the trench away from the cathode end and an irregular shape of void above the via for the 90 nm M2 line tested at j = 4.0 MA/cm^2. The irregularities of the void shape and location and out-diffusion of Cu are suspected to be due to the process-induced defects and unrefined process control.



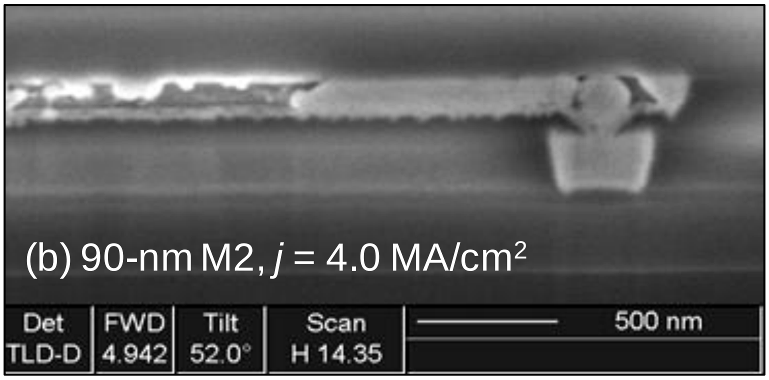


Figure 3.9 SEM images of two typical EM failed samples for the type II structures tested at high current densities: (a) 175 nm M2 line tested at $j = 2.0$ MA/cm^2 and (b) 90 nm M2 line tested at $j = 4.0$ MA/cm^2.

However, once the process is matured for each technology node, the extrinsic failures should be significantly reduced and not be a limiting factor in controlling EM reliability of Cu interconnects. The intrinsic via reliability can then be evaluated by testing the type II structures. Similar via reliability study was demonstrated by Lee *et al.* from Texas Instruments [Lee 2008]. Their test structures were similar to the type II structures except that the via width was 0.1 µm and the M2 line width varied from 0.1 to 2.0 µm, a much larger range of line width variation. The results reported in Reference [Lee 2008] are consistent with this study in that the EM behavior remains the same for different line widths except for the widest line width of 2.0 µm. The maximum current density that a single via can support without EM degradation was reported to be 32 MA/cm^2 and 13.0 MA/cm^2 for the upstream EM and downstream EM, respectively. These values were defined as the critical current densities, J_{cr}. Depending on the current density in the via, the EM lifetime exhibited two different behaviors. When J_{via} was smaller than the critical value J_{cr}, the EM lifetime was controlled by the current density in the metal line (J_{met}). However, when the metal line was very wide, inducing a much higher J_{via}, larger than J_{cr}, the EM lifetime was then controlled by J_{via}. The EM results for downstream EM tests in Reference [Lee 2008] are shown in Figure 3.10 for illustration.

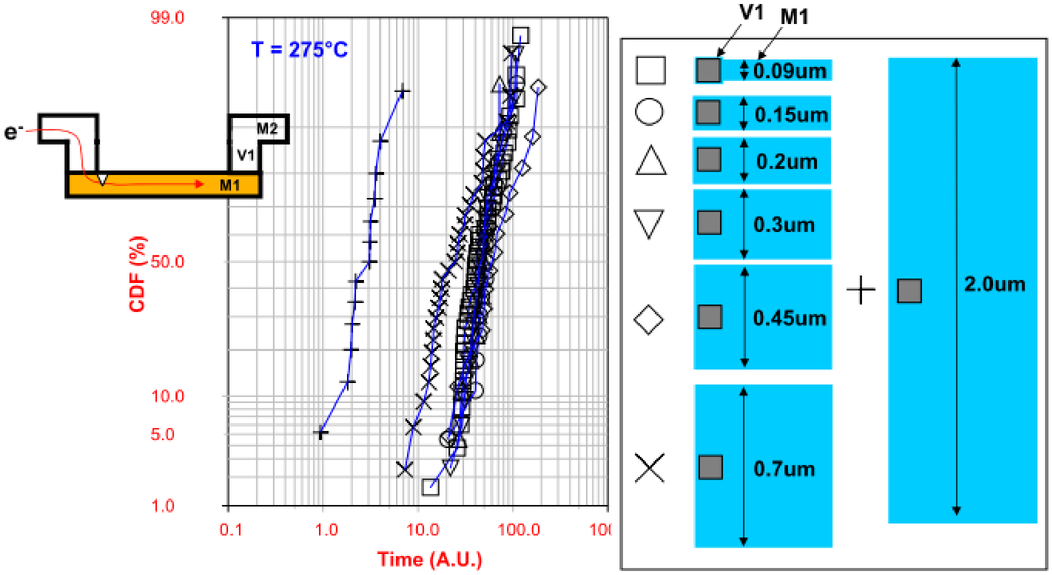


Figure 3.10 Downstream EM CDF plots with various M1 line widths tested at 275 ^{o}C. J_{met} is fixed at 2.0 MA/cm^{2}. J_{via} are 2.5, 4.2, 5.6, 8.4, 12.6, 19.6, and 56.0 MA/cm^{2} [Lee 2008].

3.3 LINE SCALING EFFECT ON GRAIN STRUCTURES OF CU INTERCONNECTS

3.3.1 Sample Preparation

The Cu line structures were fabricated by Sematech using standard damascene process. The intermetal dielectric (IMD) materials were silicon oxide (SiO_2). To produce very narrow lines, a SiON filling layer was deposited after the formation of line trenches in the SiO_2 dielectric layer. This was followed by Ta barrier and Cu seed deposition and Cu electroplating. Then after CMP, a SiN_x layer was deposited as capping and passivation to protect the Cu lines. The Cu lines used for this study were 850, 185 and 60 nm in width, 110 nm in height, and 150 µm in length. Figure 3.11 shows the schematic layout of the sample.

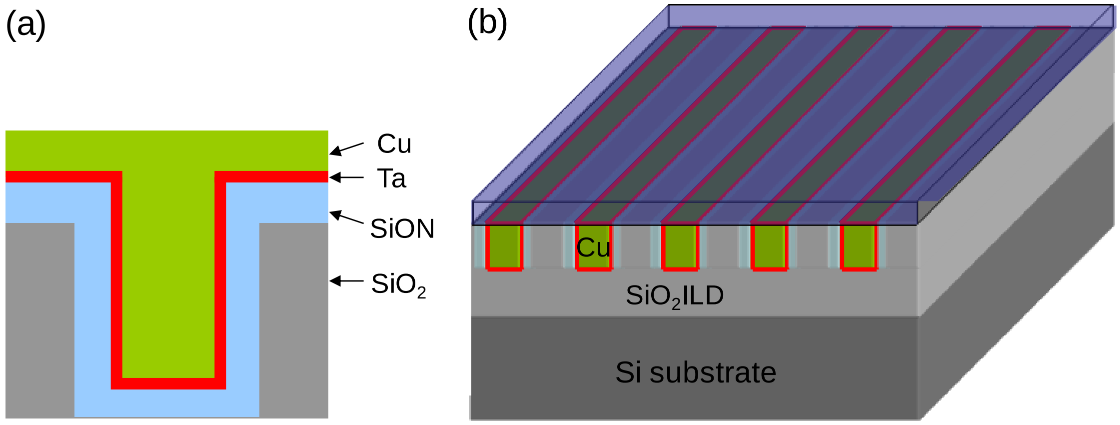
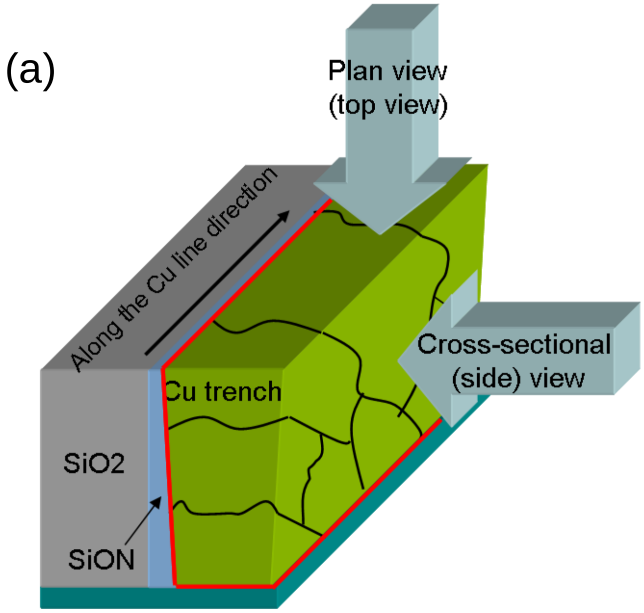


Figure 3.11 (a) Cross-sectional illustration of Cu trench with SiON filling. (b) Schematic diagram showing the periodic Cu line structures.

Both plan-view (top view) and cross-sectional (side view) TEM samples were prepared to study the Cu grain structures along the Cu line direction. Figure 3.12(a) shows a schematic illustration of the TEM sample. Planar TEM sample was prepared using a conventional method consisting of the following steps: 1) cutting a 2 mm square specimen with Cu line structures approximately at the center; 2) gluing the specimen to a 3 mm radius Ni grid (a single hole in the center) using M-bond 610 adhesive and curing at around 80 ^{o}C for 30 minutes; 3) polishing specimen down to ~100 µm thick using the diamond grit paper. The specimen thickness was roughly controlled by using Gatan Disc Grinder; 4) dimple grinding the specimen to approximately 5 µm thick and 5) ion milling until electron transparency is reached using Gatan Precision Ion Polishing System (PIPS™). The resulting TEM sample consisted of Cu lines confined with Ta liners at both side walls. The top SiN_x passivation layer and bottom Ta barrier layer have already been removed during the ion milling process. Figure 3.12(b) shows a schematic drawing of the plan-view TEM sample.

Site specific cross-sectional TEM sample was prepared using FIB. A 2.5 mm wide and 100 µm thick specimen strip was first prepared using a dicing saw. Before FIB milling, a 200 nm wide and 500 nm thick Pt strip was deposited on the target area to protect Cu lines from damage during ion milling. Then the 100 µm-thick specimen was thinned from both sides down to less 100 nm thick by using Ga ion beam. A FEI Dual Beam FIB equipped with an electron gun allowed the direct observation of the milling process. Final cleaning was done with 30 KeV/10 pA beam to minimize beam damage to the target area. Figure 3.12(c) is an SEM image of one well-prepared TEM sample by FIB. TEM images were taken using JEOL 2010F and FEI TECNAI G2 F20 microscopes operating at 200 KeV.



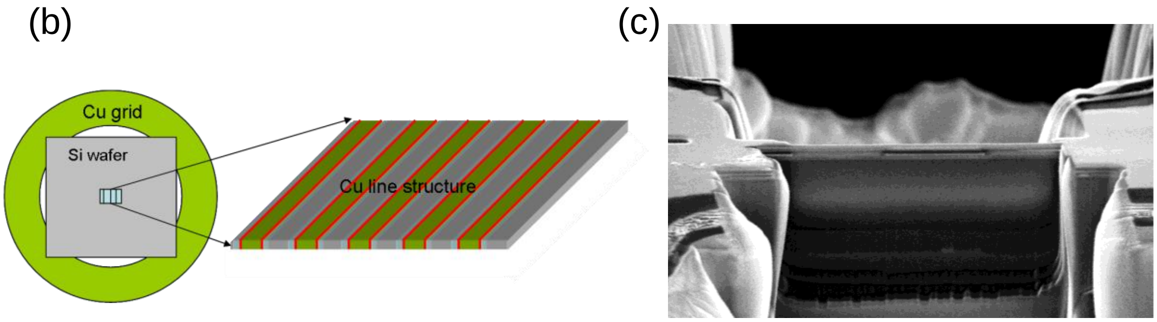


Figure 3.12 (a) Schematic diagram showing plan-view (top view) and cross-sectional (side view) observations of Cu interconnects using TEM. (b) Schematic drawing of a well-prepared plan-view TEM sample. (c) SEM image of one well-prepared cross-sectional TEM sample.

3.3.2 Plan-view TEM Observation

Figure 3.13 shows the plan-view TEM images of Cu interconnects with line width (a) 850 nm, (b) 185 nm, and (c) 60 nm. Distinct difference in the Cu microstructures can be observed for different line widths. While the 850 nm lines have both bamboo-like and polycrystalline grain structures, the 185 nm and the 60 nm lines have predominantly bamboo-like structures with the presence of microtwins. Statistical analysis on the grain size distribution was carried out on the 185 nm and the 60 nm wide lines, and the results are shown in Figure 3.14. The grain size was calculated as the diameter of the grain area by assuming the grain to be of circular shape. It shows that the average grain size scaled as the Cu line width decreased from 185 nm to 60 nm. It is also observed that the narrow 60 nm lines had a higher population of small grains. This observation is consistent with the results reported in previous work [Hu 2007].

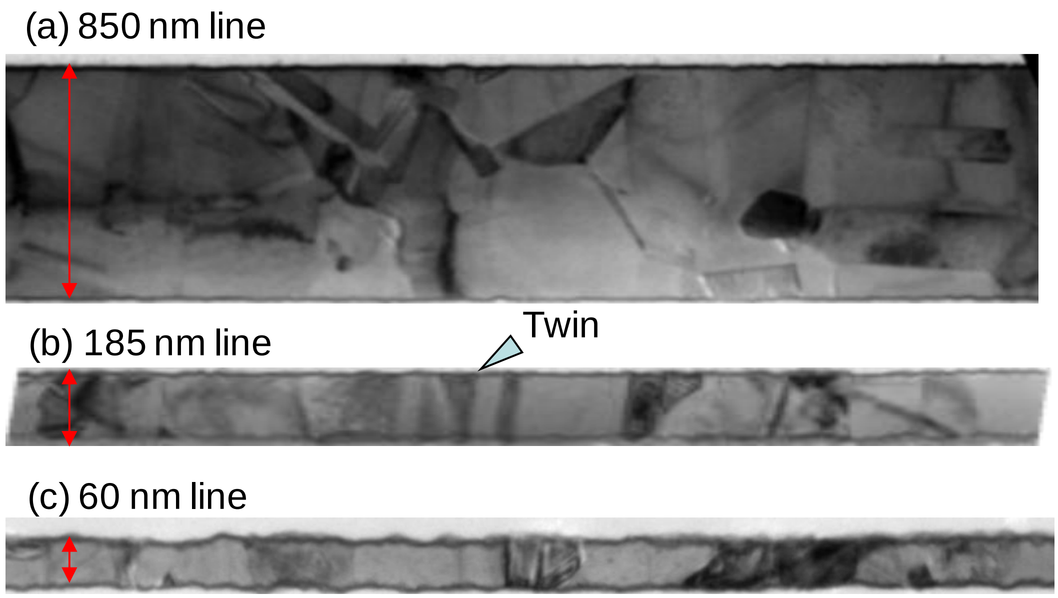


Figure 3.13 Plan-view TEM images of (a) 850, (b) 185, and (c) 60 nm Cu lines.

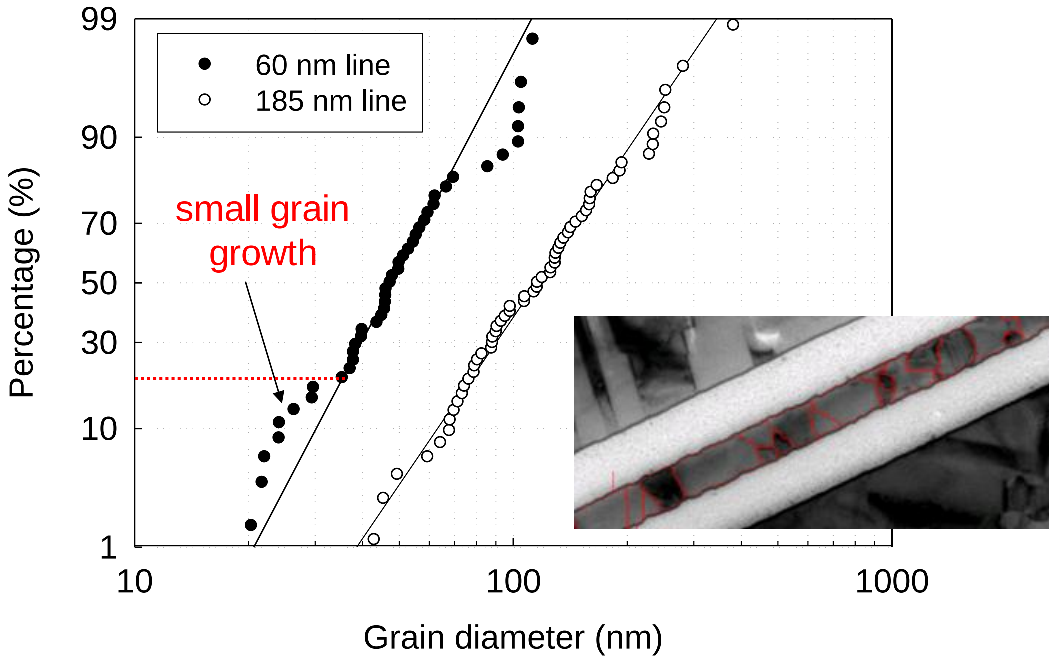
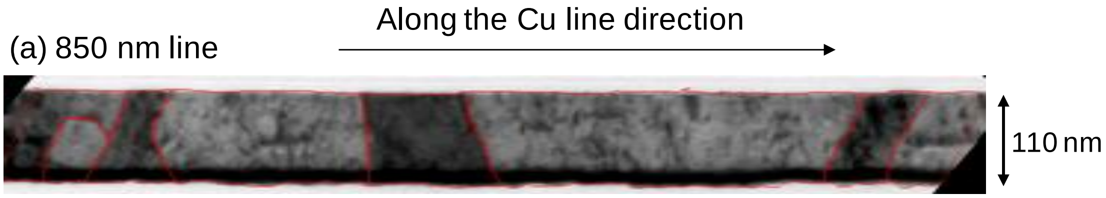


Figure 3.14 Grain size distributions of 185 nm and 60 nm Cu lines. The inset is a plan-view TEM image of 185 nm Cu lines with the grain boundaries delineated in red.

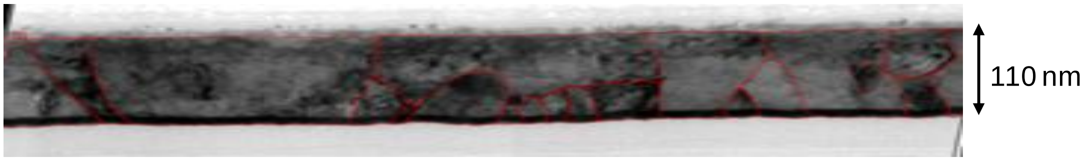
3.3.3 Cross-sectional TEM Observation

Figure 3.15 shows the cross-sectional (side-view) TEM images of Cu interconnects with line widths of 850 nm, 185 nm and 60 nm. In Figure 3.15(a), the 850 nm lines show bamboo-like grain structures across the line thickness along the Cu line direction. In Figures 3.15(b) and 3.15(c), the 185 nm and the 60 nm lines have both polycrystalline and bamboo-like grain structures throughout the trench line. Some sections of the line were observed to have one single grain spanning the thickness, while other sections showed multiple grains across the thickness with more small grains at the trench bottom. No significant difference in the microstructures of the 185 nm and the 60 nm lines were observed in this study. However, narrower lines have been reported to have more small grains due to the larger proportion of PVD Cu seed at the trench bottom during Cu deposition which prohibited extensive grain growth to bamboo-like structure [Hu 2007].

(a) 850 nm line



(b) 185 nm line



(c) 60 nm line

Figure 3.15 Cross-sectional TEM images of (a) 850, (b) 185, and (c) 60 nm Cu lines.

Grain growth in general is driven by minimization of energies, including that associated with the surface, interface, grain boundary, and elastic strain. With scaling increasing the interface to volume ratio, interfacial pinning at the sidewalls and trench/via bottoms is expected to become more effective in anchoring small grains. This will favor the formation of small grains near the line bottom as the line width decreases.

3.3.4 Monte Carlo Simulation

In addition to the direct observation of the cross-sectional grain structures using TEM, numerical simulations can serve as a good supplementary tool. Simulation approaches make it possible to track the evolution of each specific grain during grain growth, which would be impossible with conventional, microscopy-based cross-sectional observations. In addition, the grain structure obtained from simulations can be used as the input structure of EM lifetime assessment tools [Knowlton 1997]. This can significantly reduce the test time and predict the EM reliability of certain structures.

Due to the different fabrication procedure, the grain structure evolution in Al interconnects and Cu interconnects are dramatically different. For Al interconnects, the Al film is first sputter-deposited. This is followed by the photolithography and RIE processes to obtain the Al lines. The grain structure evolution in Al interconnects is essentially the same with that in the Al film, which can be well described by the two dimensional (2D) grain growth simulation used for thin films [Knowlton 1997, Thompson 1985, Frost 1993]. However, for Cu interconnects fabricated by the damascene process, the grain growth starts after Cu is deposited into the trenches by electroplating. The trench and via geometry plays an important role in controlling the grain evolution and the resultant structure. Therefore, the 2D grain growth model is no longer sufficient, and a three dimensional (3D) model must be implemented to better simulate the grain evolution in Cu interconnects. Furthermore, during Cu electroplating, chemical additives are required for Cu superfilling of the damascene structures with high aspect ratios and narrow linewidths. These additives are incorporated into the Cu lines and affect their grain structure evolution even at room temperature [Harper 1999, Ritzdorf 1999]. Therefore, the actual grain growth in damascene Cu interconnects is a rather complicated process and is affected by many parameters. It is important to simplify the problem to provide valuable understanding of the effect of each parameter on grain growth. In the following study, the grain growth in Cu interconnects is simulated by considering the interface/surface and grain boundary energies. The strain energy and the chemical impurity effect are neglected in this model. The grain boundary energy is assumed to be isotropic. Only anisotropy in the interface/surface energy is considered as the driving force of the abnormal grain growth.

3.3.4.1 Simulation Details

A 3D Monte Carlo method based on the modified Potts model is used in this study. The Cu line is represented by a simulation box consisting of 50x50x200 cubic lattice sites, in which the numbers 50, 50, and 200 correspond to the width, height and length of the Cu interconnects. Grain growth in this model is driven by the energy minimization resulting from the orientation exchange of a given site with one of its nearest neighbors. The energy H of the system can be written as:

$$H = \sum_{i}^{N} \sum_{j}^{n} \frac{J_{ij}}{2} (1 - \delta_{S_i S_j}) + \sum_{i}^{N} E_i \tag{3.2}$$

where δ is Kronecker delta. The system energy H includes the grain boundary energy J_i and the surface/interface energy E_i summing over all the sites i in the system. The orientation of site i is specified by the orientation number S_i. N refers to the number of lattice sites and n is the number of nearest neighbors of each site, which is 26 in this model by including up to the third nearest neighbors. In the simulation, the orientation of each site is allowed to change into that of one of its nearest neighbors if the system energy H is not increased; otherwise, it is still allowed with the Boltzmann probability p:

$$p = \exp(-Q / k_B T) \tag{3.3}$$

where Q is the activation energy of grain boundary migration, k_B is the Boltzmann constant, and T is the simulation temperature. To convert the simulation temperature into the real value, Q has to be determined. Since the energy unit in Equation (3.2) used in the simulation is arbitrary and the activation energy cannot be determined explicitly, it is difficult to convert the unit of the energy H into that of the thermal energy k_BT. Thus, Equation (3.3) is simplified as:

$$p = \exp(-2\Delta H) \tag{3.4}$$

where ΔH is the energy difference due to the trial of the orientation number exchange and the factor two is an arbitrary value.

Two different cases are examined and compared in this study. The first case is the isotropic, single-phase normal grain growth by including solely the grain boundary energy without taking into account the interface or surface energies. The second case includes the anisotropic "surface" energy in the model to simulate the overburden and surface effects.

3.3.4.2 Simulation Results and Discussion

Case I is first simulated in which the surface or interface energy is not considered. The width and height of the damascene interconnect structure is set as 50 sites, and the length is set as 200 sites. The overburden above the trench is not considered in this model. The isotropic grain boundary energy J_i is set as 1. The elapsed simulation time is counted in the unit of Monte Carlo Step (MCS), which is defined as the time required for all the lattice sites in the simulation box to experience one reorientation trial. The simulation results of Case I are shown in Figure 3.16 corresponding to MCSs of 2, 50, 200, and 500. It is clear that initially small grains grow into larger grains and finally transform to bamboo or near-bamboo structures.

Case II is then simulated in which the anisotropic “surface” energy is included. For simplicity, two different surface energies, a high value of 10 and a low value of 1, are applied to the top surface of the Cu line to simulate the abnormal grain growth induced by the overburden and surface effects. The interface energies at the sidewalls and trench bottom are ignored. The simulation results of Case II are shown in Figure 3.17. It can be seen that, at the initial stage, the small grains in the trench are identical to those in Case I where grains of different orientations are evenly and randomly distributed in the line. As the time elapses, the small grains grow larger. The effect of the anisotropic “surface” energy at the top surface then begins to play a role. To explicitly demonstrate the effect of surface energy, only grains with three specific orientations are assumed to have a low surface energy of 1 while grains with all other orientations are assumed to have a high surface energy of 10. The difference in the high and low surface energies is exaggerated here in comparison to the experimentally measured values [Porter 1981, Humphreys 1995, Mclean 1971, Li 1997]. It is clear that grains with low surface energies grow larger at the expense of the grains with high surface energies. The grains with low surface energies were observed to grow toward the bottom of the trench. This strongly supports the experimental observations of the overburden effect on grain growth in the damascene trench. The preferential grain growth from the trench top to bottom yields a microstructure with relatively large grains at the trench top and relatively small grains at the trench bottom. Such findings are consistent with the experimental observations in this work and in previous reports [Hu 2007].

It is important to point out that Case II can effectively simulate the abnormal grain growth in the trench caused by the overburden and surface energy anisotropy. Grain structures similar to the actual Cu microstructures can be generated using this method. The resultant microstructures could serve as the input structure of the EM lifetime model to simulate the scaling effect or the grain structure effect on EM reliability. Note that it is a simplified phenomenological model without considerations of strain energy and impurity effects.

It is also important to consider at what point the simulation should be stopped to best represent the microstructures in real Cu damascene interconnects. Given a long enough evolution time, the Monte Carlo simulation will eventually lead to a bamboo structure in the trench, which is not the case in real structures. With limited thermal budget, Cu interconnects with high aspect ratios do not always evolve to bamboo structures. As demonstrated in the previous section, more small grains occur at the trench bottom as the interconnect scaling continues, particularly for ultra-narrow Cu lines.

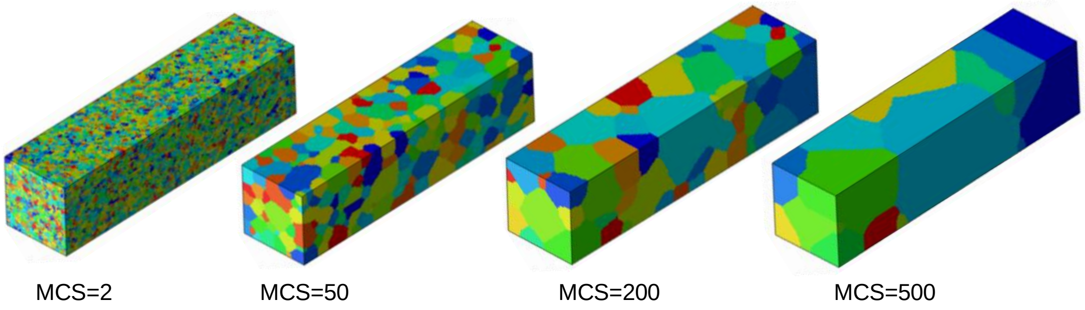


Figure 3.16 Simulation results of the microstructure evolution in the damascene structures by considering only the isotropic grain boundary energy. The width and height of the trench are both 50 sites, and the length is 200 sites.

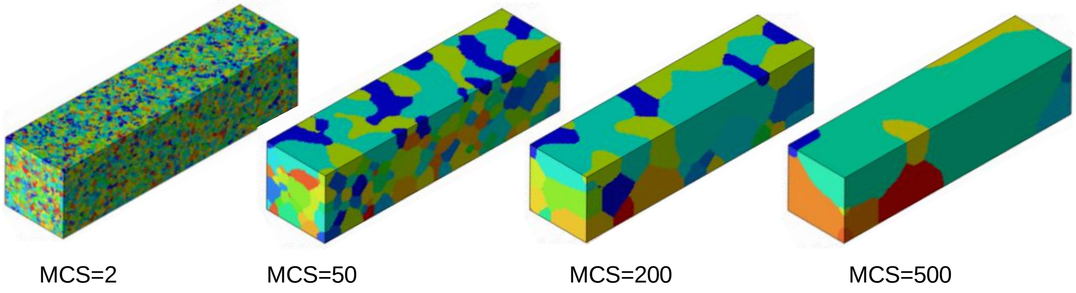


Figure 3.17 Simulation results of the microstructure evolution in the damascene structures by considering the isotropic grain boundary energy and the anisotropic "surface" energy.

3.4 SUMMARY

In this chapter, the effect of via scaling on EM reliability and the effect of line scaling on Cu microstructures were investigated.

The via scaling effect on EM reliability of Cu/low-k interconnects was studied using two types of upstream EM test structures. EM tests were first performed by keeping the current density in the M2 line constant as 1.0 MA/cm^2. For the type I structure in which the line width was scaled with the via size, the EM lifetime degraded with the via size scaling. However, for the type II structure with a constant via size, the EM lifetime and statistics were found to be similar in spite of the varied M2 line width. The difference in the EM behaviors for the two types of structures can be interpreted by using an intrinsic failure model. In this model, the cathode end trench voiding is driven by the Cu/SiN$_x$ cap interfacial mass transport and the EM lifetime is directly proportional to the critical void length, which is equal to the via size in this study. Further investigation of the EM data for the type II structure showed that the via connected with wider M2 lines could support higher current density without degrading the overall EM reliability. An important parameter, the maximum current density a single via can support, was evaluated by applying higher current densities, 2~4 MA/cm^2, to the type II structure. However, due to the process control of the samples and some external damage, it was difficult to extract a meaningful value from the EM data. Nevertheless, the results of this study provide useful insights of the via and line scaling effects on EM reliability for Cu interconnects.

The line scaling effect on Cu microstructures was investigated on ultra-narrow Cu interconnects fabricated by the damascene process with a trench filling of SiON layer. Both plan-view and cross-sectional TEM samples were prepared and investigated for Cu lines with different line widths: 850, 185, and 60 nm. Plan-view TEM images showed that the 850 nm lines had both polycrystalline and bamboo-like grain structures. However, the 185 nm and the 60 nm lines had near bamboo grain structures. Statistical analysis of the grain size distribution was performed and it showed that, compared with the 185 nm lines, the 60 nm lines had a higher population of small grains. Such a change in the grain structure was attributed to scaling-induced small grain growth. Cross-sectional TEM images showed that the 850 nm lines had bamboo-like grain structures across the line thickness; while the 185 nm and the 60 nm lines had a mixture of polycrystalline and bamboo-like structures with more small grains at the trench bottom. The presence of more small grains in the ultra-narrow Cu trench was attributed to the inadequate grain growth possibly due to a higher surface to volume ratio of the trench and a larger proportion of Cu seed at the trench bottom. A 3D Monte Carlo method based on the modified Potts model was used to simulate the grain growth in damascene structures. Two different cases were studied: in Case I, only the isotropic grain boundary energy was considered, while in Case II, both the isotropic grain boundary energy and the anisotropic surface energy were included. The results of Case II study effectively showed the effects of overburden and the surface energy on the microstructure evolution in damascene structures. Grain structures with smaller grains at the trench bottom were obtained using the Case II model. The resultant microstructure can be used as the input structure of the EM lifetime model to investigate the scaling-induced grain structure effect on EM reliability.

Chapter 4: Cap Layer and Grain Structure Effects on Electromigration Reliability of Cu Interconnects

4.1 INTRODUCTION

For Cu interconnects, it has been well accepted that the EM-induced mass transport along the Cu/SiN_x interface is faster than along the Cu grain boundaries due to the defects on the Cu interface created during the CMP process before the cap layer deposition [Hu 1999, Hau-Riege 2001, Hu 2006, von Glasow]. Prior to the 65 nm node with the line width exceeding 100 nm, the Cu damascene lines were commonly observed to have a bamboo-like grain structure where the Cu/SiN_x interface diffusion dominated the mass transport. In this case, the EM lifetime degraded by half for each new technology node due to the geometrical scaling of the critical void size, even when subjected to the same current density [Hu 2006].

The continuous degradation of EM reliability has stimulated great interests to develop methods to strengthen the cap interface for suppressing the interfacial mass transport and improving EM reliability. Among the various approaches, the implementation of a metal cap layer was found to be particularly effective where two orders of magnitude improvement in EM lifetime was reported with the application of a CoWP cap layer [Hu 2002b, Hu 2003b, Gambino 2006, Meyer 2007, Zhang 2010]. So far, the effect of the CoWP layer on the EM damage formation and lifetime statistics is not well understood. Once the diffusion at the interface is suppressed by the CoWP cap layer, the cap interface is no longer the fastest diffusion pathway. Then the grain boundaries and the Cu/liner interface become increasingly important in contributing to the mass transport comparing to the Cu/cap interface. This can cause a fundamental change in the void formation and evolution process, as well as the EM lifetime and its statistical deviation. The implication of these material and processing issues has to be understood in order to develop reliable Cu interconnects for future technology generations. For this purpose, a comprehensive study is required to understand the mass transport and failure mechanisms which control the EM lifetime and statistics for future Cu interconnects as device scaling continues.

One important scaling effect is the change in the grain structure of the Cu line with the line width. As discussed in Chapter 3, when the Cu line width scaled down to 90 nm or less, the Cu grain structures were no longer bamboo-like. Random line sections of polycrystalline grains were observed, especially at the trench bottom [Hu 2007]. As scaling continues, the Cu trench aspect ratio and the surface to volume ratio continue to increase, making it increasingly difficult to completely fill the Cu trench and to obtain bamboo-like grain structures. This raises an interesting and important question regarding the effect of grain structure on EM reliability for future Cu interconnects, particularly with the implementation of a metal cap layer.

The objective of this chapter is to investigate the effects of cap layer and grain structure on Cu EM reliability including the EM lifetime, statistics, and failure modes. First, the effect of failure criteria on EM lifetime and failure mechanism is discussed. This is followed by a review of the correlation between the void growth and the resistance trace during EM. Then the cap layer and grain structure effects on EM reliability of Cu interconnects are investigated by performing downstream EM tests on four sets of Cu lines: large or small grains with CoWP or SiCN caps. Based on the experimental results, this chapter is concluded with an analysis of the cap layer and grain structure effects on the EM lifetime scaling for the future technology nodes.

4.2 EXPERIMENTAL DETAILS

The test structures used for this study were fabricated by GLOBALFOUNDRIES using the 45 nm technology process. All test samples were fully built wafers with five Cu layers and different interlayer dielectric (ILD) materials (dense and porous low-*k* dielectrics). Figure 4.1 shows the two types of single-linked EM test structures used for this study. The type I structure consists of two-level interconnects with the M1 line as the current stressing line. The type II structure consists of three-level interconnects with the M2 line as the test line. The M1 test line is 72 nm wide and 110 nm thick while the M2 test line is 80 nm wide and 144 nm thick. Both test lines are 200 μm in length. Two different cap layer configurations were applied to the type I structure at the M1 level: low-*k* SiCN cap with and without a CoWP layer in between Cu and SiCN. The same cap layer configurations were applied to the type II structure at the M2 level. In addition, for the M2 test line, two different grain sizes, large and small, were obtained by changing the current-profile during electroplating. In this way, four sets of samples were fabricated for the type II structure: Cu interconnects with large and small grains with and without a CoWP cap. In the following discussion, the SiCN cap with and without the CoWP cap will be referred to as CoWP cap and SiCN cap, respectively.

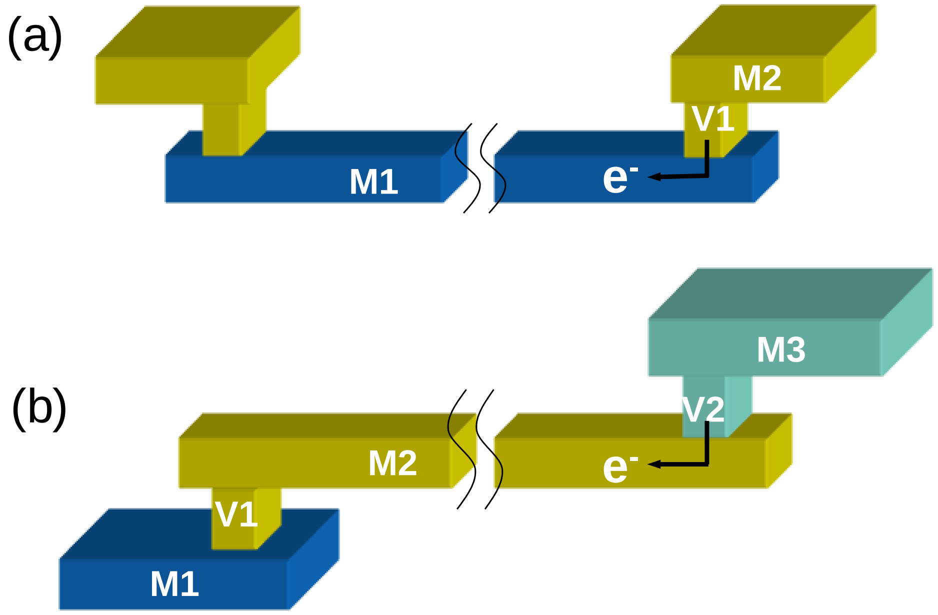


Figure 4.1 Schematic diagrams of downstream EM test structures: (a) two-level structure (Type I) and (b) three-level structure (Type II).

Package level EM tests were performed in the EM test chamber as described in Chapter 2. During the EM test, the DC electron current was passed downward along the M2-V1-M1 and M3-V2-M2 directions for the type I and type II structures, respectively. The test current density was kept constant at 1.34 MA/cm^2 for the type I structure and 1.03 MA/cm^2 for the type II structure. The test temperatures varied ranging from 260 ^{o}C to 330 ^{o}C. The resistance was monitored during the EM tests, and the EM lifetimes were determined at a fixed proportion of resistance increase. FIB and TEM were used for failure analysis and microstructure characterization.

4.3 EFFECT OF FAILURE CRITERION

4.3.1 EM Lifetime and Statistics

The failure criterion of EM tests is commonly selected as the time when the resistance of the test line increases by a certain percentage. Since the resistance change depends on the extent of void formation, setting a different percentage of resistance increase as a new failure criterion can change the EM lifetime and its statistics. To standardize the reliability study, we investigate the effect of failure criterion on EM lifetime, its statistics and the activation energy by performing downstream EM tests on the type I structure with the SiCN cap. The lifetime distribution of the M1 line tested at 330 ^{o}C with a current density of 1.34 MA/cm^2 are plotted in Figure 4.2 based on different resistance increase criteria of 10%, 30%, 50% and 100%. The EM lifetime distributions generally fitted the log-normal distribution very well, independent of the failure criterion. The EM median lifetime t_{50} and standard deviation sigma (σ) are summarized in Figure 4.3 as related to the failure criterion.

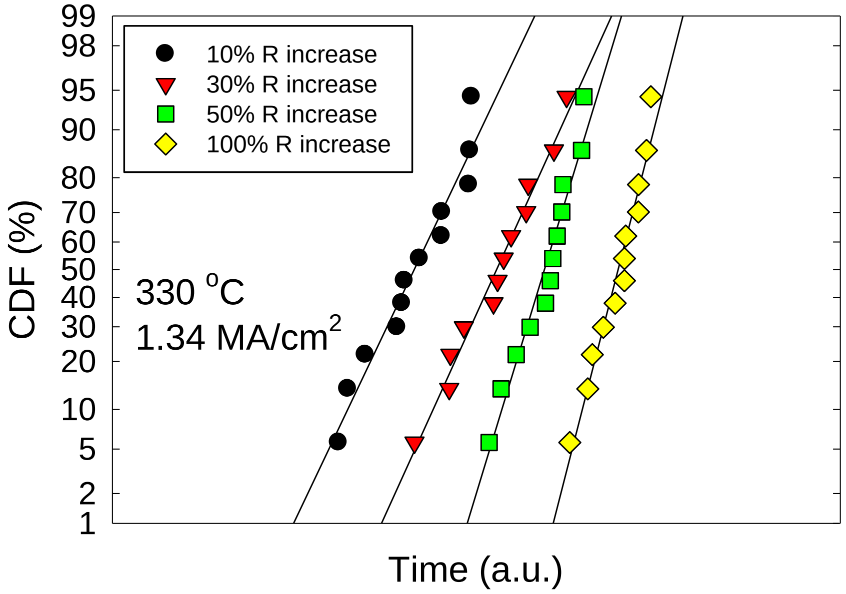


Figure 4.2 CDF plots of the type I structures based on various percentages of resistance increase failure criteria. The EM test was performed at 330 °C, with a current density of 1.34 MA/cm^2.

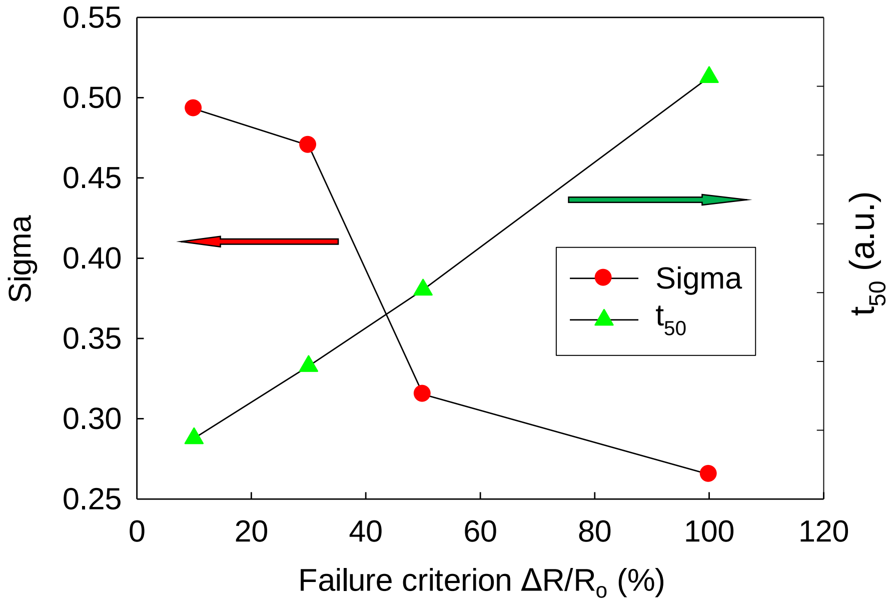


Figure 4.3 Plots of EM median lifetime t_{50} and standard deviation σ vs. various percentages of resistance increase failure criteria.

It can be seen that the median lifetime increases with the increasing failure criterion, simply because it takes a longer time to reach a larger void size and a larger resistance increase. In addition, the standard deviation of the EM lifetime decreases from approximately 0.49 to 0.27 with the increasing failure criterion, which is consistent with the results in the literature [Hauschildt 2007]. The behavior of a smaller sigma with a longer EM lifetime for increasing failure criterion can be understood by considering the void growth and evolution process and the parameters that affect them during the EM damage formation. During the EM test, the statistical variation in the EM lifetime is contributed by a number of factors, including the oven temperature non-uniformity, the current source fluctuation, the line geometry variation, the Cu diffusivity variation resulting from the interface quality and Cu grain orientations, and the shape and size variations of the void formed. For the 5% resistance increase criterion which requires a relatively small void size, all the parameters mentioned above contribute to the lifetime variation. As the resistance change increases in the failure criterion, the void size required is larger, together with a longer current stressing time. In this case, some of the variations can be averaged out. First, given a longer period of time, the Cu lines are likely to develop a similar final void shape and size. This greatly reduces the lifetime variation due to void size and geometry. Moreover, since more line segments are evolved in the mass transport during the void growth, the Cu diffusivity variation originating from the microstructure will be reduced. Thus the EM lifetime variation is primarily controlled by the intrinsic variations such as the line dimension, current density and oven temperature. This will lead to a tighter lifetime distribution. Detailed analysis of the EM lifetime statistics and the effect of each contributing factor can be found in References [Hauschildt 2004, Hauschildt 2006a, Hauschildt 2006b, Hauschildt 2007].

4.3.2 Activation Energy

In order to determine the activation energy, EM tests were performed on the type I structures with SiCN cap at temperatures ranging from 275 ^{o}C to 330 ^{o}C with a current density of 1.34 MA/cm^{2}. The Arrhenius plot of the EM lifetime is shown in Figure 4.4 for different resistance increase failure criteria. The activation energies are obtained by fitting the experimental data to Black's equation:

$$t_{50} = Aj^{-n} \exp(Q / k_B T) \tag{4.1}$$

where A is a constant, j is the current density, n is the current density exponent, Q is the activation energy for EM, and k_B is the Boltzmann constant. The results show that the activation energy remains about the same irrespective of the failure criteria. This is to be expected because the activation energy is an intrinsic EM parameter, which is determined by the bond strength of the dominant diffusion pathways during EM. For Cu interconnects with the SiCN cap, the Cu/SiCN cap interface is the fastest diffusion path controlling the EM activation energy. The activation energies extracted here, 0.82~0.85 eV, are within the range of 0.8-1.1 eV reported in the literature for the Cu/SiN$_x$-based cap interface [Hu 2002a, Fischer 2002a, Tokogawa 2002].

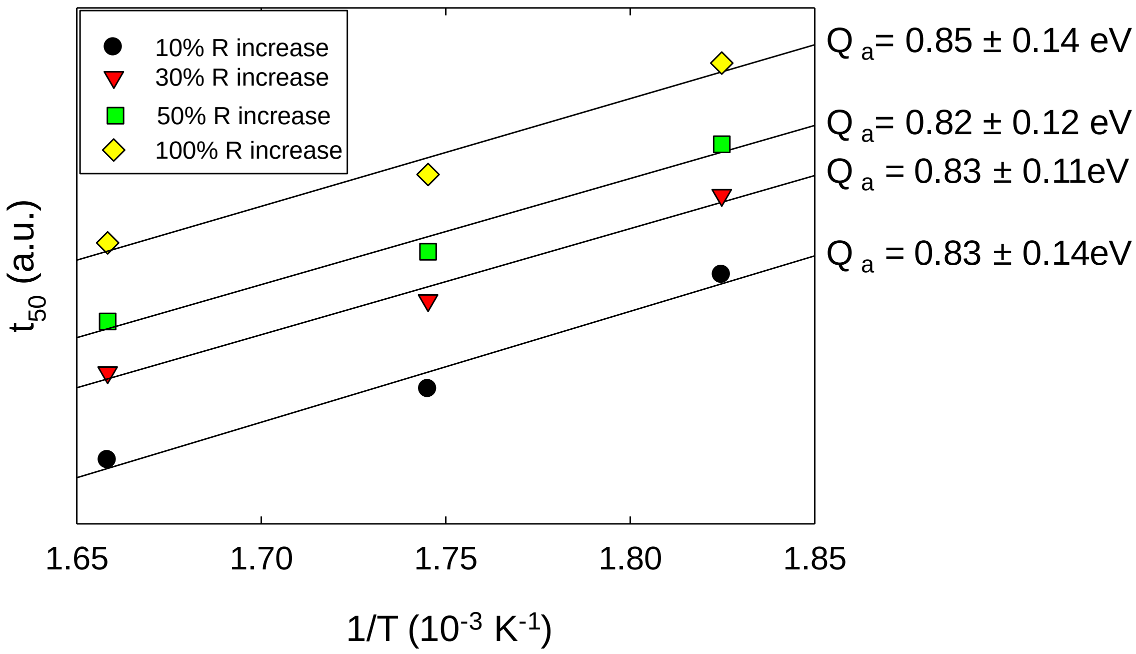


Figure 4.4 Plots of EM median lifetimes as a function of 1/T for various percentages of resistance increase failure criteria. The extracted activation energies are the same, independent of the failure criteria.

Whereas the activation energy of the test structure is independent of the failure criterion, the EM lifetime and the statistical deviation are significantly affected. The larger the resistance increase in the failure criterion, the longer the EM lifetime and the smaller the statistical deviation. Since accelerated EM tests are usually performed at elevated temperatures with higher current densities, extrapolations are necessary to assess the reliability at the service condition. The following equation is used for this purpose:

$$TTF_s = MTTF_t\left(\frac{j_t}{j_s}\right)^n \exp\left[\frac{Q}{k_B}\left(\frac{1}{T_s}-\frac{1}{T_t}\right)+NSD\times\sigma\right] \tag{4.2}$$

where NSD is the number of the statistical deviation, and σ is the lognormal standard deviation. The subscripts t and s refer to the EM test and service conditions, respectively. Equation (4.2) indicates that the EM median lifetime and σ obtained at the accelerated test conditions are the key factors in controlling the EM reliability at the service conditions. Therefore, it is critical to choose a proper failure criterion to assess the EM reliability at service conditions. The EM lifetime could be considerably different depending on the failure criterion. In the following discussion, the EM lifetime is defined based on a 10% resistance increase failure criterion, as widely accepted in the industry.

4.4 RESISTANCE TRACE AND VOID EVOLUTION DURING EM DAMAGE FORMATION

The resistance change as a function of current stressing time for the type I structure with the SiCN cap is plotted in Figure 4.5. Downstream tests were performed at 330 ^{o}C with a current density of 1.34 MA/cm^{2}. All samples showed a progressive resistance increase behavior up to 100% resistance increase, and no abrupt resistance increase was observed. This indicates that no early failures occurred during the EM test. The behavior of the resistance trace is closely related to the void formation and evolution during EM degradation. Figure 4.6 shows the typical void growth in the Cu lines at different stages during the EM test. Combined with the in-situ EM experiments [Meyer 2002, Meyer 2006], four stages can be identified for the void growth and evolution process [Hauschildt 2007]:

1) Vacancy accumulation and void nucleation
2) Vacancy diffusion along the interface and grain boundaries and virtual void migration

3) Void growth to a critical size causing a significant resistance increase, i.e., a step-like increase
4) Continued void growth causing further resistance increase and EM failure

Initially, voids nucleate at flux divergence sites which reside either at the cathode end of the line or at the interface/grain boundary triple junctions where an unbalanced mass flux exists, as shown in Figure 4.6(a). The void starts at the top interface, indicating that the Cu/SiCN cap interface is the dominant diffusion pathway for mass transport. Since the void size is very small at this stage, it is not electrically detectable. Therefore, the resistance remains constant, corresponding to stage "1" as displayed in the resistance trace in Figure 4.2.

At the second stage, voids can evolve in different ways, as shown in Figures 4.6(b) and 4.6(c). They can virtually migrate along the fast diffusion pathways such as the Cu/SiCN cap interface and Cu grain boundaries. The void close to the cathode via grows larger, while the void that is away from the cathode via is filled up by the atoms which migrate from the upstream. Voids can also get trapped at nucleation sites and grow larger there without migration. The way a void evolves is closely related to the interface diffusivity and neighboring Cu microstructures. Since the void only partially occupies the Cu line cross section at this stage, the electron current can still flow through the line, barely changing the line resistance. This is illustrated as stage "2" in the resistance trace in Figure 4.5.

At the third stage, the void grows larger until it spans the entire cross section of the line, forcing the electron current to go through the resistive Ta barrier. At this point, the void is located either at the cathode via corner or away from the via, depending on the site of void nucleation and growth at the earlier stages, as depicted in Figures 4.6(d-e). A step occurs in the resistance trace. The height of the step is directly related to the Ta barrier property such as the resistivity, the thickness, and the critical void size. Accordingly, the resistance increase can be expressed as [Hu 2006, Doyen 2008]:

$$\Delta R = R_b = \rho_b l_v / A_b \tag{4.3}$$

where R_b is the resistance of the exposed barrier layer at void locations, ρ_b is the effective resistivity of the Ta-based barrier, l_v is the void length, and A_b is the cross-sectional area of the barrier including both the trench sidewall and the trench bottom.

The last stage of void growth is depicted in Figures 4.6(f-g). Due to the redundant Ta barrier that allows the current to flow at void locations, the void can continue to grow, leading to a larger resistance increase without inducing open failure. The slope of the resistance increase at this stage is directly related to the Cu drift velocity under EM [Doyen 2008], [Lin 2010]. Interestingly, two different resistance behaviors are observed in Figure 4.5. One is the linear, stable resistance increase; the other is the step-like, unstable resistance increase. The different resistance increase behavior can be attributed to the different Cu atom migration mechanisms, either through edge displacement or grain thinning [Hu 2006], which will be discussed in detail in the following section.

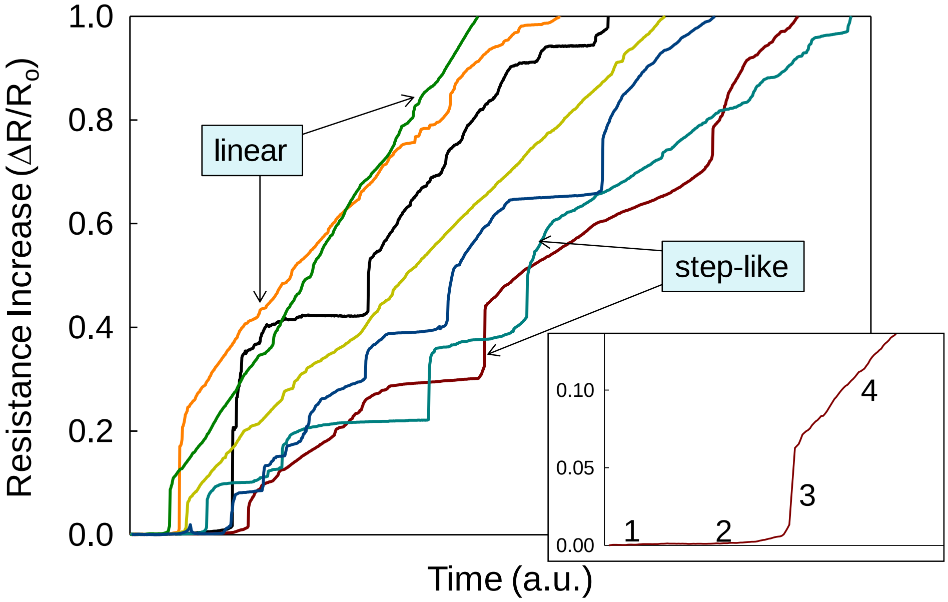
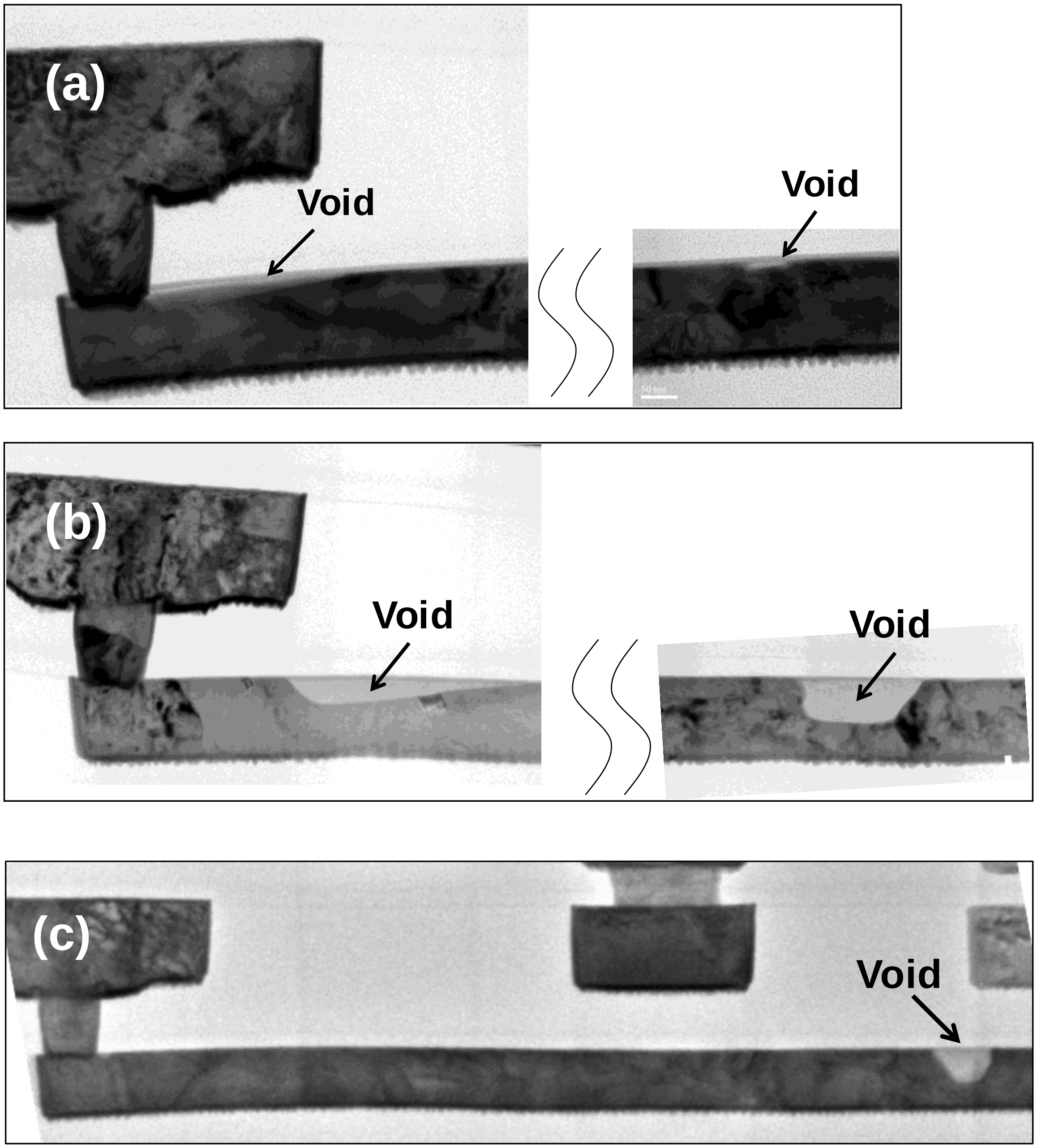


Figure 4.5 Normalized resistance change as a function of time for EM test samples. The inset shows the positions corresponding to the four different stages of void evolution.


(a)
Void
Void
50 nm
(b)
Void
Void
(c)
Void

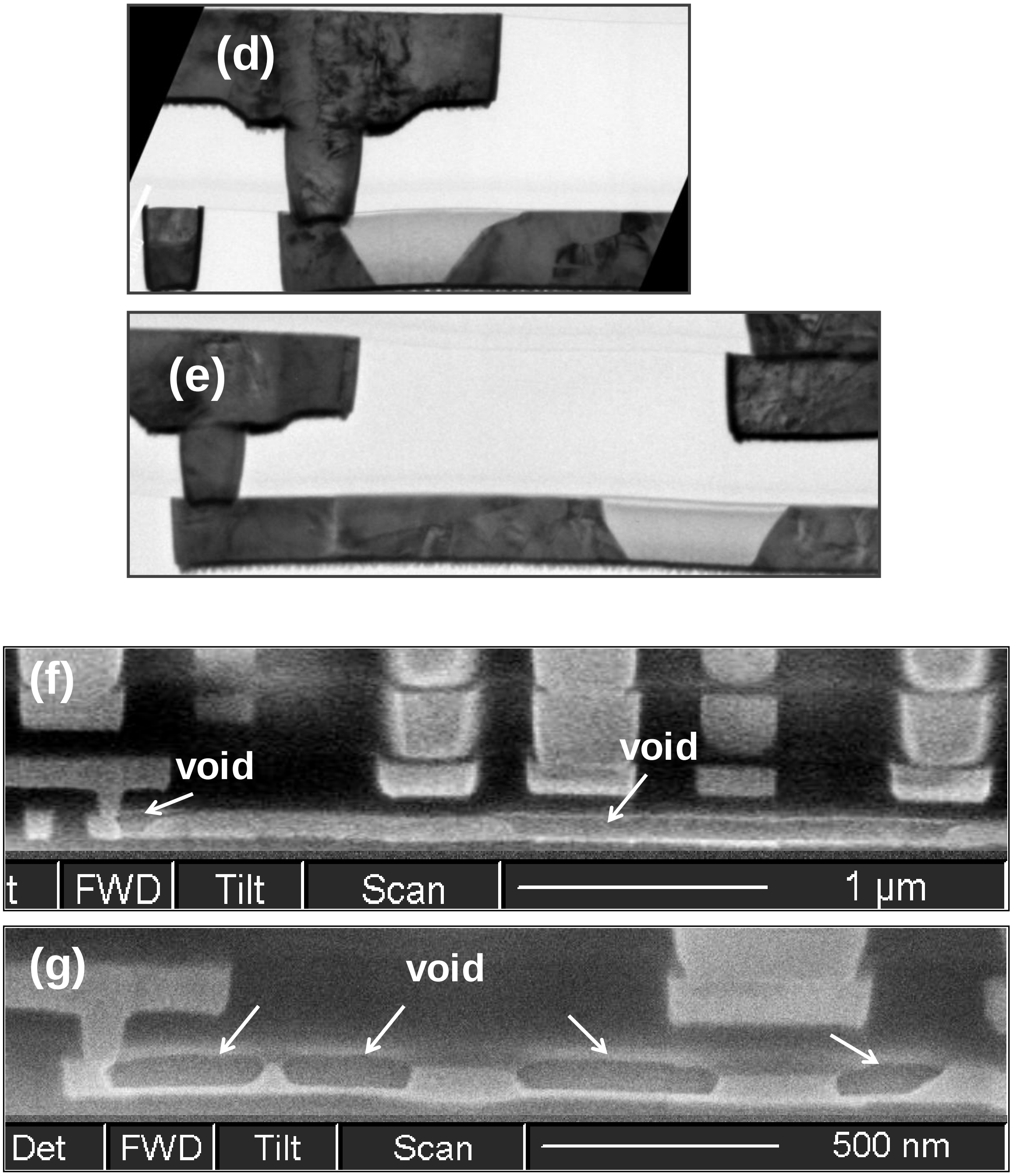


Figure 4.6 TEM and SEM images showing different stages of void growth and evolution. (a) Stage 1: vacancy accumulation, (b-c) stage 2: void evolution and growth, (d-e) stage 3: void growth to the critical size with the first step-like resistance increase, (f-g) stage 4: further void growth.

To further illustrate the different Cu atom migration processes, Figure 4.7 shows the schematic diagrams of two different voiding mechanisms: edge displacement and grain thinning. Edge displacement void growth occurs when the Cu atoms that migrate along the top surface of the Cu line are replaced by Cu atoms that diffuse from the bottom of the line. This effectively causes the void boundary to move in the direction of the electron flow, which accompanies a linear resistance increase. In contrast, for void formation due to grain thinning, the Cu atoms that diffuse along the cap interface are replenished by Cu atoms from grain thinning directly upstream. For this process, the void grows perpendicular to the current flow direction, where the line resistance is not affected, corresponding to the plateau in the resistance trace. Once one grain is completely depleted, a step in the resistance trace occurs. Multiple steps in the resistance trace can be attributed to multiple grain depletions, as shown in Figure 4.6(f) and Figure (4.7).

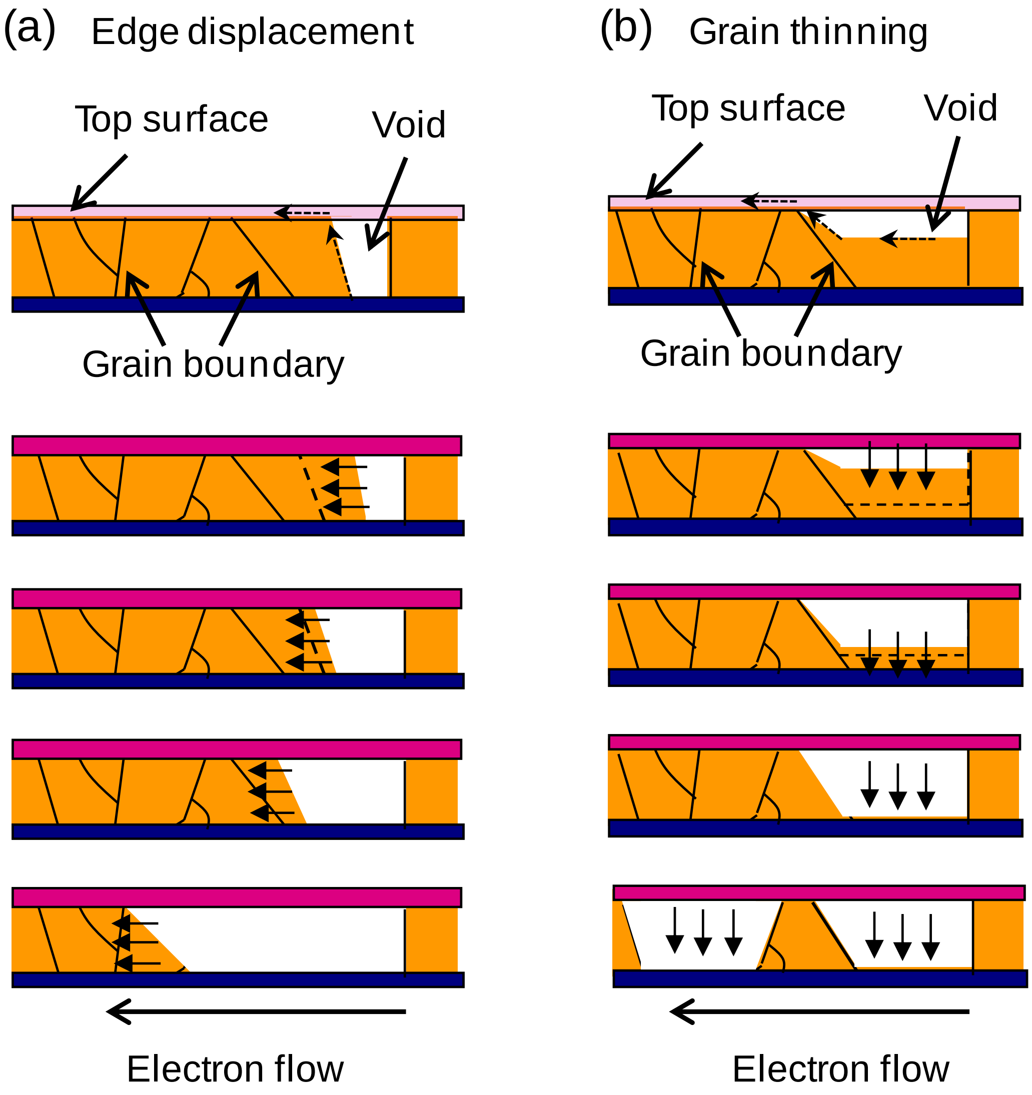


Figure 4.7 Schematic diagrams illustrating different void growth mechanisms including Cu atom migration and void growth direction for (a) edge displacement and (b) grain thinning.

4.5 CAP LAYER AND GRAIN STRUCTURE EFFECTS

4.5.1 Microstructure and Cap layer Characterization

Downstream EM tests were performed on the type II structures to investigate the cap layer and grain structure effects on the EM lifetime and statistics. The Cu microstructure and cap layer interface were first evaluated for the four sets of structures. Figure 4.8 shows the longitudinal TEM images of the M2 line with large grain (LG) and small grain (SG) structures, and the results of grain size analysis are summarized in Table 4.1. The results clearly demonstrate the difference in these two types of grain structures. The LG structure reveals a larger average grain size at the trench top (~215 nm) than at the trench bottom (~181 nm), indicating more small grain agglomerations at the trench bottom in the Cu lines. However, for the SG structure, the average grain sizes at the trench top (~123 nm) and trench bottom (~126 nm) are comparable, and both are smaller than those of the LG structure. Therefore, compared with the LG structure, the SG structure demonstrates more grain boundaries, which could affect the EM performance as discussed in the following section.

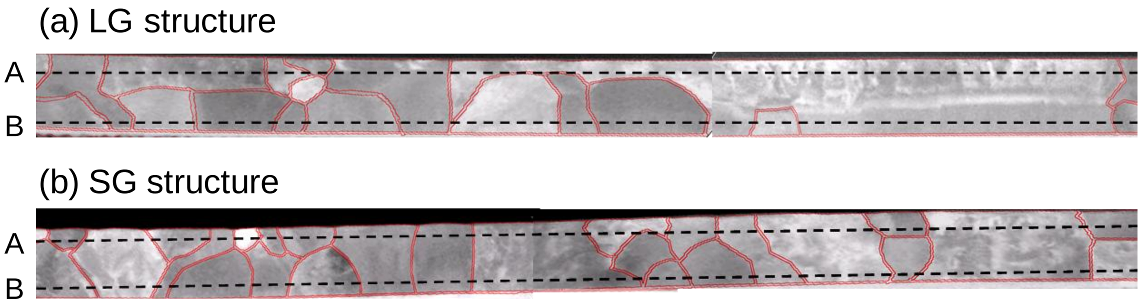


Figure 4.8 Longitudinal TEM images of Cu interconnects with two different grain sizes: (a) LG structure and (b) SG structure. The grain boundaries are marked in red.

Table 4.1 Average grain sizes for large and small grain structures along the lines A and B in Figure 4.8. The grain size is measured by averaging along the dashed line, which extends over a length of ~15 μm.

Grain Structure	**Average Grain Size Along Line A (nm)**	**Average Grain Size Along Line B (nm)**
Large Grain	215	181
Small Grain	123	126

Figures 4.9(a-b) shows the cross-sectional TEM images of the M2 trench with the SiCN cap and the CoWP cap, respectively. It can be seen that Cu is surrounded by a thick Ta-based liner at the sidewalls and the trench bottom with a thickness of around 10 nm. A SiCN cap layer (~ 30 nm thick) encapsulates the M2 trench on the top for both structures except that there is an additional CoWP coating for the CoWP capped structure. The thickness of the CoWP coating is not easily discernible from the TEM image. Therefore, an EDX line scan was performed across the Cu/CoWP/SiCN interface starting from point A in the Cu trench to point B in the SiCN layer, as shown in Figure 4.10. The Co signal in the EDX line profile indicates that the CoWP cap is approximately 6 nm thick.

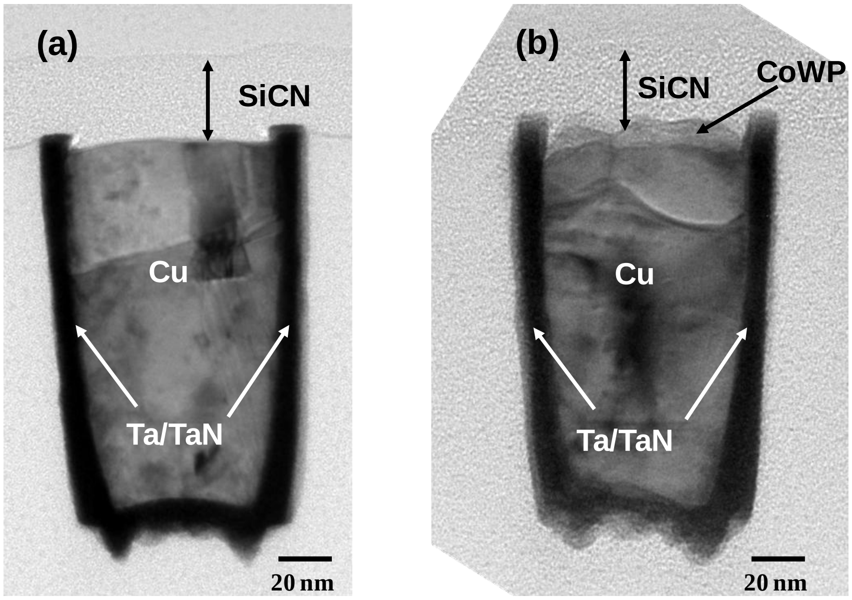


Figure 4.9 Cross-sectional TEM images of the M2 Cu trench for (a) SiCN cap and (b) CoWP cap.

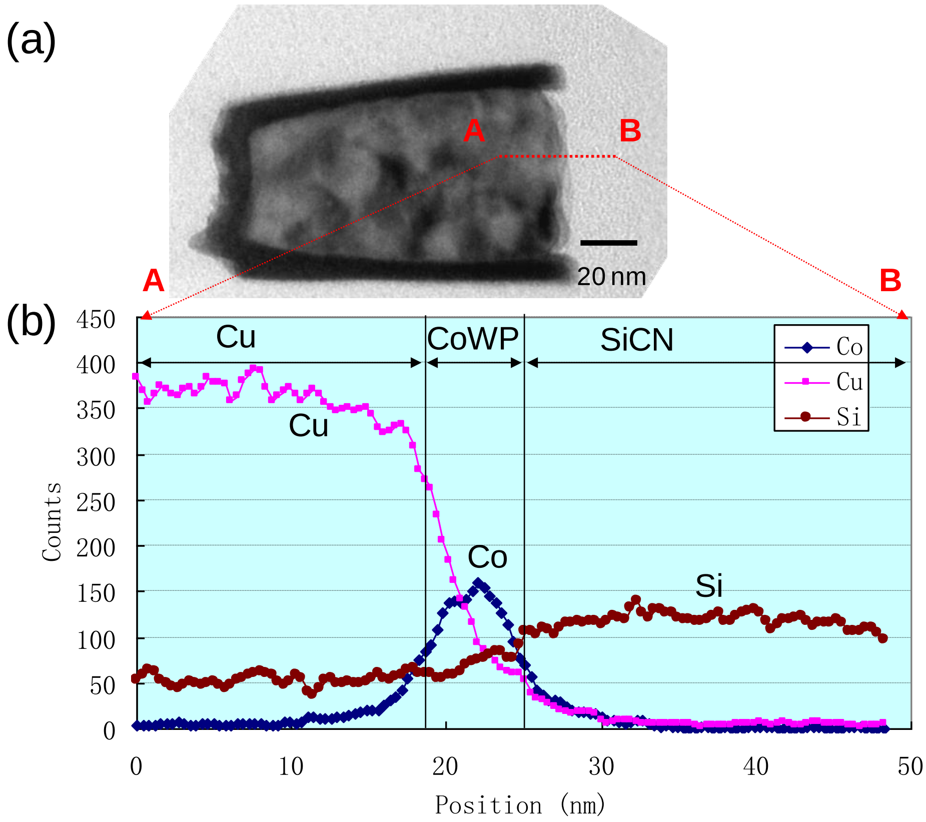


Figure 4.10 (a) Cross-sectional TEM image of CoWP capped sample. (b) EDX line profile scanned from point A to point B as indicated in (a).

High resolution TEM analysis was performed to evaluate the interface quality for both structures. Figure 4.11 shows that the Cu line has a sharp and smooth interface with the SiCN cap, for which no distinct crystalline features are identified. In contrast, almost perfect crystalline planes of Cu extend all the way through the CoWP metal cap with no distinguishable interface in between. In addition, the CoWP cap shows a blurred interface with the SiCN layer with observable morphology variation.

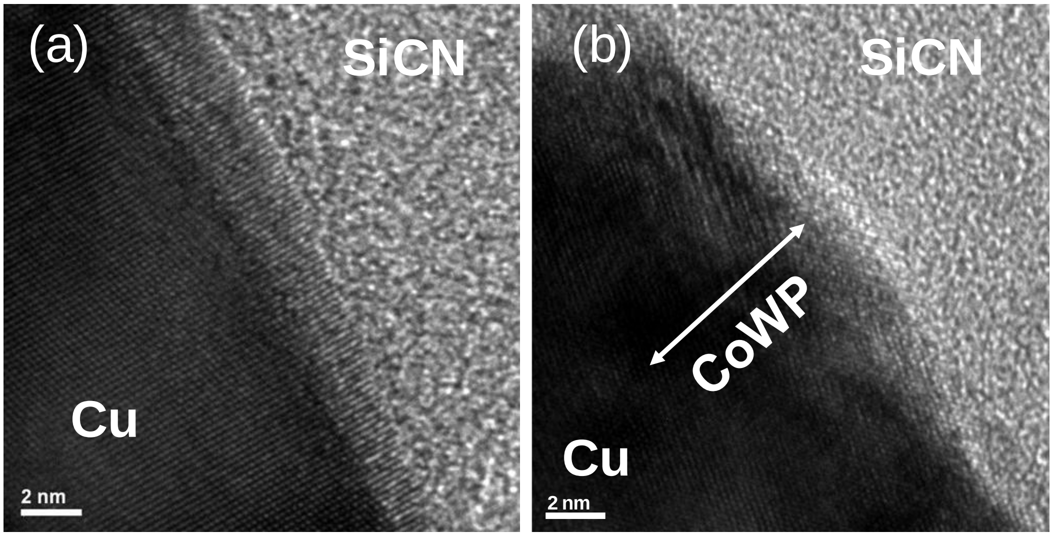


Figure 4.11 High resolution TEM images of different Cu/cap interfaces: (a) SiCN cap and (b) CoWP cap.

4.5.2 EM Lifetime and Statistics

Figure 4.12 plots the EM lifetime distribution of the four sets of test structures with the type II configuration. The EM tests were performed at 330 ^{o}C with a current density of 1.03 MA/cm^{2}. Regarding the EM tests of the CoWP capped structures with large grains, extremely long test time was employed with only four samples failed according to the 10% resistance increase failure criterion. Other test samples were intact or showed a resistance increase of less than 10% when the test was terminated. The cap layer and grain size effects are clearly identified from the EM lifetime data.

First, compared to the SiCN cap, the CoWP capped structures show a significantly improved EM lifetime. For the LG and SG structures, the improvement is >100x and ~24x, respectively. Such improvement in the EM lifetime for the CoWP cap can be attributed to a reduction in diffusion along the Cu/cap interface, which could result from the highly ordered crystalline interface between Cu and CoWP and the higher bond strength between Cu to Co over that of Cu to amorphous SiCN [Lane 2003a, Lane 2003b]. The difference in the interface crystalline quality has already been shown in Figure 4.11, where the Cu/CoWP interface was characterized by highly ordered crystalline structures with evidently good bond strength to suppress the interface diffusion. This result is in good agreement with a previous study reporting a highly disordered Cu/SiCN interface vs. a highly ordered and metallic bonding Cu/Co interface [Zschech 2005a]. The EM lifetime improvement for the CoWP cap is consistent with the results reported previously [Hu 2002b, Gambino 2006, Aubel 2008], indicating that interface modification with a CoWP cap is an effective method to improve the EM reliability of Cu interconnects.

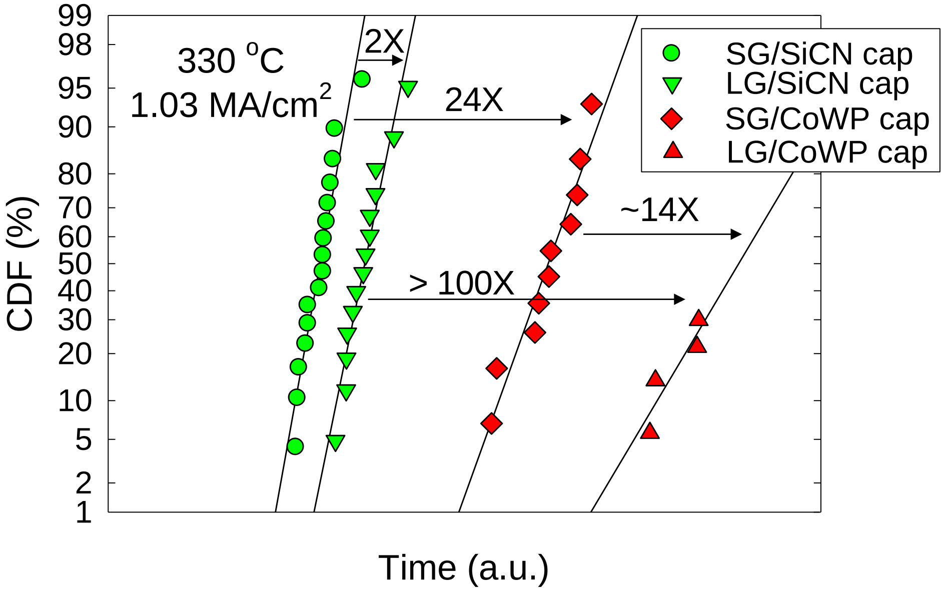


Figure 4.12 CDF plots of the four sets of Cu interconnects with the type II structure: LG/SG structures with SiCN/CoWP caps. EM tests were performed at 330 °C, with a current density of 1.03 MA/cm^2.

Moreover, the grain size effect on the EM lifetime is also clearly demonstrated for both caps. For the SiCN cap, the EM lifetime degrades by half when changing from LG to SG structure. This effect becomes more significant for the CoWP cap, for which, the EM lifetime of the SG structure degrades to about one fifth of the LG structure. For each cap, since the cap layer deposition processes for the large and small grain structures are identical, we can assume that the mass transport along their respective cap interfaces is the same. The EM lifetime degradation of the SG structure is then attributed to the additional grain boundary contributions to mass transport. Previously, Hau-Riege *et al.* [Hau-Riege 2001] reported that for a very weak Cu/cap interface, Cu microstructure did not affect the EM performance significantly. Thus, Cu lines with bamboo-like and polycrystalline structures showed a similar EM lifetime. However, when the cap interface was improved by process optimization, the Cu microstructure was found to start to affect the EM lifetime [Hu 2007]. Furthermore, when the cap interface is strengthened by the CoWP cap, the interface diffusion is markedly suppressed so that it contributes little to the mass transport. The significant lifetime degradation observed for the small grain structures with the CoWP cap observed in this study indicates that the atomic diffusion along grain boundaries becomes more important in contributing to the overall mass transport when the interface diffusion is effectively suppressed.

In addition to the EM lifetime, it is important to point out that the lifetime statistics is also influenced by the cap layer and grain size. Table 4.2 summarizes the EM statistical deviations for the four sets of structures. It is clear that the CoWP capped structures demonstrate a considerably larger statistical deviation compared with the SiCN capped structures. For the SiCN cap, the statistical deviation is almost the same for LG ($\sigma = 0.30$) and SG ($\sigma = 0.27$) structures. However, for the CoWP cap, the LG structures show a σ of 0.88, considerably larger than the σ of 0.53 for the SG structure. The results indicate that the CoWP capping inherently induces a larger statistical deviation in the EM lifetime even with a controlled fabrication process and the larger the grains, the larger the σ. The origins of this difference in the lifetime statistics are likely due to the effect of grain structure on the statistical distribution of flux divergence sites for void formation. The details will be further analyzed in the following chapter.

Table 4.2 EM lifetime statistics for the four sets of test structures: SiCN/CoWP cap with LG/SG structures.

	SiCN/SG	**SiCN/LG**	**CoWP/SG**	**CoWP/LG**
Sigma	0.27	0.30	0.53	0.88

4.5.3 Failure Mode and Resistance Trace Analysis

To better understand the effects of cap layer and grain structure, the EM damage formation were investigated further by combining the post-mortem physical failure analysis and the resistance trace analysis. Figures 4.13 and 4.14 show the resistance traces and the failure analysis of selected SiCN capped samples with LG and SG structures, respectively. Two failure modes were observed as manifested by different initial resistance steps. The mode I failure shows a small initial resistance increase followed by a gradual resistance climb. TEM and SEM images indicate that the mode I failure was due to void formation located at the cathode via corner. This often resulted from a small critical void size during EM failure, leading to a small initial resistance step. In comparison, the mode II failure demonstrates a larger initial resistance jump, reflecting a larger critical void size to induce the EM failure. This mode is mostly due to void formation by mass depletion of individual grains in the M2 trench located several microns away from the cathode via, as presented in the TEM images in Figures 4.13 and 4.14. In addition, the mode II failure demonstrates a longer EM lifetime as compared to the mode I failure.

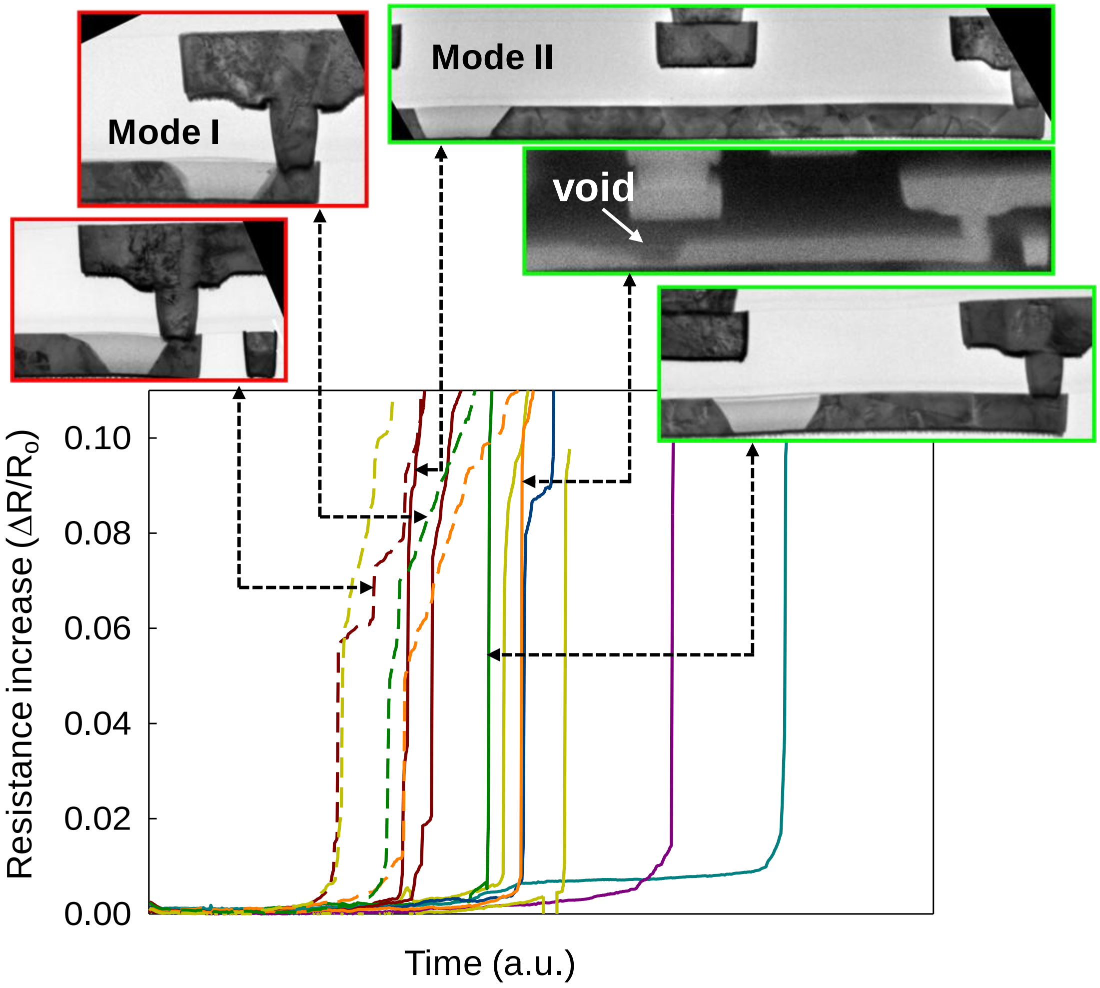


Figure 4.13 Normalized resistance change as a function of time for SiCN capped samples with the LG structure. Two failure modes are observed. The dashed lines represent mode I failures and the solid lines represent mode II failures.

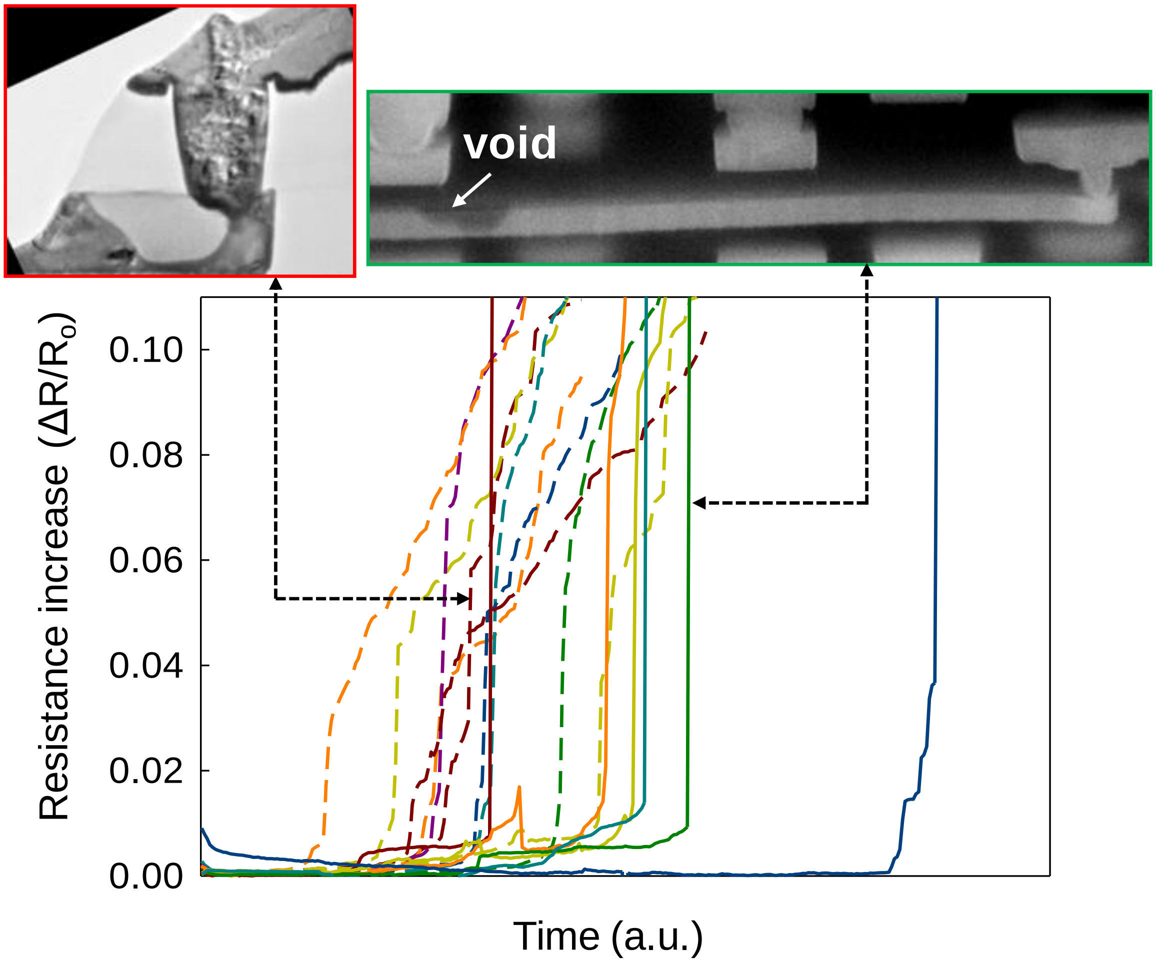


Figure 4.14 Normalized resistance change as a function of time for SiCN capped samples with the SG structure. Two failure modes are observed. The dashed lines represent mode I failures and the solid lines represent mode II failures.

The resistance traces and the SEM analysis of the CoWP capped samples are shown in Figures 4.15 and 4.16 for LG and SG structures, respectively. Different from the SiCN cap, the EM failures of the CoWP capped samples are predominately mode II failures with void formation in the trench with a certain distance away from the cathode via.

For the SiCN capped structures, a direct correlation exists between the initial resistance step (R_{step}) and the void location: a small initial R_{step} for void formation at the cathode via corner (mode I) and a large initial R_{step} for void formation in the trench away from the via (mode II). According to Equation (4.3), the amount of resistance increase is directly proportional to the void size. By comparing the resistance increases and the void sizes identified by the physical failure analysis, a correlation between the resistance increase and the void length l_v can be established. Thus, the critical void length, which is directly related to R_{step}, can be calculated. It is found that the critical void length of the mode I failure is approximately 63 nm, while that of the mode II failure is about 146 nm. The different critical void length can be attributed to the difference in the void location and the electron current flow direction. Figure 4.17 illustrates the schematic representation of the two voiding modes. For the mode I failure where the void forms at the cathode via, the electron flow has two components at the via corner: perpendicular and parallel to the line direction, as shown in Figure 4.17(a). The vertical electron flow pushes the Cu atoms to migrate towards the trench bottom, especially when a grain boundary is present. This effect can cause a fast vertical Cu atom migration. The void can grow across the line thickness direction, resulting in a relatively small critical void length and a small initial R_{step}. In comparison, for the mode II failure, the current flow is primarily parallel to the line direction. Cu atoms are depleted by diffusion along the inner void surface. The void tends to start with an initial slit shape and eventually grows to a large critical size. This will require a longer time to deplete the larger amount of Cu for the void to span over the entire height of the line.

For the CoWP cap, however, there seems to be no direct correlation between the void location and R_{step}. Instead, a small R_{step} is present in most test samples, irrespective of the failure modes. This is likely due to the fact that the strong Cu/cap interface bonding significantly reduces the interface diffusion in CoWP capped structures. Since the Cu/cap interface diffusivity is much lower than that at grain boundaries and inner void surfaces, once a void is formed in the trench, it grows primarily as a relatively narrow slit with a small critical void size. Details of void formation and evolution characteristics for CoWP capped samples need further investigations.

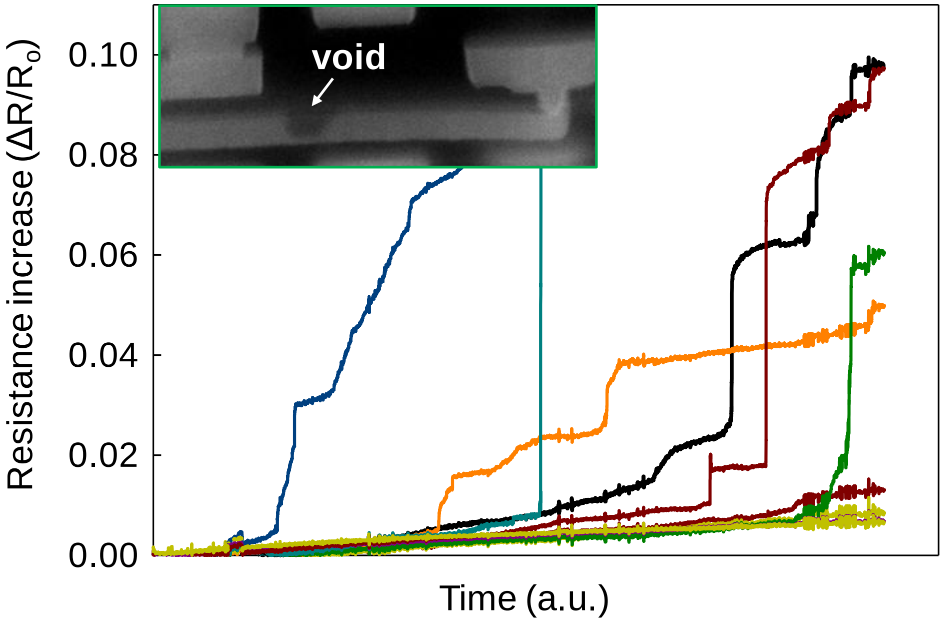


Figure 4.15 Normalized resistance change as a function of time for CoWP capped samples with the LG structure. Only mode II failures are observed.

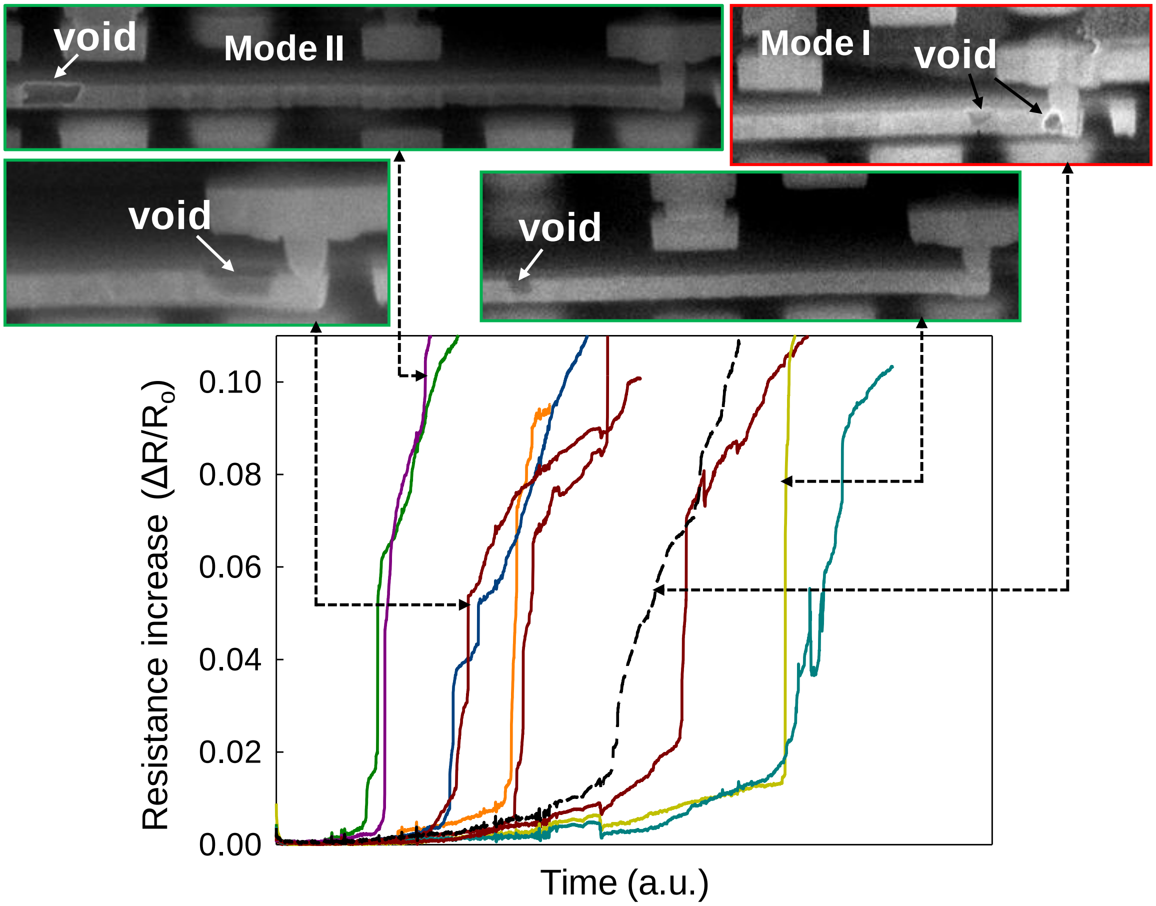


Figure 4.16 Normalized resistance change as a function of time for CoWP capped samples with the SG structure. Two failure modes are observed. The dashed lines represent mode I failures and the solid lines represent mode II failures.

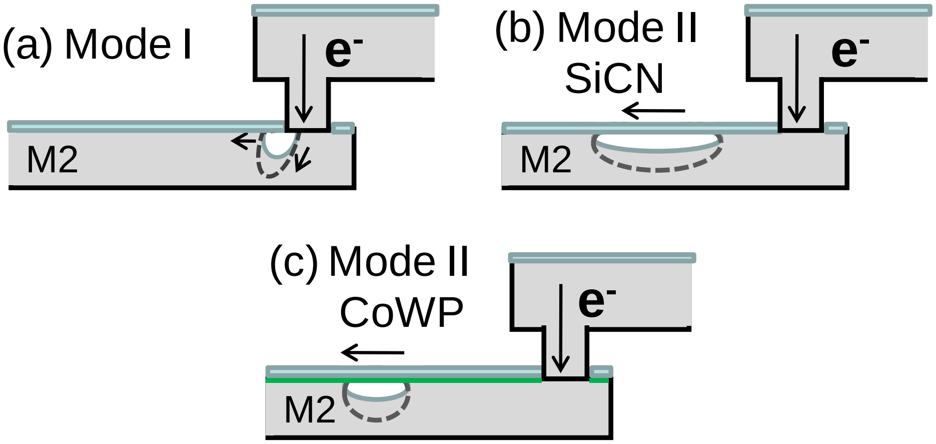


Figure 4.17 Schematic diagrams illustrating the void growth for (a) mode I failures for SiCN cap, (b) mode II failures for SiCN cap, and (c) mode II failures for CoWP cap.

The overall void formation process is dynamic in nature depending on the location of void nucleation and the void evolution process during EM. These parameters can be traced to the characteristics of the flux divergence sites where vacancy can agglomerate and the effective diffusivity that controls the void migration rate. During EM, Cu atoms diffuse along the electron flow direction driven by the momentum transfer due to scattering by the electrons. Voids form at flux divergence sites where an unbalanced Cu flow rate exists, i.e., Cu atoms that come from the cathode end of the sites are fewer than those that diffuse away from the sites. For downstream EM, flux divergence sites tend to reside at the cathode via corner where the Ta barrier at the via bottom blocks the Cu atoms in the via from diffusing down to the trench line. Flux divergence sites can also occur at interface/grain boundary intersections due to either interface quality or the grain texture-induced interface diffusivity variations [Sukharev 2007]. After voids nucleate at these flux divergence sites, they will evolve with continuing current stressing in different ways. In some cases, they are filled with the Cu atoms migrated from the upstream and the voids virtually migrate along the line towards the cathode end. In other cases, voids get trapped at the nucleation sites where they grow until failure occurs. This process of void evolution and growth is affected significantly by the cap interface adhesion strength and Cu grain structures [Sukharev 2007, Meyer 2007, Meyer 2002, Zschech 2009].

The failure modes of the four sets of structures are further correlated to their EM lifetimes, as summarized in Figure 4.18. The EM lifetime increases from SiCN/SG, SiCN/LG to CoWP/SG, and CoWP/LG structures, corresponding to a combination of cap layer and grain structure changing from the weakest case to the strongest case in terms of the resistance to EM. This is accompanied with a decrease in the proportion of mode I failure and an increase of mode II failure. The latter trend can be understood by considering the effective diffusivity difference emanating from cap interface and grain boundary. For the SiCN cap, the cap interface diffusivity is large. Voids move readily along the interface and eventually accumulate at the cathode via corner to fail the line. For the CoWP cap with suppressed interface diffusion and enhanced interface bonding, the energy barrier for a void to de-pin from the nucleation site is much higher than for the SiCN cap. Consequently, once a void nucleates at the intersection of interface and grain boundaries, it is likely to get trapped there and grow further, leading to mode II failures. Similarly, compared with the SG structure, the LG structure reduces the grain boundary mass transport and the effective diffusivity for void diffusion. This leads to void formation at local grains due to mass depletion and consequently makes the Cu lines more prone to mode II failures. These two factors together: cap material and Cu grain size, shift the failure mode from mode I to mode II, yielding a superior EM performance for the CoWP capped LG structure.

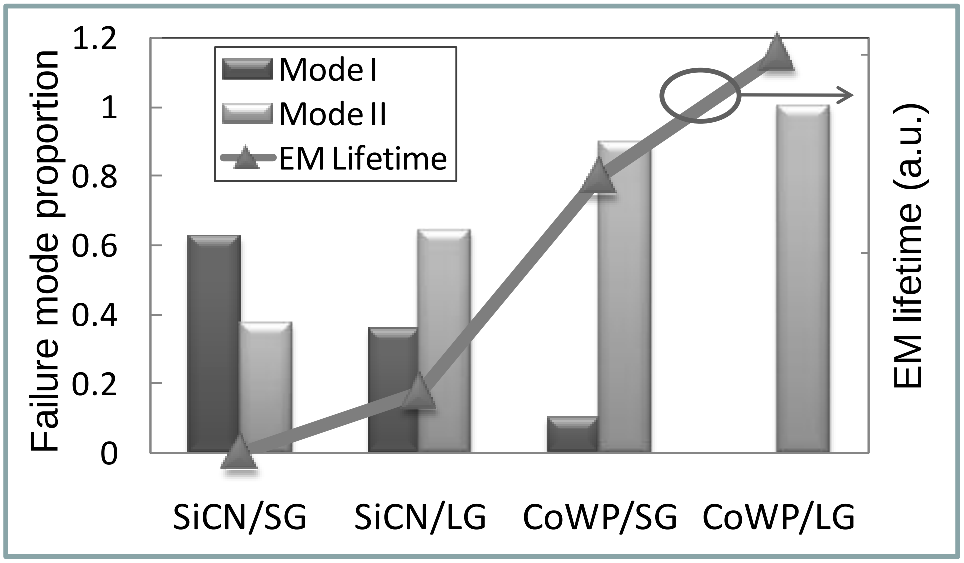


Figure 4.18 Comparison of failure mode proportion and relative EM lifetime for M2 Cu interconnects with different cap layers and grain sizes.

4.5.4 Activation Energy

To further clarify the EM failure mechanism, the activation energies of different structures were investigated. The EM median lifetimes are plotted in Figure 4.19 as a function of 1/*T* for SiCN capped structures with large and small grains. The test temperatures employed were 270 ^{o}C, 300 ^{o}C and 330 ^{o}C and the current density remained constant at 1.03 MA/cm^2. The EM data revealed that, under all test conditions, the EM lifetimes of the SG structures were shorter than those of the LG structures. The activation energies for the SG and LG structures extracted based on Black's equation were found to be 0.96 ± 0.07 eV and 0.90 ± 0.05 eV, respectively. The results are in good agreement with the reported values of 0.8-1.1 eV [Hu 1999, Fischer 2002a, Hu 2002a, Bradshaw 1964, Croes 2009] for the Cu/SiN$_x$ cap interface diffusion and 0.8-1.2 eV [Gupta 1988, Surholt 1997, Gupta 1997, Croes 2009] for the grain boundary diffusion.

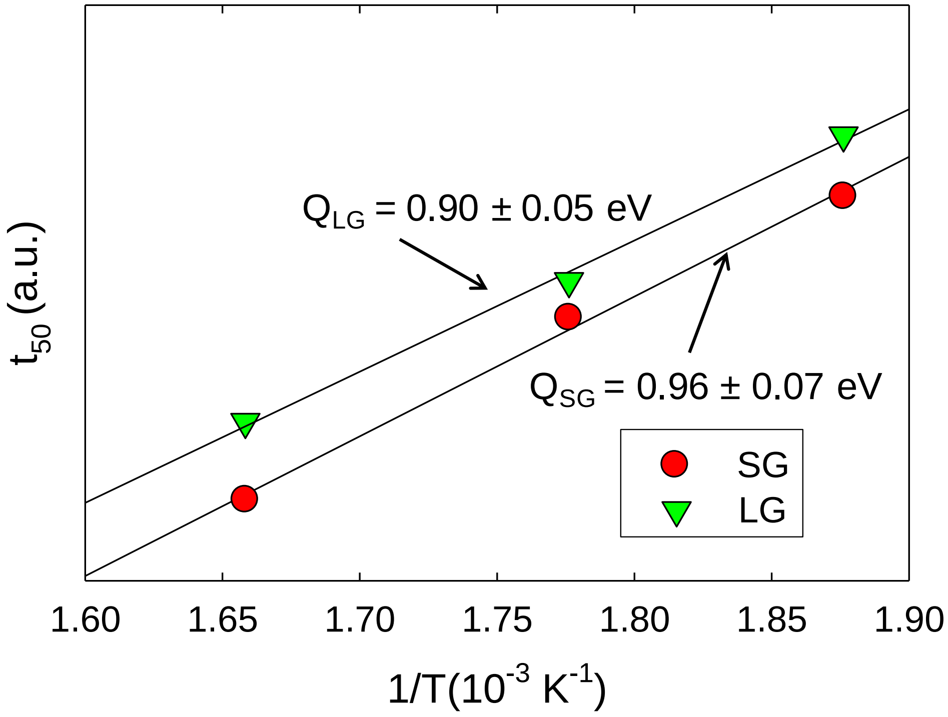


Figure 4.19 Plot of the EM median lifetime as a function of 1/*T* for SiCN capped structures with large and small grains.

The activation energies for CoWP capped structures were not measured in this study due to the limited availability of test samples and extremely long test time required. However, it has been reported that the activation energy for damascene Cu interconnects with a CoWP cap is much larger than that for the SiCN cap, ranging from 1.32 eV to 2.0 eV [Hu 2006, Aubel 2008, Gambino 2006, Hu 2003b], depending on the specific process applied. The activation energy for the CoWP capped structures in this study is expected to be in the same range, and the value for the SG structures should be smaller than that for the LG structures, taking into account the additional grain boundary diffusion contribution to mass transport in the SG structures.

4.5.5 EM Lifetime Scaling

As the technology scaling continues, it is important to study the EM lifetime scaling and the impact of cap material and grain structure. In this section, the EM lifetime scaling is investigated taking into account the contributions from both cap interfaces and grain boundaries. During EM, the mass transport driven by the EM driving force $F_e = Z_{eff}^{*} e\rho j$ can be written as:

$$v_d = \left(\frac{D_{eff}}{k_B T}\right) F_e = \left(\frac{D_{eff}}{k_B T}\right) Z_{eff}^{*} e\rho j \tag{4.4}$$

where v_d is the drift velocity, D_{eff} is the effective diffusivity, $Z_{eff}^{*} e$ is the effective charge, ρ is the metal resistivity, j is the applied current density, k_B is the Boltzmann constant and T is the absolute temperature. Two parameters in Equation (4.4) determine the drift velocity of metal ions and in turn the EM lifetime. The first is the current density j which continues to increase as specified by the ITRS [http://www.itrs.net/]. The second is the effective diffusivity D_{eff} of moving ions through various diffusion paths. In Cu damascene interconnects, there are two dominant diffusion paths: Cu/cap interface and Cu grain boundary. Accordingly, the effective diffusivity can be expressed as:

$$Z_{eff}^{*}D_{eff} = \frac{Z_{N}^{*}D_{N}\delta_{N}}{h} + \frac{Z_{GB}^{*}D_{GB}\delta_{GB}}{d}f \tag{4.5}$$

where δ_i is the effective width and D_i is the diffusivity of the metal ions. The subscripts N and GB refer to the Cu/cap interface and the Cu grain boundary, respectively. The factor h is the line thickness, d is the average grain size and f is the geometrical factor defined by the average orientation of the grain boundaries relative to the current flow.

For simplicity, the single damascene Cu interconnects are considered with the void forming at the cathode end of the line to fail the interconnect. The EM lifetime τ can be expressed as:

$$\tau = \frac{\Delta L_{cr}}{v_d} = \frac{\Delta L_{cr}k_BT}{e\rho j(Z_{N}^{*}D_{N}\delta_{N}/h + fZ_{GB}^{*}D_{GB}\delta_{GB}/d)} = \frac{\Delta L_{cr}k_BT}{e\rho jZ_{N}^{*}D_{N}\delta_{N}(1+fgh/d)} \tag{4.6}$$

where ΔL_{cr} is the critical void length to cause the failure, which is approximately the via size or line width w. The g factor is defined as the ratio of the mass transport through the grain boundary vs. the cap interface and can be expressed as:

$$g = Z_{GB}^{*}D_{GB}\delta_{GB} / Z_{N}^{*}D_{N}\delta_{N} \tag{4.7}$$

Equation (4.6) is written in a format to facilitate the discussion of cap layer and grain structure effects on EM lifetime. According to Equation (4.6), the ratio of the median lifetime for each technology node relative to that of the 0.13 μm technology is plotted in Figure 4.20 as a function of the critical void volume $\Delta L_{cr}h$ (or cross-sectional area wh). Both grain boundary and interfacial diffusion contributions to mass transport are included here. The data points with open circular symbols are experimental data based on this study and provided by GLOBALFOUNDRIES.

For standard SiCN capped Cu interconnects with bamboo or near-bamboo grain structures, the f term approaches to zero and can be neglected, thus the EM mass transport is dominated by the Cu/SiCN interface diffusion. For each new technology generation, if the current density j is assumed to remain the same, the EM lifetime degrades by half due to the scaling of the geometrical factor $\Delta L_{cr}h$ (wh), as shown by the reference line "1" in Figure 4.20. However, when the CoWP metal cap is applied to the Cu interconnects, the atomic diffusion along the interface is effectively suppressed; the D_N term varies depending on the metal cap process. The scaling curve will shift up significantly as shown in Figure 4.20, where a 40x lifetime improvement is assumed just for illustration.

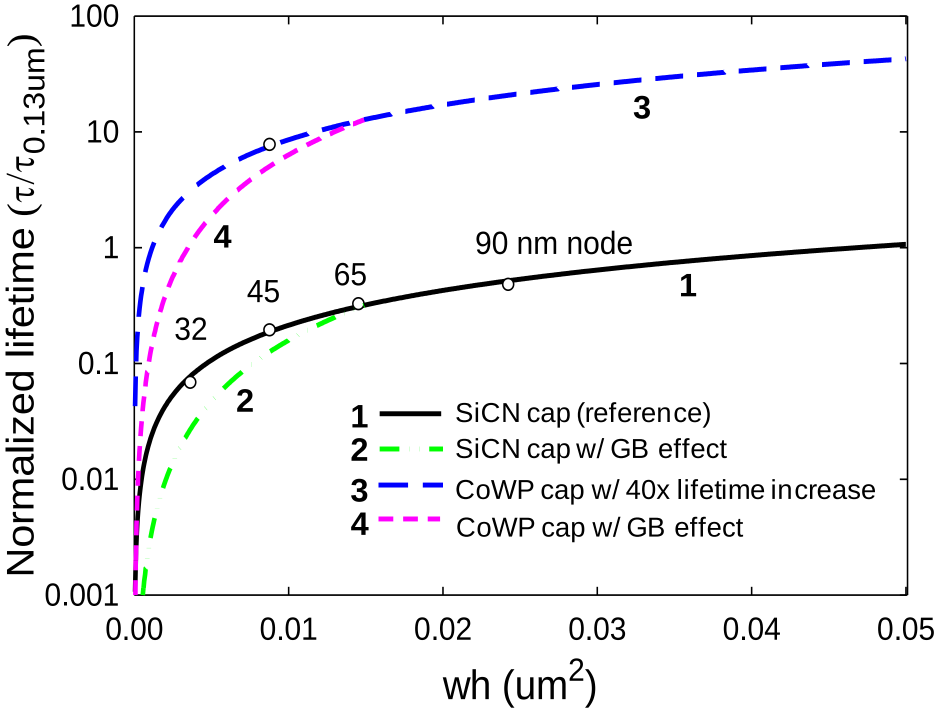


Figure 4.20 Normalized EM median lifetime vs. *wh* (cross-sectional area) for various Cu interconnect generations considering both cap interface and grain boundary contributions. The open circles represent the experimental data.

As scaling continues, more small grains emerge in the Cu lines beyond the 65 nm node, and a higher proportion of grain boundaries are aligned with the current flow. This will result in a larger *f* and a smaller *d* value, thus the *fgh*/*d* term will increase. Therefore, grain boundary diffusion will become increasingly important, which will accelerate the mass transport and the EM degradation, as illustrated by the green dashed line labeled by "2" in Figure 4.20. Due to the lack of comprehensive experimental data regarding the effect of scaling-induced grain structure degradation on the *f* and *g* factors, here the curve "2" was plotted by assuming a scaling factor directly related to the Cu line cross-sectional area *wh* starting at the 65 nm node. Such EM lifetime degradation due to the presence of small grains can be more significant for the CoWP cap, as observed in this study. This is due to the fact that, with the suppression of interfacial diffusion by the CoWP cap, grain boundary diffusion becomes more dominant. Therefore, a small change in the grain structure can result in a large change in the overall Cu diffusivity and in turn the EM lifetime. In addition, for the CoWP cap, the EM lifetime statistics is closely related to the grain structure, which is illustrated in the scaling curve and will be further addressed in Chapter 5.

4.6 SUMMARY

In this chapter, the effect of failure criteria on EM lifetime, statistics and activation energy for Cu interconnects was firstly studied, and the correlation between the void formation/evolution and the resistance traces was investigated. It was demonstrated that the EM lifetime increases and the statistical deviation decreases as the failure criterion changes from 5%, 10%, 50%, to 100% resistance increase. The 10% resistance increase was selected as the failure criterion in the following study. A 4-stage void formation and evolution process was established by correlating the features in the resistance trace with the physical failure analysis images.

Then the effects of cap layer and grain structure on EM reliability were investigated by performing downstream EM tests on four sets of Cu interconnects: large/small grain structures with SiCN/CoWP caps. The CoWP cap was found to significantly improve the EM lifetime compared to the SiCN cap. In addition, LG structure showed a longer EM lifetime than the SG structure, particularly for the CoWP cap.

Compared with the SiCN cap, the CoWP cap was found to improve the EM lifetime by ~25 times for the SG structure and >100 times for the LG structure. For the SiCN cap, the LG structure was observed to improve the EM lifetime by ~2 times compared to the SG structure with no significant effect on the lifetime statistics. However, for the CoWP cap, the grain structure effect was more significant, with a ~14x improvement in the EM lifetime accompanied with an increase in the statistical deviation.

In addition, for SiCN capped structures, two failure modes were identified by distinct resistance traces and void locations. Mode I failures corresponded to a small initial resistance increase with void formed at the cathode via corner, while mode II failures corresponded to a large initial resistance jump with void formed several microns away from the cathode via. Overall, mode II failures corresponded to a longer EM lifetime. However, for CoWP capped structures, voids mostly formed in the trench several microns away from the cathode via, corresponding to mode II failures. The proportion of mode II failures increased from SG to LG structure, from SiCN cap to CoWP cap. This trend in EM damage formation can be understood by considering the void nucleation and evolution process, as well as the effective diffusivity during EM. For the SiCN cap, voids move readily along the Cu/SiCN cap interface and some eventually accumulates at the cathode via corner to cause the failure. On the contrary, for the CoWP cap, the atomic diffusion along the cap interface is significantly suppressed. Consequently, voids cannot move freely along the Cu line and easily get trapped at interface/grain boundary intersections. Similarly, the SG structure provides more grain boundary diffusion paths to facilitate the void formation and agglomeration at the cathode via. Therefore, the stronger interface and the larger grain size will facilitate the void formation in the trench away from the cathode via, leading to superior EM performance.

Based on the experimental results, the effects of cap layer and grain structure on EM lifetime scaling were deduced. The results enable us to predict the scaling trend by considering both the interface and grain boundary contributions to diffusion. It was found that for the current technology node, the application of the CoWP metal cap seems to be able to meet the EM reliability requirements; with further scaling, however, when the grain structure degrades from bamboo-like to more polycrystalline grains, the additional contributions to mass transport from grain boundaries will significantly degrade the EM performance. It becomes increasingly important to investigate the grain structure effect on EM reliability even with the application of the CoWP cap, and simultaneously seek for good solutions to develop Cu lines with bamboo-like microstructures.

Chapter 5: Statistical Analysis of Electromigration Damage of Cu Interconnects with CoWP Capping

5.1 INTRODUCTION

In Chapter 4, the effect of grain structure on EM characteristics was discussed for Cu interconnects with different capping materials. The effect was found to be significant for CoWP capping showing that the EM lifetime for the large grain structure was about 14 times longer than the small grain structure. However, the improvement in EM lifetime came with an increase in the statistical deviation σ increasing from 0.53 for the small grain structure to 0.88 for the large grain structure. It was also demonstrated that the mass transport along the top interface was suppressed effectively by the CoWP capping so that the grain boundary now became the dominant diffusion pathway. While the overall results on CoWP capping are quantitative and consistent with previous studies, the effect of grain structure on EM lifetime and statistics is not well understood. The grain structure effect is potentially significant regarding the application of the CoWP capping for EM improvement of future Cu interconnects. In this chapter, a statistical model will be developed to analyze the grain structure effect on EM damage formation in Cu interconnects with CoWP capping.

The grain structure effect on EM characteristics has been investigated for Al interconnects. In 1970, Agarwala *et al.* [Agarwala 1970] proposed a “structural defect model” to explain the increase of the EM lifetime and standard deviation as the line length decreases. Later on, Cho *et al.* [Cho 1989] proposed a “failure unit model” or “weakest-link model” based on Agarwala’s structural defect model. This model was able to successfully interpret the EM statistics in Al interconnects and received general acceptance. Furthermore, Korhonen *et al.* [Korhonen 1993b] demonstrated a statistical model to analyze the microstructure effect on EM damage of Al interconnects. In this model, the mass transport in Al interconnects under EM comes mainly from diffusion through the lattice and grain boundaries. Void formation is statistical in nature, depending on the distribution of line segments with cluster grains and bamboo grains. When a cluster grain segment is adjacent to a bamboo grain segment, the different mass transport rates in these segments will lead to void formation at the cathode end of the cluster grain or at the anode end of the bamboo grain. The model considers that there are N segments of mixed grain clusters and calculates the flux divergence in these segments arising from the difference in lattice and grain boundary diffusivities. The flux divergent sites are distributed statistically through the line, dependent on the grain structure and the line width. The EM lifetime and its failure statistics are deduced using a statistical model to predict the failure probability in the interconnects.

For the submicron Cu interconnects up to the 90 nm node, the Cu grain structures are near bamboo or bamboo-like. The EM lifetime is usually found to be dominated by the Cu/SiN$_x$ interface diffusion. This is different from the Al interconnects, in which the grain boundary is the fastest diffusion pathway. For the 65 nm technology node and beyond, small grain clusters were reported to mix with large bamboo grains [Hu 2007, Arnaud 2010], which were observed to degrade the EM performance. For Cu interconnects with CoWP capping, the interface diffusion is effectively suppressed and at the same time, small grain clusters emerge, resulting in grain boundary diffusion dominating the mass transport. With these basic changes in the grain structure and diffusion characteristics, Korhonen's microstructure-based model will be extended to analyze the grain structure effect on the EM lifetime and statistics for Cu interconnects with CoWP capping.

In this chapter, the change in the interface diffusion relative to the grain boundary diffusion due to CoWP capping will be estimated first. The reduction in the interface diffusivity demonstrates that the grain boundary diffusion indeed dominates the mass transport and thus justifies the application of the Korhonen's model to analyze the EM characteristics for Cu lines with CoWP capping. This will be followed by deducing the EM lifetime of a single cluster based on the stress evolution in the cluster segment. This provides a basis to establish a correlation between the lifetime distribution and the cluster length distribution. Then, the grain structure of the CoWP capped Cu interconnects is examined by TEM, and the cluster length distribution is extracted from the TEM images. The weakest-link model is applied to calculate the EM lifetime and statistics based on the measured cluster length distribution in Cu interconnects, and the simulation results are compared with the measured EM results. Finally, the effect of bamboo and cluster segment diffusivity on the EM lifetime will be discussed.

5.2 DETERMINATION OF GRAIN BOUNDARY AND INTERFACE DIFFUSIVITY

The grain boundary and interface diffusivity for CoWP capped structures can be estimated according to the EM results displayed in Figure 4.12 in Chapter 4. According to Equation (4.6), the effective diffusivity $Z_{eff}^{*}D_{eff}$ in Cu interconnects during EM can be expressed as:

$$Z_{eff}^{*}D_{eff} = \frac{Z_N^{*}D_N\delta_N}{h} + \frac{Z_{GB}^{*}D_{GB}\delta_{GB}}{d}f = \frac{\Delta L_{cr}k_B T}{e\rho j\tau} \tag{5.1}$$

where the effective diffusivity consists of two parts: one is from the cap interface and the other is from the grain boundary. To simply the analysis, the term from the grain boundary diffusion is neglected for the large grain structure due to its minimal contribution to the overall diffusion. In this case, the mass transport during EM is assumed to be primarily through the Cu/cap interface. Equation (5.1) can be rewritten as:

$$Z_{eff}^{*} D_{eff} = \frac{Z_N^{*} D_N \delta_N}{h} = \frac{\Delta L_{cr} k_B T}{e\rho j \tau} \tag{5.2}$$

By comparing the EM lifetime data for the large grain structures with different caps, it is projected, based on Equation (5.2), that the effective interface diffusivity of the SiCN cap is about 160 times larger than that of the CoWP cap at the test temperature.

In addition, for the SiCN cap, the EM lifetime of the small grain structure is about one half the large grain structure. According to Equation (5.1), the effective diffusivity of the small grain structure is about two times that of the large grain structure. Therefore, for the small grain structure, the effective grain boundary diffusivity is approximately equal to the interface diffusivity. It is concluded that for CoWP capped Cu interconnects, the effective grain boundary diffusivity $Z_{GB} D_{GB} \delta_{GB}/d$ is at least 160 times larger than the cap interface diffusivity. This indicates that for CoWP capped Cu interconnects, the cap interface diffusion is indeed significantly suppressed and the grain boundary diffusion dominates the mass transport during EM. Therefore, it is appropriate to apply Korhonen's statistical model to study the grain structure effect on the EM lifetime and statistics in Cu interconnects with CoWP capping.

5.3 MICROSTRUCTURE-BASED MODEL FOR EM DAMAGE FORMATION IN CU INTERCONNECTS

5.3.1 Stress Evolution during EM

In this section, the basic microstructure used in the statistical model is described first. Figure 5.1 shows the longitudinal TEM image of the Cu interconnect and two schematics illustrating the grain boundaries. The Cu grain structure is comprised of two types of line segments which are connected in series: the poly-grain cluster segment and the single-grain bamboo segment. The poly-grain cluster segment consists of at least one grain boundary parallel to the line direction, while the bamboo segment has one large grain spanning over the whole cross-section of the line. The atomic diffusion in the cluster segment is dominated by grain boundary diffusion, which is much faster than the interface-dominated diffusion in the bamboo segment. As shown in the previous section, the cap interface diffusion is very small compared to the grain boundary diffusion due to the CoWP capping. During EM, the bamboo grains, having much smaller effective diffusivity than cluster grains, can essentially block the diffusion from cluster grains. Within the poly-grain clusters, however, stresses can build up easily and voids will nucleate and grow quickly through the grain boundary diffusion.

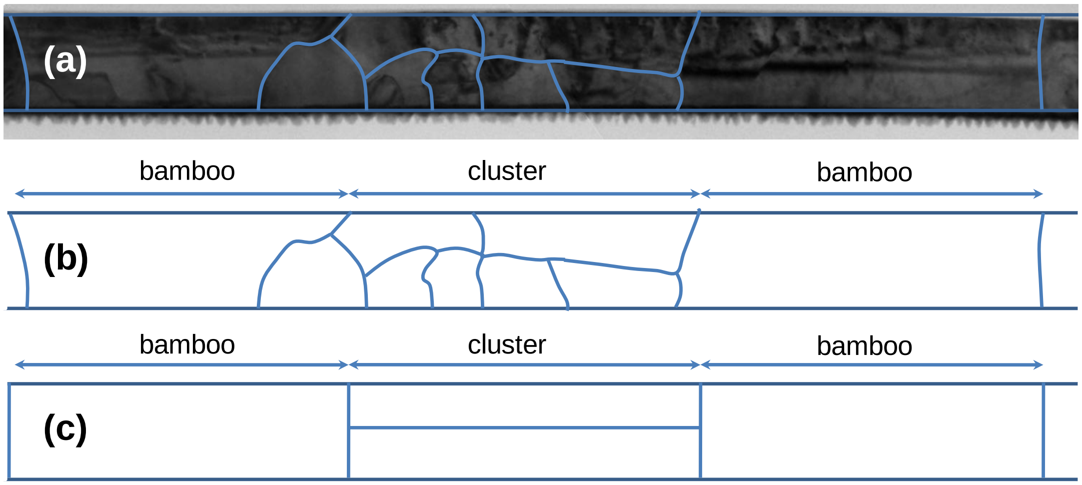


Figure 5.1 (a) Longitudinal TEM image showing Cu microstructure. (b) Schematic drawing of grain boundaries in Cu interconnects indicating both poly-grain cluster segment and single-grain bamboo segment. (c) Simplified Cu microstructure with cluster and bamboo grains connected in series.

During EM, given the EM driving force of $\gamma = |eEZ^*/\Omega\,| = |eZ^*\rho j/\Omega|$, the mass flux J in the metal line can be expressed as:

$$J = \frac{D}{kT}\left(\frac{d\sigma}{dx} + \gamma\right) \tag{5.3}$$

where D is the atomic diffusivity, k is the Boltzmann constant, T is the absolute temperature, σ is the stress in the metal line, e is the elementary charge, Z^* is the effective charge number, E is the electric field, Ω is the atomic volume, ρ is the metal resistivity and j is the current density.

In the confined metal lines with blocked boundary conditions at both ends, i.e., zero flux boundary conditions, the requirement of mass balance yields the governing differential equation for stress evolution as follows [Korhonen 1993b]:

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}[k(\frac{\partial \sigma}{\partial x} + \gamma)] \tag{5.4}$$

where $k = DB\Omega/kT$ is the effective diffusivity, in which B is the effective bulk modulus.

By solving Equation (5.4), the stress evolution as a function of time for different locations in a typical interconnect is shown in Figure 5.2. Figure 5.2(a) shows the case where no void forms, and Figure 5.2(b) is for the case where voids form at the cathode end of the cluster grains. It can be seen in Figure 5.2(a) that, at time t_o when no current flows in the line, the stress is essentially zero in the line in the absence of residual thermal stress. Then when an electrical current is applied, the very low diffusivity in the bamboo segment makes it act as a blocking boundary for the cluster segment. The fast grain boundary diffusion in the cluster segment enables a rapid stress buildup. A tensile stress builds up at the cathode end of the cluster segment and a compressive stress is developed at the anode end of the cluster segment. Finally, atoms start to diffuse in the bamboo segment and eventually a quasi-steady state of stress is developed, which is depicted as the solid line in Figure 5.2(a). However, when voids form at the cathode end of the cluster segment, the stresses are compressive everywhere in the metal line, as shown in Figure 5.2(b), even though the final stress pattern looks similar to the case in Figure 5.2(a). The difference is due to the fact that voids are effective sinks for the atoms and the stress next to them must be essentially zero.

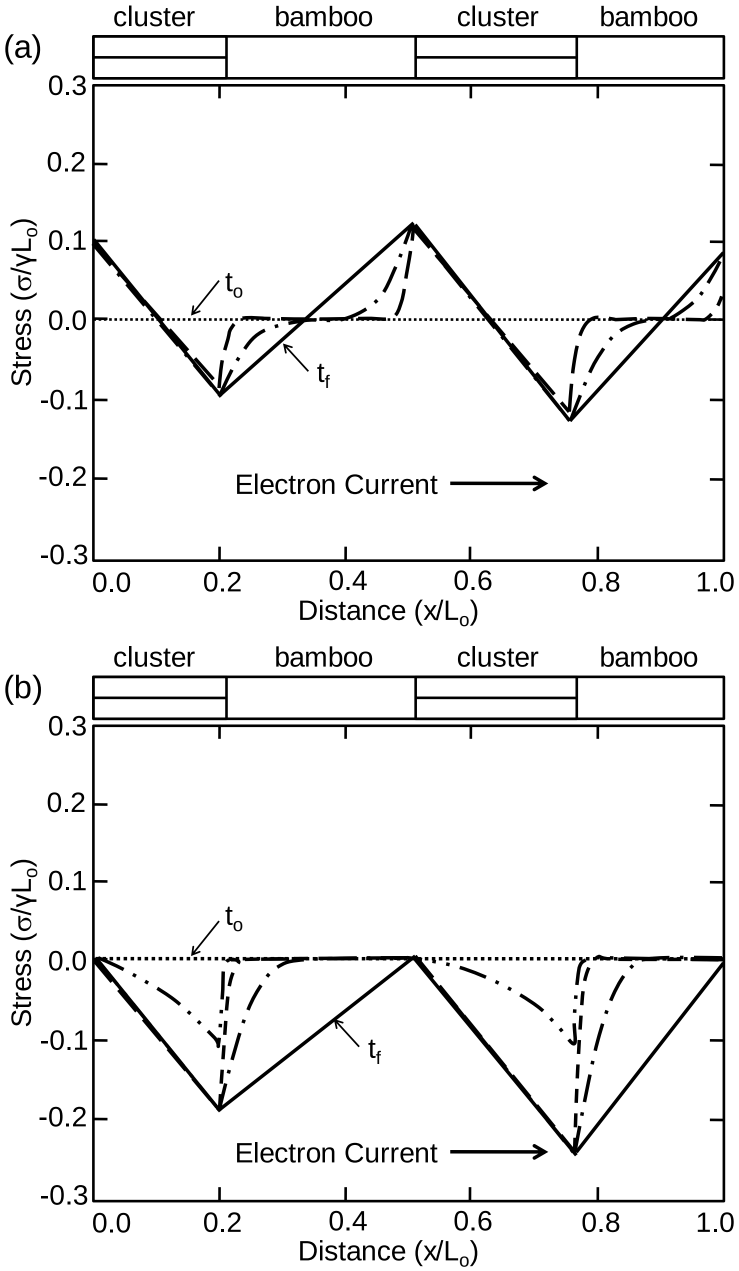


Figure 5.2 Illustration of stress distribution during EM in a line section consisting of cluster and bamboo grains. The initial stress is indicated by the small dotted line while the final stress distribution is shown by the solid line; the broken lines indicate the stresses at intermediate times. (a) No void formation and (b) voids formed at the cathode end of the cluster grains. [Korhonen 1993a].

5.3.2 EM Lifetime vs. Cluster Length

Considering a certain cluster with length $L>L_c$, the stress evolution solved from Equation (5.4) can be written as:

$$\sigma = -\gamma[x - 2L\sum_{n=0}^{\infty}(-1)^n \exp(-m^2 k_c t / L^2)\sin(mx/L)/m^2] \tag{5.5}$$

where $k_c = D_c B\Omega/kT$ is the effective diffusivity in the cluster segment and $m = (n+1/2)\pi$. To simplify the model, the thermally induced stress is ignored in Equation (5.5) and in the following discussion. The void volume $V_o(t)$ at time t up to the steady-state stress distribution can be calculated by integrating the volume strain associated with the atomic distribution as:

$$V_o(t) = (1/B)\int_0^L \sigma(x,t)dx \tag{5.6}$$

where the void volume is normalized by the cross-sectional area of the metal line. Substitution and integration of Equation (5.6) gives the following expression:

$$V_o(t) = \gamma L^2 / 2B[1 - 4\sum_{n=0}^{\infty}(-1)^n \exp(-m^2 k_c t / L^2)/m^3] \tag{5.7}$$

Figure 5.3 plots the void growth in a cluster segment based on Equation (5.7). The cluster length L is assumed to be 1.0 μm as a typical example. Initially, the void grows linearly with time; then the void saturates and levels out as the current stressing continues. The maximum void volume that can be reached is given by $\gamma L^2/2B$. According to Equation (5.7) and Figure 5.3, the characteristic time required to reach 90% of the final void volume is given as [Korhonen 1993a]:

$$t_1 = \frac{L^2}{k_c} \tag{5.8}$$

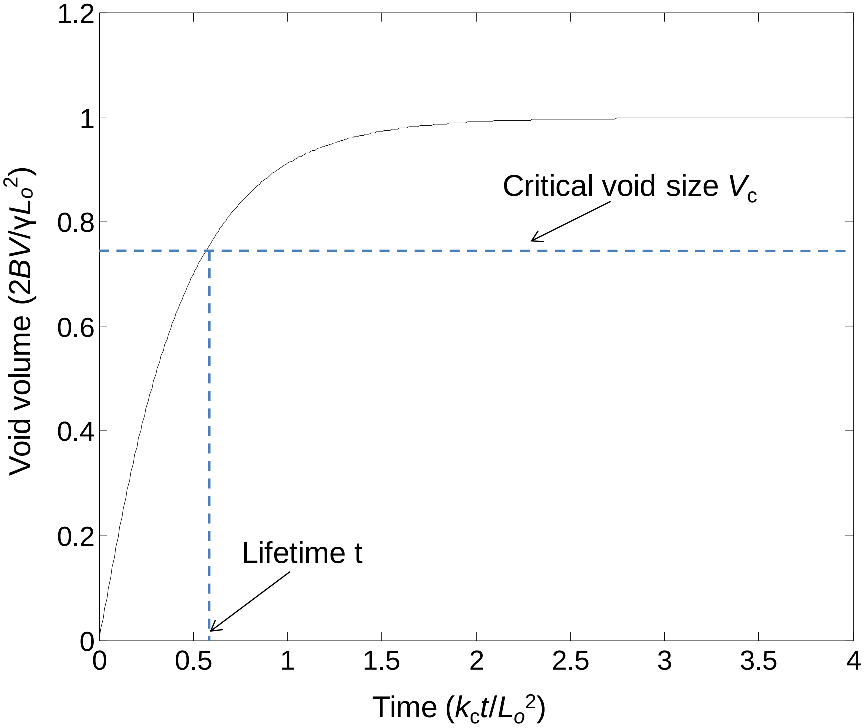


Figure 5.3 Void growth as a function of time in a cluster segment with $L = 1.0$ µm. The critical void size V_c is selected arbitrarily for the illustration of the EM lifetime determination for the case of $L > L_c$.

Equation (5.8) indicates that for a cluster with length $L > L_c$, the characteristic time depends solely on the cluster length and the effective diffusivity inside the cluster, independent of the applied current density. If the EM failure criterion is defined as the void growth to a critical size V_c, the EM lifetime of the cluster can be determined by substituting V_c into Equation (5.7) and solving for the corresponding time *t*.

When the cluster length is shorter and fulfills $L < L_c$, the void growth in the cluster itself is not large enough to cause the interconnect failure. In this case, the bamboo segment is needed to participate in the atomic diffusion process. Here, the EM lifetime consists of two parts: one for the void nucleation and growth time (t_1) in the cluster segment, which is given by Equation (5.8); the other for the void growth time (t_2) inside the bamboo segment. Thus, the total lifetime required can be represented by the following equation [Korhonen 1993a]:

$$t = t_1 + t_2 = \frac{L^2}{k_c} + \frac{[(BV_c - \gamma L^2/2)/\gamma L]^2}{k_b} \tag{5.9}$$

where k_b is the effective interface diffusivity in the bamboo segment. This equation gives the direct relation between the EM lifetime *t* and the cluster size *L* for $L < L_c$. In the Cu interconnects, the typical cluster size *L* is usually much smaller than L_c (~ 20 μm) [Lee 2003]. Accordingly, Equation (5.9) will be applied to calculate the EM lifetime of a failure unit with the cluster length *L* as discussed in the following section.

5.4 THE WEAKEST-LINK MODEL

If the cluster inside the line is longer than the critical length L_c, the line will be able to accommodate enough atoms for the void to reach the critical size and cause a rapid failure of the metal line. The cluster in this case is the weakest link and the failure usually falls into the category of early failure, because the degradation process involves solely the fast grain boundary diffusions. However, if all the cluster lengths are smaller than L_c, the void growth inside a single cluster is not large enough to fail the line. In this case, the atoms must diffuse into the bamboo segments so that the void can grow large enough to cause the metal line failure. Essentially the mass exchange through the bamboo segment induces the failure. Therefore, the EM degradation is governed by the much slower interface diffusion in the bamboo segments and thus results in a much longer EM lifetime. Here the failure unit is defined as a cluster segment connected with its neighboring bamboo segment.

For a line with N failure units connected in series, let $F(t)$ be the probability that the lifetime of a single unit is smaller than t, assuming that the N segments are alike and equivalent, then the following equation

$$F_N(t) = 1 - [1 - F(t)]^{N} \tag{5.10}$$

gives the probability of this line surviving up to time t. The discussion in the previous section shows that the EM lifetime t of a single unit increases monotonically with the increasing cluster length L, as indicated by Equations (5.8) and (5.9). We can define $G(L)$ as the cluster length distribution and $G(L)$ is also the probability that a cluster length is smaller than L inside the interconnect. Due to the direct correlation between the cluster length L and its lifetime t, the failure probability of a single unit at time t will be the probability that its cluster length is longer than $L(t)$,

$$F(t) = 1 - G(L) \tag{5.11}$$

Combining Equations (5.10) and (5.11), the lifetime of the line is expressed as:

$$F_N(t) = 1 - [G(L)]^N \tag{5.12}$$

Equation (5.12) indicates that the lifetime distribution of the interconnects is directly related to the grain cluster size distribution inside the metal line.

5.5 DETERMINATION OF CLUSTER LENGTH DISTRIBUTION IN CU INTERCONNECTS

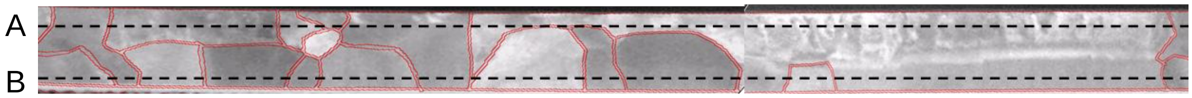
Figure 5.4 shows two grain structures with large grains and small grains. Based on the EM lifetime in Equation (5.12) given by the failure unit model, it is important to analyze the grain structure characteristics for the EM reliability prediction. The grain structure characteristics include the average poly-grain cluster length, the cluster length distribution, and the bamboo segment length distributions. Figures 5.5-5.8 show the poly-grain cluster length distribution for large and small grain structures with different distribution functions used to fit the data. In Figures 5.5-5.6, a lognormal distribution function is applied, and in Figures 5.7-5.8, an exponential distribution function is used. It can be seen that the lognormal distribution function fits the data very well while the exponential distribution gives a bad fit. This observation is consistent with the findings described in Chapter 3 that the grain size distribution in damascene Cu interconnects generally follows a lognormal distribution function [Hauschildt 2005]. Therefore, the cumulative distribution function of the cluster length distribution can be numerically expressed as:

$$G(L;\mu,\sigma)=\frac{1}{2}erfc(-\frac{\ln L-\mu}{\sigma\sqrt{2}}) \tag{5.13}$$

where L is the cluster length, μ is the mean, σ is the standard deviation, and *erfc* is the complimentary error function. Table 5.1 summarizes the fitting parameters in the lognormal distribution function for the large and small grain structures.

In the following section, the EM lifetime and statistics for the copper interconnects will be predicted by combining the weakest-link failure unit model (Equation (5.12)), the cluster length-EM lifetime correlation (Equation (5.9)), with the cluster length distribution (Equation (5.13)) acquired from the actual Cu microstructure.

(a) Large Grain



(b) Small Grain

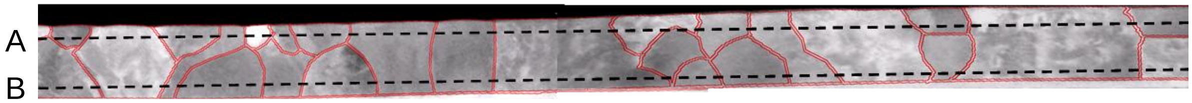


Figure 5.4 Longitudinal TEM images showing the grain structure for (a) large grains and (b) small grains.

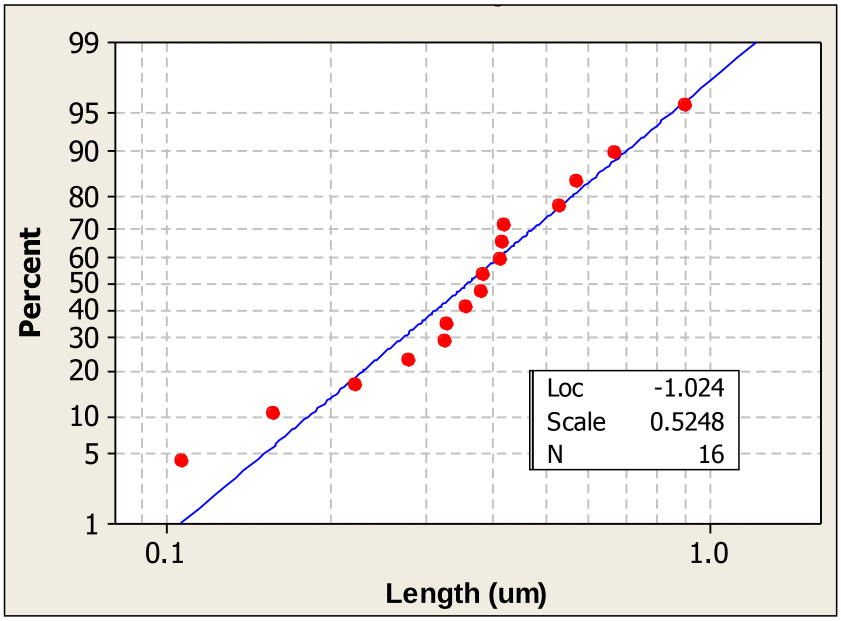


Figure 5.5 Cluster length distribution for the large grain structure with a lognormal distribution function to fit the data.

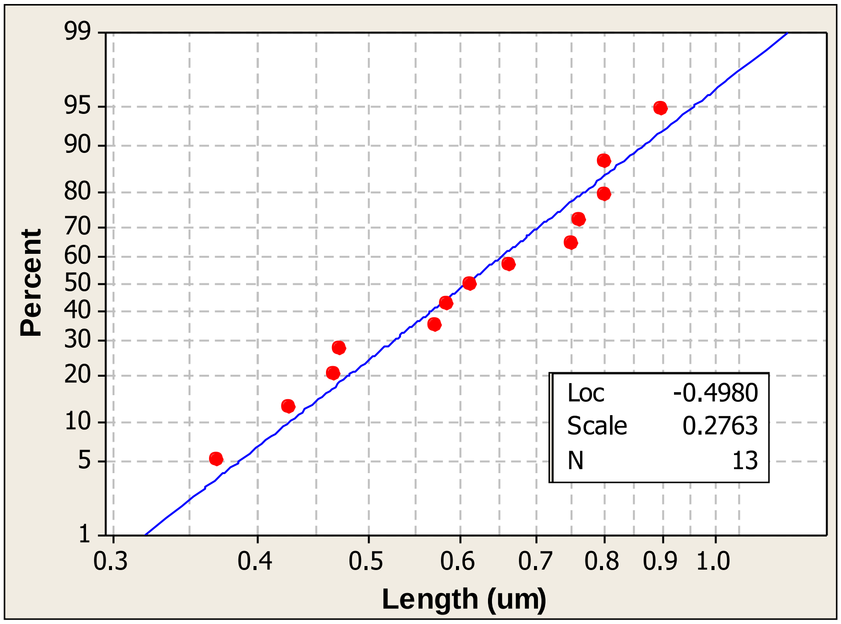


Figure 5.6 Cluster length distribution for the small grain structure with a lognormal distribution function to fit the data.

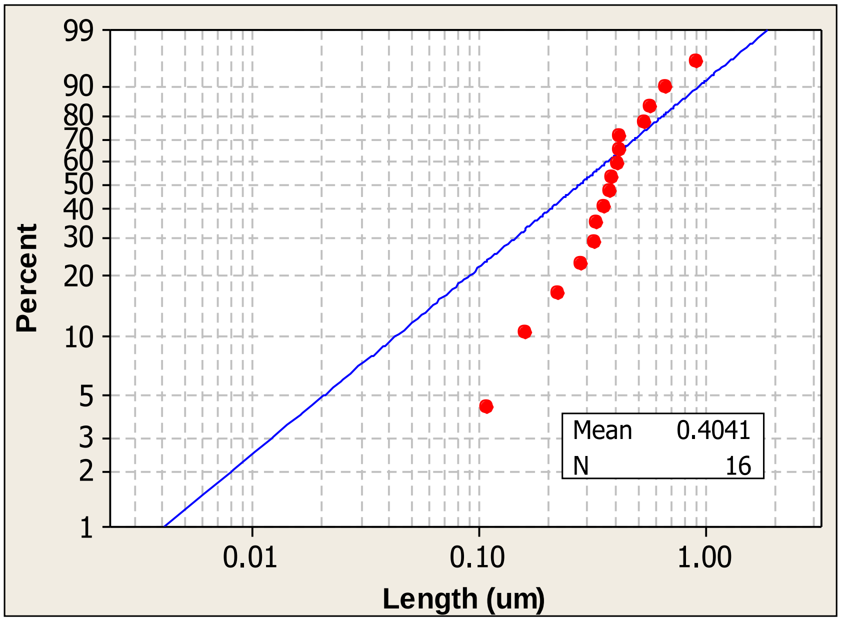


Figure 5.7 Cluster length distribution for the large grain structure with an exponential distribution function to fit the data.

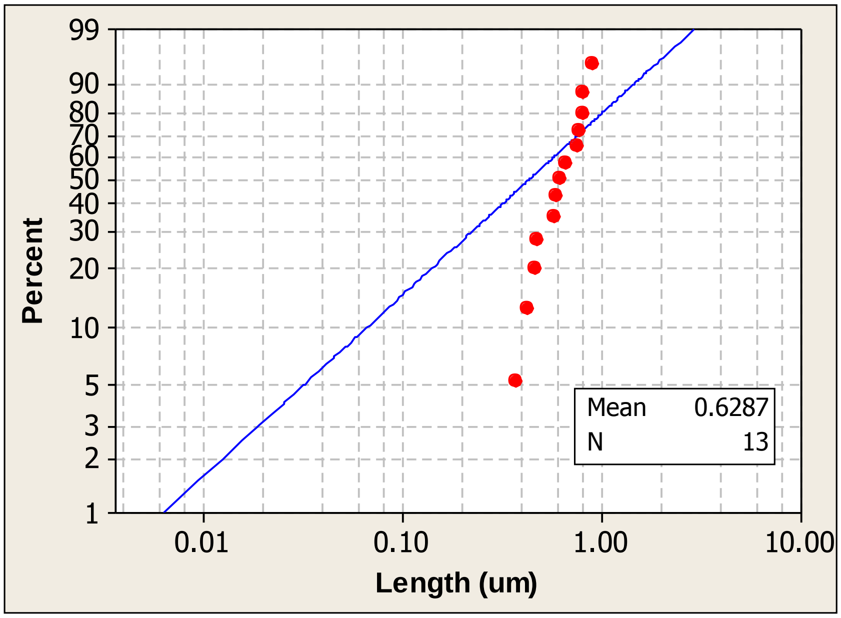


Figure 5.8 Cluster length distribution for the small grain structure with an exponential distribution function to fit the data.

Table 5.1 Cluster length distribution parameters in the lognormal distribution function for the large and small grain structures.

	Median (μm)	**Sigma**
Large Grain	0.36	0.52
Small Grain	0.61	0.28

5.6 SIMULATIONS OF EM LIFETIME AND STATISTICS

5.6.1 Simulation Results

Table 5.2 lists the parameters used in the simulation. The critical void size to cause an EM failure, as determined from the experimental observation, is around 0.06 um (normalized by the cross-sectional area). The Cu grain boundary diffusivity k_c at the test temperature 330 ^oC is estimated to be around 144 $\mu m^2/hr$ according to Reference [Tu 2003], and the effective interface diffusivity in the bamboo segment is assumed to be $k_b \sim k_c/150$ at this temperature. The EM driving force γ is calculated based on a current density of 1.0 MA/cm^2 and the effective charge number $Z^* = -5$ [Sullivan 1967]. For simplicity, the thermal stress σ^T is not taken into account in this model. The effective bulk modulus B for the damascene Cu interconnects surrounded by low-k dielectrics is around 20,000 MPa according to Reference [Lu 2005].

Table 5.2 Parameters used in the simulation.

V_c (μm)	**k_c ($\mu m^2/hr$)**	**γ (MPa/μm)**	**B (MPa)**
0.06	144	50	20,000

Figure 5.9 shows the CDF plots of the EM lifetime for the large and small grain structures with *N* = 1, 2, 4. It can be seen that, for the same *N*, the large grain structure clearly shows a longer EM lifetime and a wider lifetime distribution compared to the small grain structure. In addition, for the same grain structure, an increasing *N* results in a decreasing lifetime and a decreasing lifetime variation, which is consistent with the prediction of the weakest-link statistics and has been confirmed by experiments in Al interconnects [d'Heurle 1978, Kwok 1988]. A fraction of the simulation results is plotted in Figure 5.10 in the probability scale. The solid line in the figure is the linear regression of each curve in the plot. The plot agrees well with the experimental results, as shown in Figure 4.12. The ratio of the extracted lifetimes for large and small grain structures and their respective sigma value are summarized in Table 5.3. The experimental results in Chapter 4 are also compared in this table. It is found that the simulation results agree very well with the experimental observation, especially for the *N* = 1 case. With increasing *N*, the difference in the lifetime statistics for different grain structures is reduced. Given a large enough *N,* the difference eventually vanishes. This suggests that only a few cluster segments close to the cathode end of the line, i.e., one or several failure units corresponding to a small *N*, contribute to the void growth and the final EM failure. This is also consistent with the experimental observations that voids usually form within several microns' distance from the cathode via during EM failure in CoWP capped samples, as shown in Figures 4.15 and 4.16.

This result deduced from this study could be significant suggesting that only the grain structure within one or two cluster segments is important in controlling the EM failure. This indicates that the microstructure effect becomes quite localized and the effect is no longer obtained by statistical average over many segments, as long as there is one defective cluster segment. Producing a desired microstructure to maintain a good EM statistics will require a high degree of perfection in processing over the whole Cu interconnect. Furthermore, it is important to point out that the simultaneous increase in the EM lifetime and the statistical deviation for the large grain structure may not lead to an improvement in EM reliability. In actual integrated circuits, millions of interconnects are connected in series to execute a logic function. It is the very first failure that controls the overall EM lifetime. The EM lifetime at the very low percentile is not only related to the mean time to failure (MTTF), but also closely related to the statistical deviation.

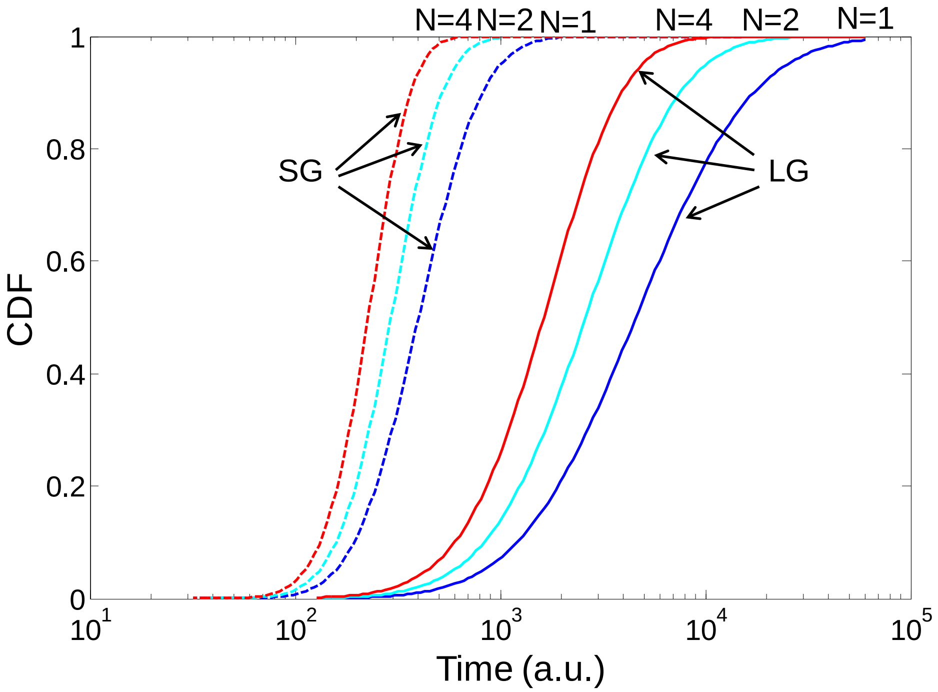


Figure 5.9 Simulated CDF plots for large and small grain structures with *N* = 1, 2, 4.

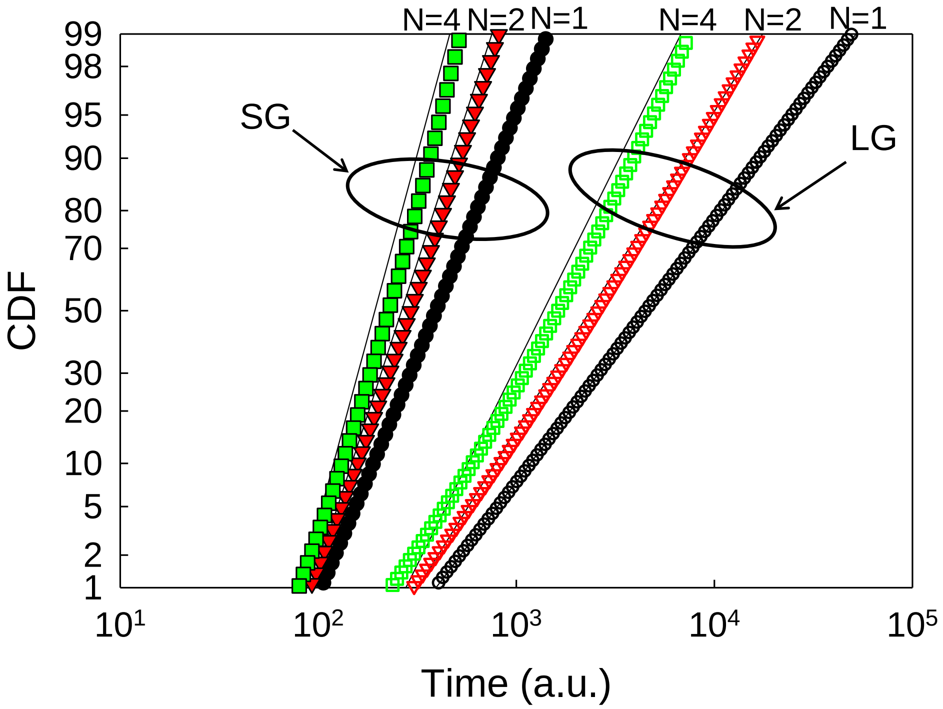


Figure 5.10 Simulated CDF plots for large and small grain structures with *N*=1, 2, 4 in the probability scale.

Table 5.3 Simulation and experimental results of EM lifetime and statistics for large and small grains.

	Simulation (N=1)		**Experiment**	
	LG	**SG**	**LG**	**SG**
Sigma	1.05	0.57	0.88	0.53
t_{50} Ratio (LG/SG)	12		14	

5.6.2 Discussion

The effects of k_b and k_c on the lifetime distribution will be discussed further in this section. Figure 5.11 depicts the lifetime distribution with different k_b, which demonstrates a strong effect on MTTF. With a constant k_c, when k_b decreases from $1/150k_c$ to $1/15{,}000k_c$, the MTTF increases by ~100 times. However, for a constant k_b, the MTTF remains the same when k_c increases from $150k_b$ to $15{,}000k_b$, as shown in Figure 5.12. This suggests that the diffusion process in the bamboo segment strongly affects the EM lifetime. For clusters significantly shorter than L_c, due to the fact that the effective diffusivity in the cluster segment is much larger than that in the bamboo segment, the lifetime will be predominantly controlled by the slow process, i.e., the atomic diffusion and void growth in the bamboo segments.

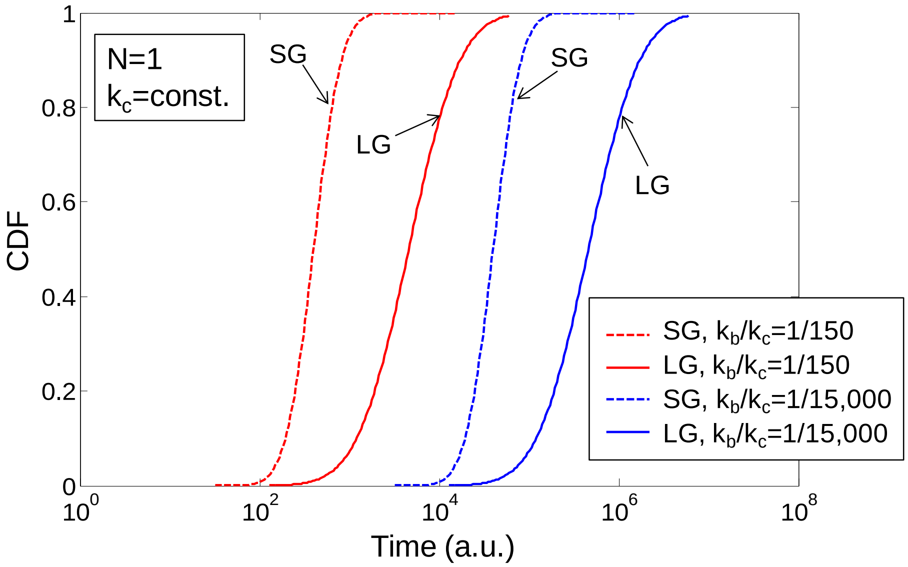


Figure 5.11 CDF plots ($N = 1$) for large and small grain structures with a fixed k_c and different k_b values. k_b demonstrates a significant effect on the EM lifetime.

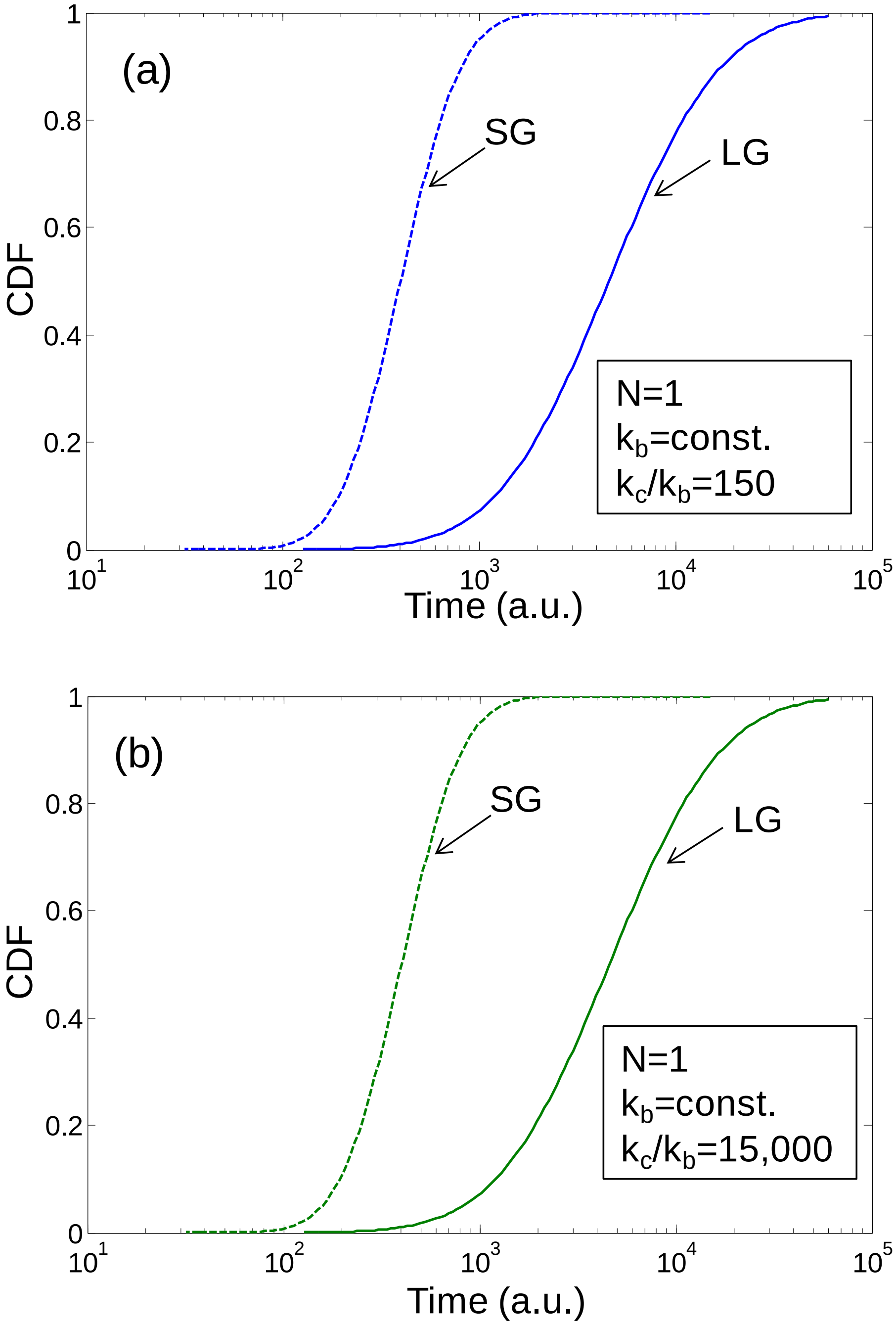


Figure 5.12 CDF plots ($N = 1$) for large and small grain structures with a fixed k_b and different k_c values: (a) k_c/k_b = 150 and (b) k_c/k_b = 15,000. k_c shows little effect on the EM lifetime.

Although it seems that cluster diffusivity k_c is not important in terms of the lifetime, the cluster length L does play a crucial role in determining the total lifetime. As mentioned before, the EM lifetime is determined by a critical void size V_c. For a failure unit consisting of a cluster segment and a bamboo segment, the final void size V_c is comprised of two parts: V_1 corresponds to the void volume contributed from the cluster segment and V_2 corresponds to the void volume contributed from the bamboo segment.

$$V = V_1 + V_2 \tag{5.14}$$

The cluster-segment-contributed V_1 is directly related to the cluster length L and can be expressed as:

$$V_1 = \gamma L^2 / 2B \tag{5.15}$$

Equation (5.15) indicates that a larger L will result in a larger V_1. Therefore, a smaller V_2 is required to reach the critical void size V_c. Due to the significantly larger effective diffusivity in the cluster segment than in the bamboo segment, a slight increase in V_1 will not result in the increase of the lifetime very much; however, the same amount of increase in V_2 can markedly reduce the total lifetime. Consequently, this will result in a shorter lifetime, given the fact that the slow interface diffusion process controls the total lifetime.

It is also important to point out that the bamboo segment in the large grain structure is longer than that in the small grain structure. When the bamboo segment between two clusters is much shorter than the adjacent clusters, the two neighboring clusters start to interact with each other. The interaction can significantly increase the stress that is developed in the metal line and thus accelerate the EM damage formation. This effect has been clearly demonstrated through the stress evolution curve in Reference [Brown 1995]. It has been shown that not only the cluster length affects the EM lifetime, but the bamboo segment length and distribution also affect the stress evolution and may eventually dominate the overall damage evolution in real circuits. In the current study, the difference in the bamboo segment length for large and small grains is simplified by a diffusivity coefficient. The effective interface diffusivity in the small grain structure was assumed to be 4 times as large as that in the large grain structure, taking into account the shorter bamboo length in the small grain structure. This results in a reasonable agreement between the simulation results and the experimental observation in terms of the EM lifetime ratio between the large grain and small grain structures. However, to simulate the EM lifetime and statistics more accurately, the bamboo segment distribution and the effect of bamboo length on cluster-to-cluster interaction must be included in the model.

5.7 SUMMARY

In this chapter, EM statistics for Cu interconnects with CoWP capping was analyzed using a microstructure-based statistical model. The model was applied to a specific case where the interfacial diffusivity is effectively suppressed, leading to the grain boundary diffusion dominating the mass transport under EM. The physical picture behind the model is the following. For clusters shorter than the critical length L_c, the failure unit is composed of a cluster grain and a bamboo grain. The void formation initiates at the cathode end of the cluster grain, and the atoms need to diffuse through the bamboo grain in order for the void to grow large enough to cause the EM failure. A direct correlation between the cluster length L and the EM lifetime t is established: the lifetime is directly related to the cluster length in the failure unit and the effective interface diffusivity in the cluster and bamboo segment. Based on this relation and the weakest-link model and combined with the cluster length distribution obtained from the actual Cu interconnects, the EM lifetime and statistics were modeled. The simulation results agree well with the experimental observations, confirming that the longer EM lifetime and the larger statistical deviation for the large grain structure stem from its shorter average cluster length and wider cluster length distribution. It is also found that based on the weakest-link model, only a few clusters close to the cathode end of the line (small N) control the EM statistics, which is consistent with the experimental observation that voids usually form within 10 μm distance from the cathode end of the line. The combination of simulation results and experimental observations suggests that for the CoWP capped Cu interconnects, the grain structure plays a key role in controlling the EM lifetime and statistics. The microstructure effect could become increasingly important as the Cu interconnect continues to be scaled. Due to the large lifetime deviation, the CoWP capped Cu interconnects with large grains may not make the expected improvement in the overall EM reliability of actual integrated circuits, in which millions of interconnects are connected in series to achieve a logic function.

Chapter 6: Conclusions and Suggestions for Future Work

6.1 CONCLUSIONS

Although the scaling effect on EM reliability has been widely investigated, the continuing scaling and the introduction of new materials and processes give rise to new reliability concerns and challenges in Cu/low-*k* interconnects. This dissertation investigated the scaling effects on EM lifetime and Cu grain structures, as well as the Cu grain structure effect on EM characteristics, particularly for the CoWP capped interconnects.

The via scaling effect on EM reliability for Cu/low-*k* interconnects was first studied using two types of upstream EM test structures. EM tests were first performed by keeping the current density in the M2 line constant at 1.0 MA/cm^2. For the type I structure wherein the line width was scaled with the via size, the EM lifetime degraded as the via size was scaled. However, for the type II structure with a constant via size and a varied line width, the EM lifetime and statistics were found to be similar, independent of the M2 line width. The difference in the EM behaviors for the two types of structures can be interpreted by using an intrinsic failure model. In this model, the cathode end trench voiding is driven by the mass transport along the Cu/SiN$_x$ cap interface and the EM lifetime is directly proportional to the critical void length, which is the via size in this study. Further investigations of the EM data for the type II structure showed that the via with wider M2 lines could support a higher current density without degrading the overall EM reliability. An important parameter, the maximum current density a single via can support, was evaluated by applying higher current densities, 2~4 MA/cm^2, to the type II structure. However, due to the process control of the samples and some external damage, it was difficult to extract a meaningful maximum current density value from the EM data.

Nevertheless, the results of this study demonstrated that the EM lifetime degraded due to the reduced critical void length caused by the via size scaling.

The line scaling effect on Cu microstructures was investigated on ultra-narrow Cu interconnects fabricated by the damascene process with a trench filling of a SiON layer. Both plan-view and cross-sectional TEM samples were prepared and investigated for Cu lines with different line widths: 850, 185, and 60 nm. The plan-view TEM image analysis showed that, compared to the 185 nm lines, the 60 nm lines had a larger population of small grains, which was attributed to the scaling-induced small grain growth. Cross-sectional TEM images showed that, while the 850 nm lines had bamboo-like grain structures across the line thickness, the 185 nm and the 60 nm lines had a mixture of polycrystalline and bamboo-like structures with more small grains at the trench bottom. The presence of more small grains in the ultra-narrow Cu trench was attributed to inadequate grain growth possibly due to a higher surface to volume ratio and a larger proportion of Cu seed at the trench bottom. A 3D Monte Carlo method based on the modified Potts model was used to simulate the grain growth in the damascene lines. By considering the grain boundary and effective "surface" energies in the model, the effects of the overburden and the surface energy on the microstructure evolution in the damascene trenches were modeled. The resultant grain structure could be used as an input to the EM lifetime model to investigate the scaling-induced grain structure effect on EM reliability.

Then the effects of the cap layer and the grain structure on EM reliability were investigated by performing downstream EM tests on four sets of Cu interconnects: large/small grain structures with SiCN/CoWP caps. The effect of failure criteria on EM lifetime, statistics, and activation energy for Cu interconnects was first studied, and then the correlation between the void formation/evolution and the resistance trace was reviewed. In this study, a 10% resistance increase was selected as the failure criterion.

The EM results of the four sets of Cu interconnects showed significant cap layer and grain size effects on EM reliability. Compared to the SiCN cap, the CoWP cap significantly improved the EM lifetime by ~25 times for the small grain structure and >100 times for the large grain structure. The effect of the grain structure on EM performance was observed to be more significant for the CoWP cap than for the SiCN cap. For CoWP capped samples, the large grain structure improved the EM lifetime by ~14 times compared to the small grain structure, which is accompanied with the statistical variation σ changing from 0.88 to 0.54. In contrast, the grain structure effect was less pronounced for the SiCN capped samples, with ~2x difference in the EM lifetime and no significant effect in the statistical variation. The results indicated that, for CoWP capped structures with the interface diffusion being suppressed, the grain boundary diffusion dominated the mass transport where the grain structure played a key role in controlling the EM lifetime and statistics.

Failure analysis showed that two failure modes can be identified by distinct resistance traces and void locations for SiCN capped samples. The mode I failure corresponded to a small initial resistance increase with a void formed at the cathode via corner, while the mode II failure corresponded to a large initial resistance jump with a void formed in the trench away from the cathode via. Overall, the mode II failure demonstrated a longer EM lifetime. In contrast, for CoWP capped samples, voids mostly formed in the trench, several microns away from the cathode via, corresponding to mode II failures. The difference in the failure mode for different caps could be understood by considering the void nucleation and evolution process, as well as the effective diffusivity during EM. For SiCN capped structures, voids moved readily along the Cu/SiCN cap interface and some eventually accumulated at the cathode via corner, causing the final failure. However, the atomic diffusion along the Cu/CoWP cap interface was greatly suppressed by the strengthened interface bonding. Voids could not move freely along the Cu line and easily got trapped at interface/grain boundary intersections. In this case, the voiding location was directly controlled by the local grain structure in the Cu line. This suggests that for CoWP capped structures, the grain structure not only affects the mass transport rate, but also impacts the flux divergence site distribution.

Finally, the EM characteristics for Cu interconnects with the CoWP cap were analyzed using a microstructure-based statistical model. This model is suitable for the case where the cap interface diffusion is effectively suppressed and the grain boundary diffusion dominates the mass transport. The physical picture behind the model is the following. For clusters shorter than the critical length L_c, the failure unit is composed of a cluster grain and a bamboo grain. The void growth initiates at the cathode end of the cluster grain, and the metal ions need to diffuse through the bamboo grain in order for the void to grow large enough to cause the EM failure. A direct correlation between the cluster length L and the EM lifetime t is established. This is combined with the weakest-link model, and the cluster length distribution obtained from the actual Cu lines; then the EM lifetime and statistics can be modeled. The simulation results agreed well with the experimental observations, confirming that the longer EM lifetime and the larger sigma for the large grain structure stemmed from its shorter average cluster length and the wider cluster length distribution. It was also found that, in the weakest-link model, only a few clusters (small N) close to the cathode end of the line controlled the EM statistics, which was consistent with the experimental observation that voids usually formed within 10 µm distance from the cathode end of the line. The combination of the simulation results and the experimental observations suggested that, for CoWP capped Cu interconnects, the grain structure plays a key role in controlling the EM lifetime and statistics. The microstructure effect could become increasingly important as the interconnect scaling continues and the grain structure keeps deteriorating.

6.2 SUGGESTIONS FOR FUTURE WORK

As the EM lifetime degrades continuously with interconnect scaling, Cu interconnects with the CoWP cap turns out to be a good candidate for massive production with significantly improved EM performance. The implementation of the CoWP cap can potentially eliminate the EM reliability limit to the maximum current density in the Cu line. Therefore, it is worthwhile to investigate the EM behavior of Cu interconnects with the CoWP cap with further scaling. While the results in this study have shown the significant effect of the grain structure on the EM characteristics for CoWP capped structures, more work needs to be done for future technology developments.

The grain structure effect on EM reliability has been statistically investigated in this work; however, the grain texture information is not included. It would be of great interest to investigate the correlation between the voiding location and the local grain structures (both the grain size and the grain orientation), particularly for Cu interconnects with the CoWP cap.

All the results regarding the CoWP cap presented in this work focused on the EM behavior of single-linked EM test structures. Significant improvement in the EM lifetime was accompanied with an increase in the standard deviation σ. Since in actual integrated circuits, millions of interconnects are connected in series for the chip to function, it is of practical interest to study the EM behavior of multi-linked Cu interconnects. Under the circumstances, the early EM failures at the low percentage can be obtained. This can improve the accuracy of the EM lifetime extraction at the operating conditions.

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