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Direct Sampling Receivers for Broadband Communications

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Dedicated to my children: Jia-Lu Fang and Jia-Ray Fang

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Direct Sampling Receivers for Broadband Communications

Jie Fang, Ph.D.
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Supervisor: Jacob Abraham

Today everything tends to be connected in the Internet of Things (IoT) universe, where a broad variety of communication standards and technologies are used for those connected devices. It is always a dream to design a Software-Defined Radio (SDR) supporting different standards solely based on the software configuration. As integrated-circuit (IC) manufacture and design advance, a partial of SDR can be realized. This thesis investigates one of the most important parts in a SDR: the analog design of a direct sampling (DS) receiver, which mainly consists of a broadband RF front end and a wideband ADC. Especially, a DS receiver shows a great flexibility and efficiency for the simultaneous reception of multiple channels comparing with the traditional parallelism of superheterodyne structure.

The research contributions of this work include (1) demonstration and comparative analysis of two new architectures of broadband RFPGAs: voltage-mode: RFPGA-V and current-mode: RFPGA-I. RFPGA-V and RFPGA-I utilize an innovative interpolation method and current steering approach, respectively, to achieve a fine gain step of 0.25-dB over 40-dB gain range for several GHz frequency range.

Besides, with innovative design, no off-chip inductor is needed for the both RF-PGAs. (2) The design of a 5-GS/s 10b time-interleaved SAR. The ADC power efficiency is significantly improved by many design techniques: the low-energy CDAC switching scheme, optimized input common-mode voltage for comparator, optimal reduced radix-2 capacitor ratio for low-power reference buffers and higher conversion speed, etc. The lane-to-lane mismatches in a time-interleave ADC are minimized by using optimal floor plan and then are calibrated digitally.

Three prototypes: the broadband RF front ends with RFPGA-V, the broadband RF front ends with RFPGA-I and a 5-GHz ADC, are fabricated to verify the proposed ideas in 28nm CMOS technology.

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Chapter 1

Introduction

1.1 Motivation

Today everything tends to be connected in the Internet of Things (IoT) universe, which has created fundamental change throughout society, driving it forward into a connected era. There are broad varieties of communication standards and technologies for numerous applications. These communication technologies can roughly be categorized as short-range communication system like Wi-Fi, Bluetooth, etc., medium-range wireless like cellular communication system, long-range wireless like satellite communication technologies and wired like twisted pair fiber optic and power-line communication. [wikipediaIoT] Among all the communication technologies, several rapid-evolving ones will be briefly introduced in this section.

First, mobile communication system, the largest technology platform in human history, has evolved several generations starting from the first generation mobile network started in early 1980s, as shown in Fig. 1.1. The rapid evolution of cellular network technology has allowed users to experience much faster data speeds and lower latency, and has prompted exponentially data usage for services and applications. The upcoming 5G mobile technology not only is backwards compatible with LTE Evolution for the previous mobile technology gen-

erations, but also includes a New Radio access technology (NR) which is operable at two frequency bands, FR1 (<6 GHz) and FR2 (mm-Wave), as shown in Fig. 1.2. [Qualcomm [2017]][Huawei [2017]][Zaidi et al. [2016]][Salgueiro [2016]][3GPP [2015]]. Meanwhile, such wide 5G spectrum radio access will require breakthroughs in fundamental radio technologies like radio frequency transceiver, miniaturized antenna and so on.

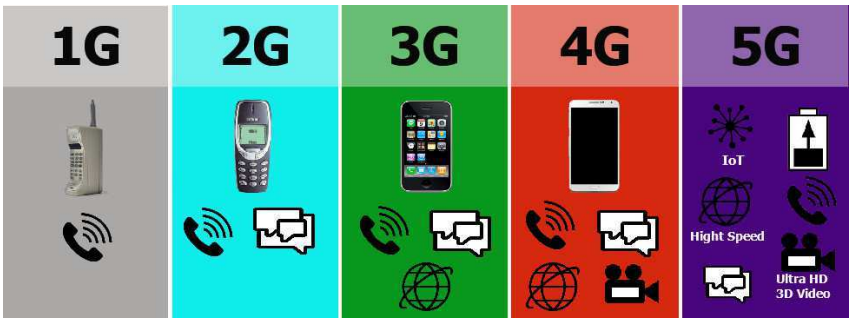

Figure 1.1: Evolution of mobile communication system[Salgueiro [2016]]

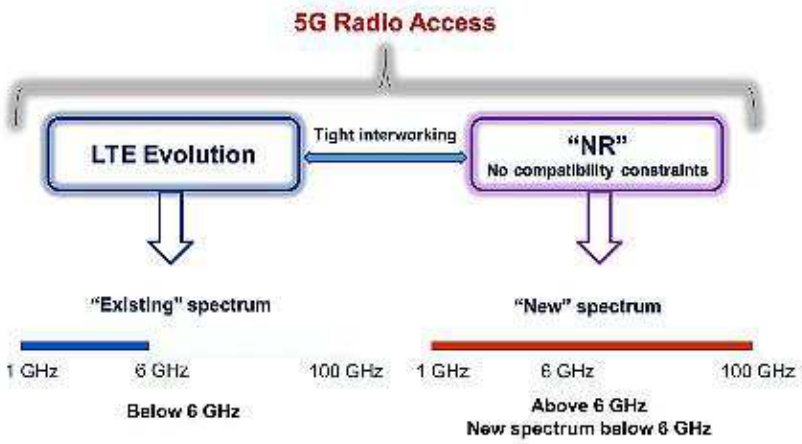

Figure 1.2: 5G Radio Access vision[3GPP [2015]]

Second, a wide range of Smart applications such as Smart Vehicles, Smart Buildings, Smart Cities, Smart Energies, Smart Industries, etc. are rapidly adopted and creates the always-on society. These smart applications mainly rely on wireless sensor network (WSN). The node of WSN includes two parts: the sensors for monitoring and recording the physical conditions of the environment and the short-range wireless radio, which has a numerous of standards such as Wi-Fi, NFC, RFID, Bluetooth, ZigBee, Z-Wave, etc. Those nodes can form different network topologies varying from a simple star network to an advanced multi-hop wireless mesh network. In a self-assembling mesh network, the collected data could be propagated to a gateway node, which directly communicates with servers in the cloud[wikipediaWSN]. Fig. 1.3 shows a possible example: the mesh nodes perform the management tasks, and are controlled and stored in the Internet cloud [Wagenknecht et al. [2014]]. Since hundreds or thousands of nodes are spatially dispersed in many WSNs to monitor temperature, sound, pressure, etc. size and cost constraints on the nodes results in the constrains of sensor function, memory, communication bandwidth and distance and energy. The low-power low-cost design for the sensor and radio in the node is vital in WSNs. Further, the energy-harvest design could be incorporated in the sensor node for many battery-power applications.

Third, the recent ambitious satellite-based projects aiming to provide global broadband Internet services have been announced by a number of companies, such as Boeing, OneWeb, SpaceX and so on. The satellite-based broadband can cover entire regions without the need to build out expensive land-based internet infrastruc-

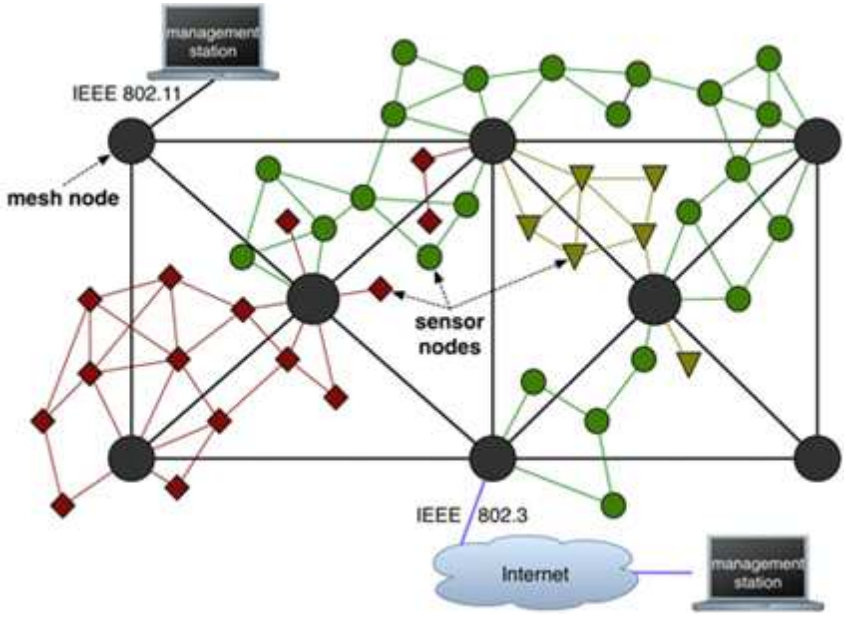

Figure 1.3: A possible WSN [Wagenknecht et al. [2014]]

ture. However, there are several big traditional disadvantages: the costly expense to launch high-altitude satellites, high latency due to the long distance like geostationary orbit (GEO) satellites is about 22 thousand miles above the equator, and weather interruption. Low-earth orbit (LEO) satellites with the altitude of hundreds of miles provide great opportunities to overcome those traditional disadvantages. Especially, LEO satellite features fewer components, lighter weight, easier to manufacture and cheaper to launch. Meanwhile, the issue for LEO satellite method is that each LEO satellite can only cover a much smaller patch of territory. To provide competitive coverage, large satellite constellation, as shown in Fig. 1.4, is needed to form space-based mesh network. For example, Oneweb plans to launch 900 LEO satellites beginning in 2018, to deliver affordable Internet access globally.

SpaceX proposes to initially deploy 800 LEO satellites for initial U.S. and international coverage. Then it wants to throw over 7,000 Very Low Earth Orbit (VLEO) to fill in the blanks as needed. [OnewebSatellites][WikipediaStarlink]. Especially, mmWave band is very suitable due to extra wide bandwidth resource and low space loss without atmospheric absorption for inter-satellite communication in the space.

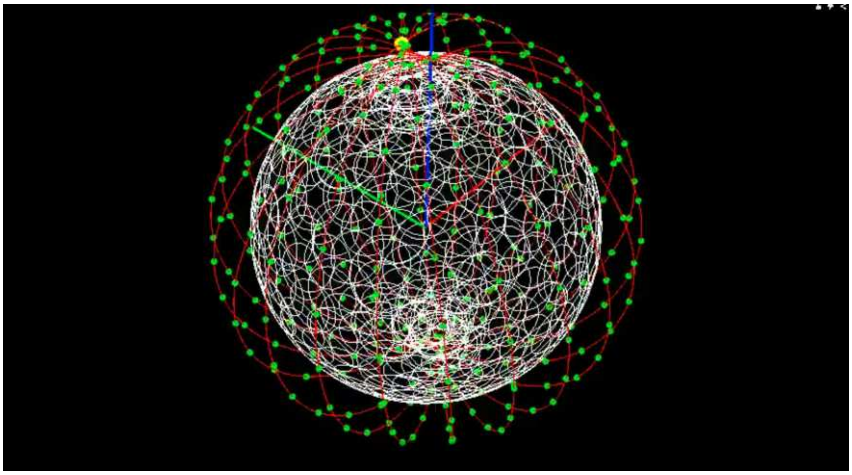

Figure 1.4: LEO constellation[WikipediaStarlink]

The broad variety of communication standards and technologies nowadays are enabled by all sorts of different RF technologies. However, it is always a dream for engineers to design a flexible hardware supporting all of those standards and technologies. Such a design produces a radio which can receive and transmit widely different radio protocols based solely on the software configuration, is often called as the software defined radio (SDR).

The ideal receiver for a SDR would be like that an ADC directly digitizes the incoming RF signal right after an antenna. A digital signal processor and its software would convert the data stream into any other form the application requires.

Similarly, the ideal transmitter would be like that a digital signal processor and its software would generate the data stream based on the different radio protocol. A DAC converts the data stream into a RF signal, which is transmitted by an antenna. The main problem of SDR is that the data converters (ADC and DAC) require a high sampling rate and a high resolution at the same time[WikipediaSDR]. As integrated-circuit (IC) manufacture and design advance, a data converter is approaching the speed and resolution requirement satisfying a partial of SDR applications. The boundary between configurable and non-configurable parts is closed to antenna and it is able to support a broad frequency range. In this thesis, the motivation is to investigate the design of a direct sampling (DS) receiver, one of the most important parts in a SDR.

1.2 Organization

Chapter 2 briefly introduces several concepts for RF communication system: a narrowband RF signal, a broadband RF signal, a superheterodyne receiver and a direct sampling receiver.

Chapter 3 reviews previously reported state-of-art architectures of RFVGA/PGA, then describes and comparatively analyzes two new architectures of RFPGA: voltage-mode RFPGA-V and current-mode RFPGA-I. The broadband RF front ends with either RFPGA-V or RFPGA-I for a direct sampling receiver are manufactured in 28nm CMOS technology. The measurement results of prototypes are discussed.

Chapter 4 presents a 5-GS/s 10b time-interleaved SAR ADC for direct sampling receivers. The ADC power efficiency is significantly improved by many de-

sign techniques: the low-energy CDAC switching scheme, optimized input common-mode voltage for comparator, optimal reduced radix-2 capacitor ratio for low-power reference buffers and higher conversion speed, etc. The measurement results of prototype in 28nm CMOS technology are discussed.

Chapter 5 concludes this thesis and discusses the future research direction.

Chapter 2

Narrowband and Wideband Communications

2.1 Narrowband RF Signal

Many communication systems mentioned in the previous chapter have narrowband incoming RF signals, where desired signal, adjacent-channel interferer (ACI) and an alternate-adjacent channel interferer are in relatively narrow frequency range, as shown in Fig. 2.1. For example, A GSM receiver must withstand 9dB ACI or 41dB higher alternate adjacent channel interference with channel bandwidth of 200 kHz. The off-chip Band-Pass Filter like BAW, SAW, etc. is typical utilized to select the band.

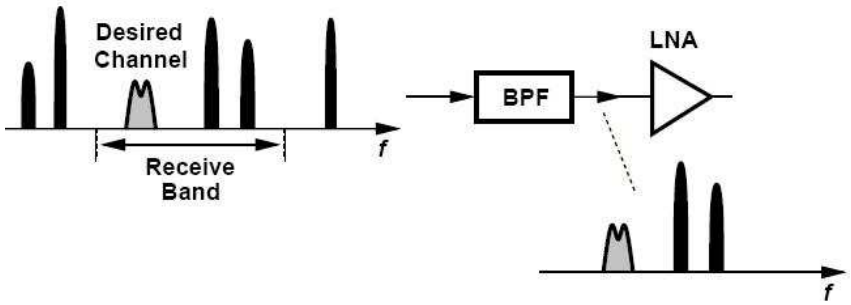

Figure 2.1: Narrow-band RF input and its receiver [Razavi [2011]]

In a transceiver, the circuits like Low-Noise Amplifier (LNA), mixer, ADC, etc., are not perfectly linear and result in distortion products. It is convenient to use a tone to represent the energy of a single channel. Two-tone tests can be a powerful

tool to study the linearity for narrow-band systems. If two tone frequencies are spaced closely, their intermodulation products would fall in band too and can be used to evaluate the linearity. For example, two tones (A and B) will generate third order intermodulation (IM3) products 3A, 3B, 2A + B, 2A - B, 2B + A and 2B - A. The third order products: 2A - B and 2B - A fall in band and can be used to measure the linearity. A common method of the circuit linearity characterization is to measure intercept points for two-tone tests, where each tone has equal signal power. As shown in Fig.2.2(a), as the amplitude of each tone increases, IM3 terms increases in a cubic power of amplitude. The input level and the output level where the fundamental line and the IM3 line meet together, are called input third intercept pint (IIP3) and output third intercept pint (OIP3), respectively. In addition, IIP2 and OIP2 can be similarly defined, where IM2 terms increases in a square power of amplitude, as shown in Fig.2.2(b).

2.2 Broadband RF Signal

In contrast with limited frequency range in a narrowband system, there are many channels spreading over the broad frequency range in a broadband system. Multiple tones are typically used to model a broadband signal. Fig. 2.3 shows one of the most difficult scenarios for a broadband system, where multiple equal-power interference channels are present where the aggregated power of interference could be 30 or 40 dBc higher than the desired channel. As a result, the intermodulation products from the transceiver non-linearity can severely degrade the system SNR at the desired channel, which poses a linearity challenge for a transceiver.

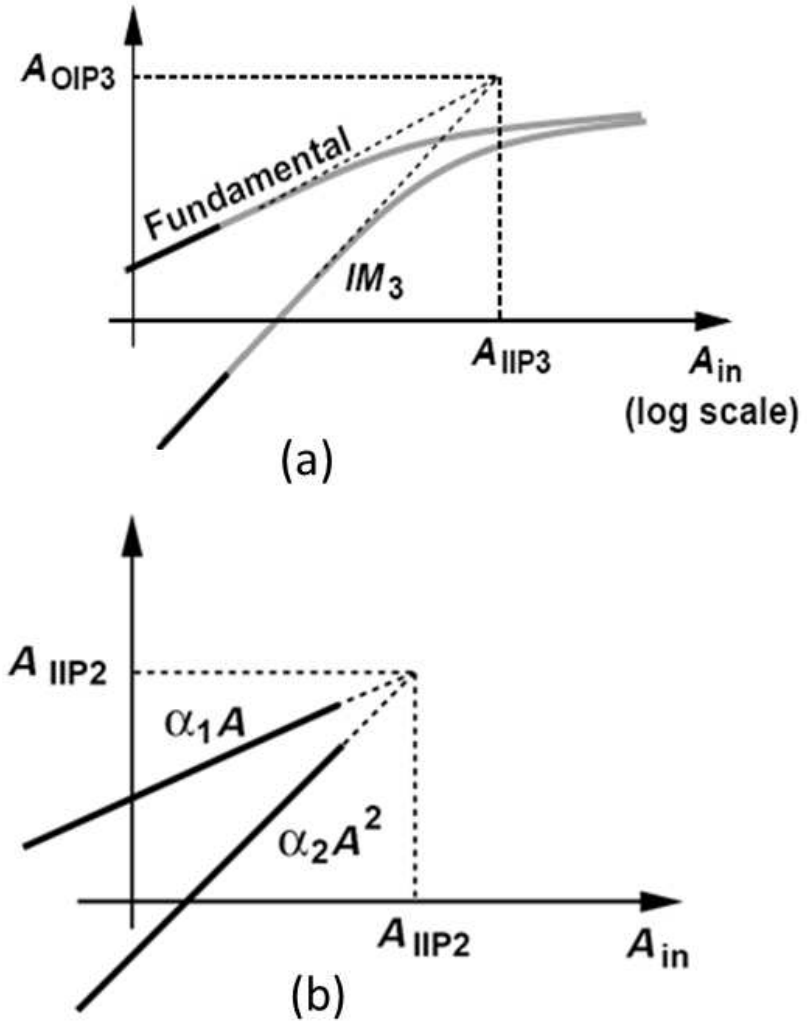

Figure 2.2: (a) definition of IIP3. (b) definition of IIP2.

It is worth noting that since the ratio of maximum to minimum frequency is less than two for a narrowband system, second-order intermodulation specification does not need be significantly considered. In contrast, the second-order intermodulation distortion of the two in-band interferers in broadband systems could

possibly fall into the frequency range of the desired channel, the second-order intermodulation products are as important as the third-order intermodulation products.

Besides IIP2 and IIP3 from two-tone tests, composite second-order (CSO) and composite triple beat (CTB) are also commonly utilized to characterize the broadband system linearity. CSO and CTB are the ratios expressed in dB of the power of the desired channel to the average power of the 2nd and 3rd distorted components centered at the frequency of the desired channel, respectively. As a matter of fact, the approximated relationship between CSO and IIP2 or CTB and IIP3 can be simply derived in [MatrixTestEquipment].

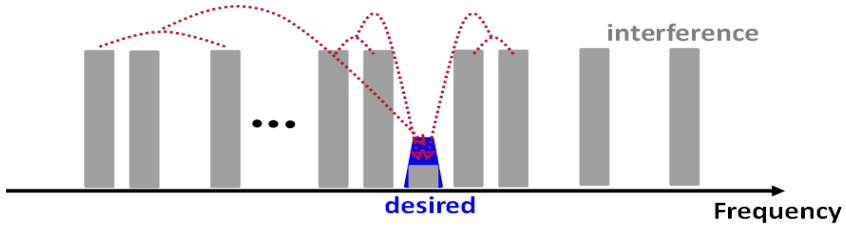

Figure 2.3: Broadband RF signal.

Further, if the number of tones in a broadband system is extended into infinity, then the signal spectrum eventually approaches flat line as band-limited Gaussian noise. Moreover, if the RF signal spectrum becomes noise-like spectrum with an in-band notch, the intermodulation products due to a transceiver non-linearity would result in excess noise at the notch frequency. Noise power ratio, which is defined as the ratio of power spectrum density (PSD) of noise-like signal and PSD at the notch frequency, is another important method to characterize linearity for a broadband system. As shown in Fig. 2.4 [Gomez [2016]], the distortion spectrum

is roughly flat in the middle and tapering at its edges due to the convolution in the frequency domain. In a broadband system, distortion and noise are typically comparable in the fully loading scenario to achieve a power-efficient design.

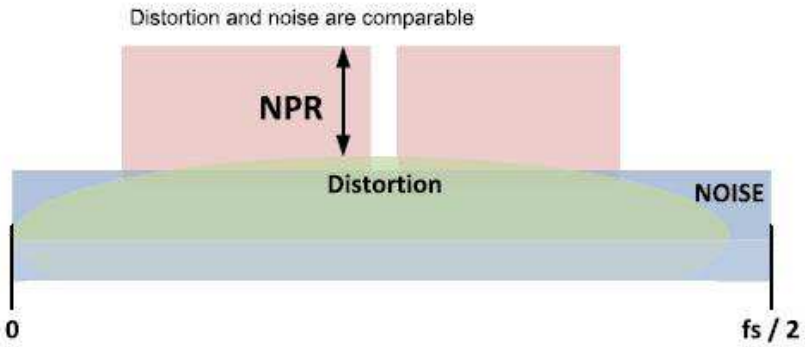

Figure 2.4: Noise power ratio in broadband system.

As mentioned above, broadband RF signal is composite of many channels, usually over 100 channels. According to law of large numbers, a broadband RF signal should have a "bell shape"of Gaussian voltage distribution, as shown in Fig. 2.5. A special example is already described in the last paragraph: the RF input with infinite equal-power channel is actually a band-limited noise, which has a well-known "bell shape "of Gaussian voltage distribution. However, this type of voltage distribution inevitably causes high crest factor or Peak-to-Average Ratio (PAR). For example, OFDM signal in LTE system PAR is approximated 12dB and QAM signal in CATV is approximated 15dB. The large PAR is undesired, because it means that the transceiver needs more dynamic range to handle the large peak signal. On the other hand, the good news is that most of signal information concentrates in the middle of "bell shape", as shown in Fig. 2.5. This property can be used to alleviate

the linearity difficulty, because gain compression for an extra-large signal can be largely tolerated, and a transceiver could be designed targeting at linearity with relatively small signals like 30% of a full scale signal. However, it is worth noting that ”wiggles-like” non-linearity is not tolerated easily most of time.

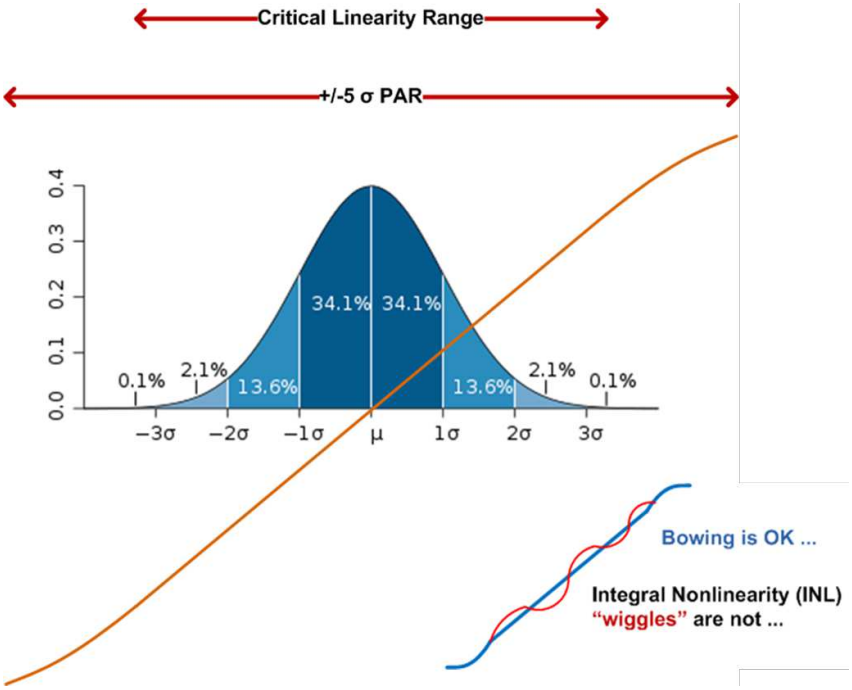

Figure 2.5: Gaussian voltage distribution .

2.3 Superheterodyne Receiver

A superheterodyne receiver, which mixes RF signals in a non-linear fashion and moves signal spectrum into a lower frequency, has been developed and improved by many pioneer engineers over a long history. A significant milestone was R. Fessenden’s ”Liquid barretter”, which later was used to perform the first AM

broadcast by Fessenden himself on 1906 Christmas Eve. Vacuum tube, the first electronic device capable of amplification, was invented by Lee de Forest in 1907. Edwin Armstrong utilized the vacuum tube to invent the regenerative receiver in 1912. After many decades developments, a superheterodyne receiver has become a dominant architecture in radio electronics [Lee [2004]].

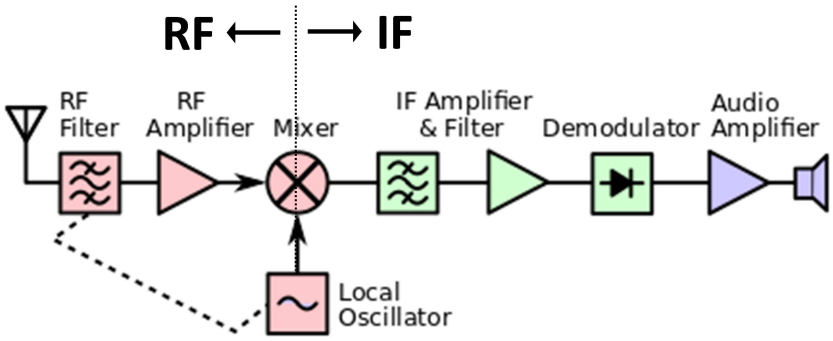

Figure 2.6: Block diagram of a typical superheterodyne receiver.

Fig. 2.6 shows the block diagram of AM/FM radio, a typical superheterodyne receiver and Fig. 2.7 illustrates the spectrum for a typical sperheterodyne receiver. After an antenna receives an incoming RF signal, a RF filter selects band of interest and suppresses image S2, whose frequency is the mirror of the signal S1 frequency with the symmetry of local oscillator (LO) frequency. After mixing a RF signal and LO, band of interest is translated into intermediate frequency (IF). And then an IF filter is utilized to select channel of interest and to reject others. Finally, demodulator extracts the modulated signal and audio amplifier drives a speaker/headset, which plays audio out[Wikipediaradio]. It is worth noting that RF filter's transition band is much wider than that of IF filter, for Q value, which

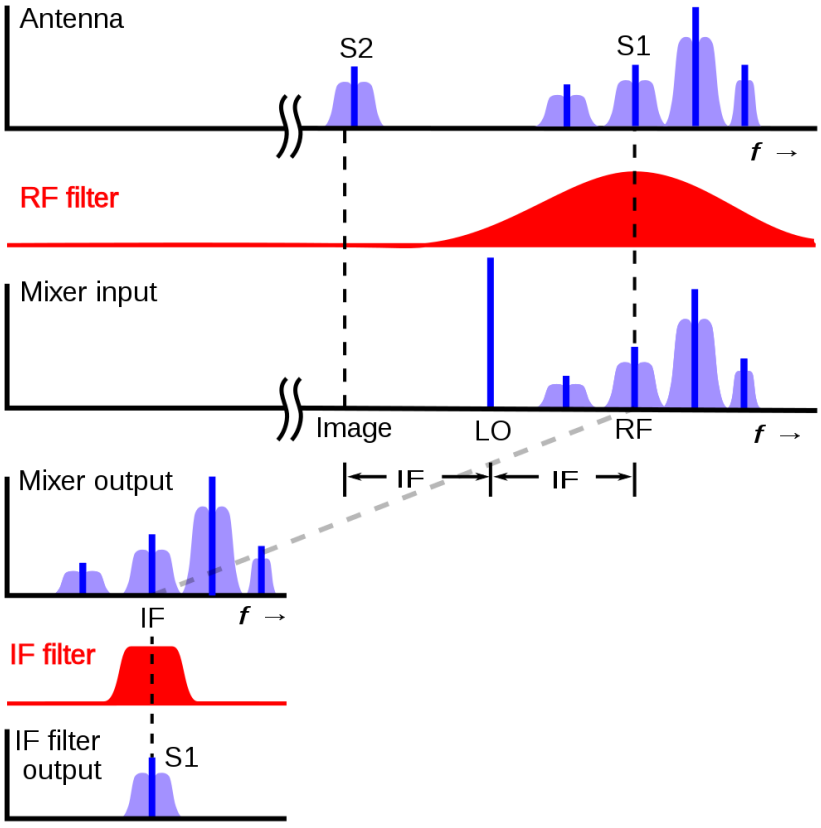

Figure 2.7: Spectrum for a typical superheterodyn receiver.

can be calculated as ratio of 3-dB bandwidth and the center frequency, has to be reasonable for the implementation.

As a matter of fact, one major disadvantage to a superheterodyne receiver is the image issue, especially (1): when the image power is much larger than the signal power, saying 30-dBc higher. (2): and/or when the distance between band of interest and the image frequency is too narrow. An RF filter, which is required to provide sufficient attenuation on images, often relies on expensive off-chip components like

SAW, BAW filters. In addition, the choice of single LO or several LO frequencies can greatly influence the filter complexity in a superheterodyne receiver. [Razavi [2011]] illustrates how to make the proper choice of LO in details.

If LO frequency is chosen right on the center of band of interest, IF would be at DC without any image, as shown in Fig. 2.8. Obviously, quadrature conversion by mixing incoming signal with the quadrature phases of LO is required to preserve the content on the both side of LO frequency. This popular type of receiver is often called zero-IF or direct-conversion architecture. Therefore, the absence of image greatly simplifies the receiver complexity, because (1) much less filtering is needed; (2)mixing spurs are much reduced and easier to handle; (3) A sharp IF LPF filter can be much easier to be implemented for channel selection. However, Zero-IF receivers also have several important issues: LO leakage, DC offset, Flicker noise, even-order distortion, I/Q mismatch and so on.

LO leakage effect is that LO couples into the receiver input through substrate or parasitic capacitance or electromagnetic (EM) emission, de-sensitizing the receiver. Meanwhile, the leaked LO would mix the LO to create a DC offset, called LO self-mixing. DC offset can also be from LO self-mixing and the device mismatch. Since following baseband blocks can provides a large gain, saying 60dB or more, DC offset like 5 mV can significantly reduce the maximum signal swing or even saturates the baseband blocks. A typical method to cancel DC offset is to inject a corrective very-low frequency current back to the receiver. Flicker noise can be considered as slow-moving DC offset and has a similar effect as DC offset. Even-order distortion such as the term of "$A - B$" from RF blocks would cre-

ate low frequency components. Those low-frequency components after the mixer feedthrough could have similar effect of DC offset or Flicker noise.

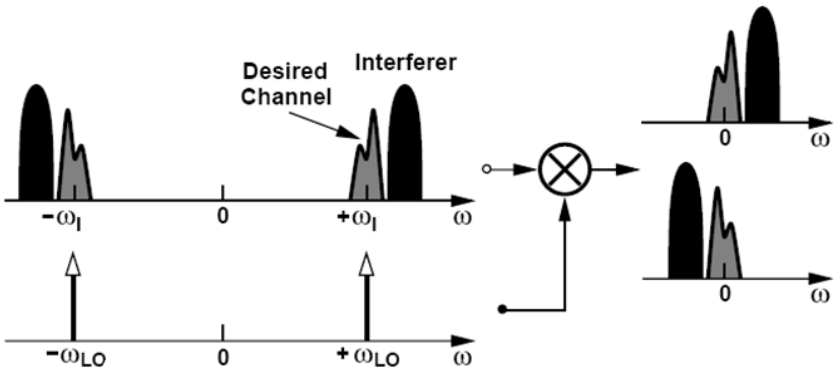

Figure 2.8: Zero-IF spectrum.

IQ mismatch is very important for a superheterodyne receiver, because it could significantly undermine the system SNR or BER in a zero-IF receiver or limit the image rejection ratio (IRR) for an image-reject receiver with none-zero IF. The sources of IQ mismatch can be phase mismatch and gain mismatch from clock paths and from signal paths. Careful IQ mismatch simulations must be performed to evaluate its influence to the system SNR or to satisfy IRR requirement.

2.4 Direct Sampling Receiver

Although superheterodyne receiver is a dominant architecture in radio electronics, the parallelism of superheterodyne receivers, as shown in Fig. 2.9, can be an expensive solution for simultaneous reception of multiple channels in the state-of-art communication applications. First, the power consumption and hardware including the silicon area and the off-chip components like antenna, off-chip fil-

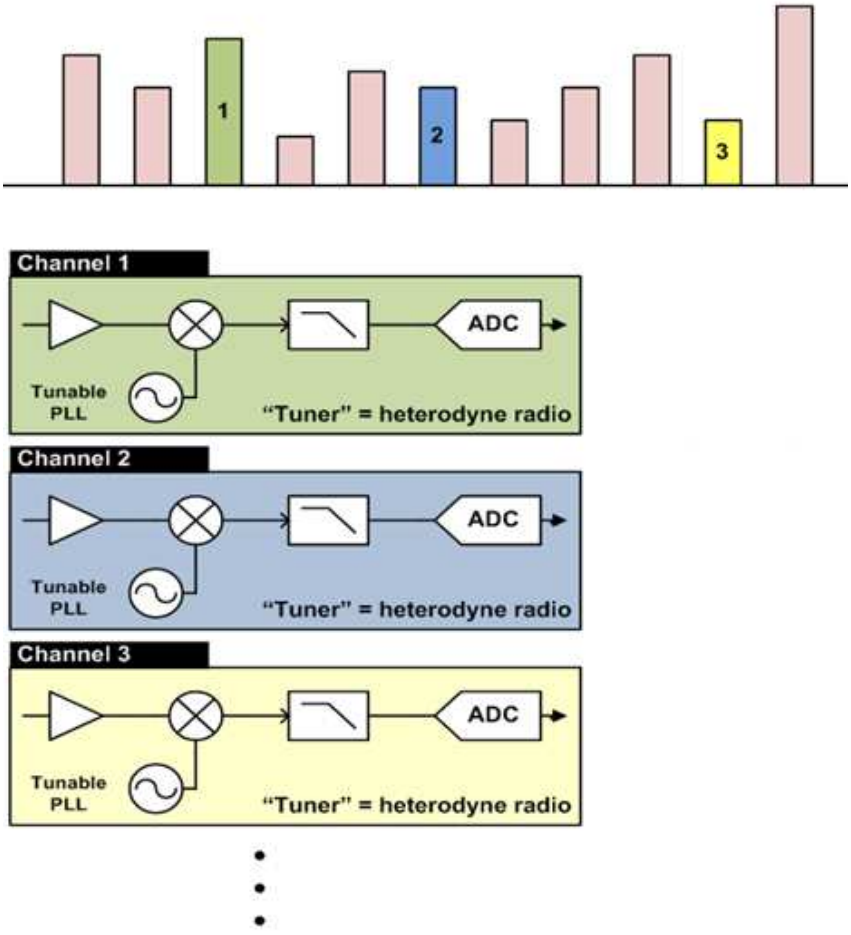

Figure 2.9: Simultaneous reception of multiple channels with superheterodyne receivers.

ters, PCB area explodes linearly with the number of channels. Thinking about the case of an 8- or 16-channel receiver, the power consumption and cost would be too high by using this parallelism idea. Second, each receiver requires a tunable PLL for channel selection, and each PLL has A LC VCO for its low phase noise. For the parallelism of multiple superheterodyne receivers, different VCOs pulling each

other would cause undesired spurs. To manage those spurs into an acceptable level, each PLL needs to be separated widely in layout, which causes extra silicon area.

Because of the above mentioned issues for the parallelism of multiple superheterodyne receivers, a direct sampling (DS) receiver, where entire RF band is digitized by a wideband ADC, is gaining more and more attention. Fig. 2.10 shows a simplified block diagram of a DS receiver. First, an incoming RF signal is received by an antenna, and then is selected for band of interest by an off-chip filter. This band-limited RF signal is fed into to the RF input of an integrated receiver, and conditioned into a proper level by an RF Programmable/Variable-Gain Amplifier (RF-PGA/VGA). And then an anti-aliasing filter (AAF) is applied to restrict the folded noise and distortion before the digitization. Finally, a wideband ADC digitizes the entire spectrum from DC to Nyquist frequency, whereas all down-conversions and demodulations are done as much as possible in the digital domain.

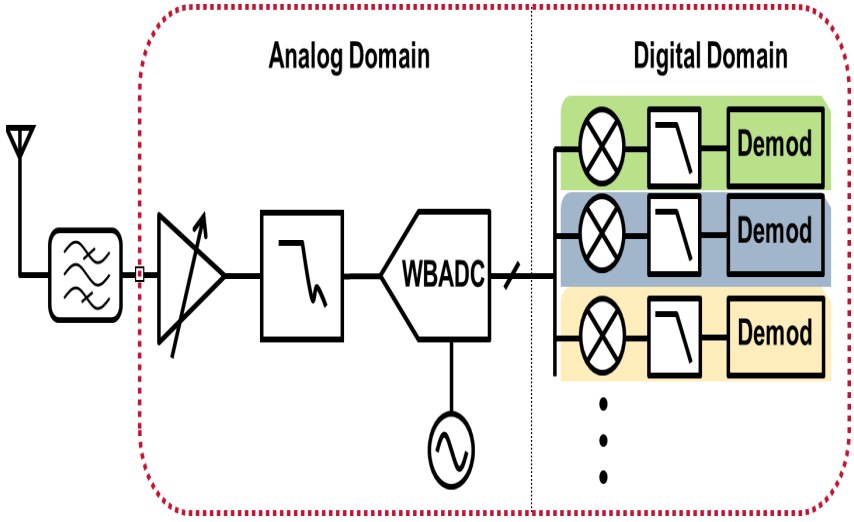

Figure 2.10: Diagram of direct sampling receiver.

Comparing with the analog channel selection using analog mixer and IF filters in a superheterodyne receiver, the digital channel selection is realized by using digital mixers and filters in a DS receiver. First, thanks to evolution of advanced technologies, the digital circuit for digital channel selection is much smaller and consumes much less power. Then, multiple precise tunable PLLs in the parallelism of superheterodyne receivers are no longer needed. Instead, only a fixed frequency PLL for a wideband ADC is needed in a DS receiver. Further, a DS receiver has an inherent fast channel hopping without any fine tuning of an analog PLL. Therefore, a DS receiver is very efficient for the simultaneous reception of multiple channels and dramatically reduces the hardware complexity.

Comparing with a baseband ADC in a superheterodyne receiver, a wideband ADC in a DS receiver is often considered as a RF block because it is in front of the mixing. For a RF block, the noise and linearity performance are usually characterized by NF and IIP3/IIP2, respectively. For an ADC, they are traditionally characterized by SNR and THD, respectively. First, the relationship between SNR and NF will be derived in the following. ADC SNR can be expressed as:

$$SNR_{dB} = P_{FS} - PSD_n - 10log_{10}(f_s/2) \tag{2.1}$$

where P_{FS}, PSD_n, f_s is the power of the full scale signal, power spectral density and sampling frequency, respectively. Meanwhile, NF can be calculated as referencing PSDn to thermal noise at 290 K based on IEEE standard:

$$NF = 10log_{10}(1 + \frac{10^{\frac{PSD_n}{10}}}{k \cdot 290K}) \simeq PSD_n + 174dBm/Hz \tag{2.2}$$

$$NF \simeq P_{FS} - 10log_{10}(f_s/2) - SNR + 174dBm/Hz \tag{2.3}$$

The approximation holds when ADC noise floor is much higher than 174 dBm/Hz. From Eq. 2.3, NF has 1-dB-to-1-dB relationship with ADC SNR.

Next, the relationship between THD and IIP3 will be derived. Assuming the third harmonic is the dominant term among all harmonics. When a full-scale sinusoid wave is applied to ADC, THD is typically specified as:

$$THD_{dB} = P_{FS} - HD_3 \tag{2.4}$$

A two-tone test (A and B) is used for IIP3 calculation, where each tone is set to be 3dB lower to keep the full-scale amplitude. So the third harmonic term for each tone is 9dB lower power. Moreover, according to Binomial theorem for $(x+y)^3$, the third intermodulation (IM3) term (A^2B or AB^2) is 3 times of the third harmonic term (A^3 or B^3) or 9.5dB higher power than that of the third harmonic for a two-tone test. IM3 can be expressed as:

$$IM_3 = 9.5dB + (P_{FS} - 3dB) - (HD_3 - 9dB) \tag{2.5}$$

Thus,

$$IIP3_{dB} = (P_{FS} - 3dB) + IM_3/2 = P_{FS} + \frac{THD_3 + 9.5dB}{2} \tag{2.6}$$

From Eq. 2.6, IIP3 has 0.5-dB-to-1-dB relationship with ADC THD if the third harmonic is dominant among all other harmonics . Taking a specific example:

for a 1-GHz ADC with 1-Vppd full-scale, 10-b SNR and 10-b THD, NF and IIP3 is approximated as 27.7dB and 38.1 dBm with reference of 50-ohm impedance, respectively.

Chapter 3

A Broadband CMOS RF Front-End

This chapter presents comparative analysis between two new architectures for RF programmable-gain amplifiers (RFPGA): voltage-mode RFPGA-V and current-mode RFPGA-I. RFPGA-V utilizes multiple-switch-multiple-amplifier configuration and gain interpolation method to achieve a fine gain step of 0.25-dB over 42-dB gain range for the band of 250 MHz to 2.3 GHz. Meanwhile, RFPGA-I uses a current steering approach to achieve a fine gain step of 0.25-dB over 42-dB gain range for an even wider band of 250 MHz to 3.4 GHz. **Since the active feedback topology is used, no off-chip inductor is needed in either RFPGA, especially for the low-frequency band. Additionally, both RFPGA-V and RFPGA-I are able to handle maximum 4.4V peak-to-peak input signal without compromising their high operating bandwidth.** Two broadband RF front ends for direct sampling receivers, which include either RFPGA-V or RFPGA-I followed by the same gain buffer and RF filter, have been demonstrated. For the RF front-end with RFPGA-V, the measured gain, NF, IIP3 and IIP2 in the differential mode are 29.5dB, 5.2dB, -10.9dBm and 31.4dBm, respectively. With RFPGA-I, they are 30.5dB, 3dB, -

[0]This chapter is a partial reprint of the publication: Jie Fang, Chaoming Zhang, Frank Singor, Jacob Abraham, "A Broadband CMOS RF Front-End for Direct Sampling Satellite Receivers," has been submitted. I thank all the co-authors for their valuable advice in designing and testing of the prototype.

10.5dBm and 21.1dBm, respectively. Both RF front ends consume approximated 50 mW and occupy the similar area of 0.32 mm^2 in 28nm CMOS technology.

This chapter is organized as follows: Section 3.2 previously reported architectures of RFVGA/PGA. Section 3.3.1 describes the new architecture of RFPGA-V, develops a new gain interpolation scheme, discusses the design of an amplifier and a RF filter and a gain buffer, and then presents the measurement results. Section 3.4.1 focus on the second new architecture of RFPGA-I, discusses the design of the amplifier, and then presents the measurement results. Section 3.5 concludes this chapter.

3.1 Introduction

Fig. 2.10 shows a simplified block diagram of a direct sampling receiver. Right after an off-chip band-select filter, a RF programmable/variable-gain amplifier (RFPGA/VGA) conditions an incoming signal into a proper level, and then an anti-aliasing filter (AAF) restricts the folded noise and distortion from the LNA before digitization. A RFPGA/VGA is the critical block in the direct sampling receivers and needs satisfy many requirements over wide frequency range in modern broadband communication applications such as cable, terrestrial, satellite, cellular receivers. For example, the input signal spectrum spans very broad range from a few tens of MHz to 1 GHz in cable and terrestrial receivers [Gatta et al. [2009]][Lee et al. [2014]][Manstretta and Dauphinee [2007]][Kim and Kim [2006]][Xiao et al. [2007]][Im et al. [2010]][Greenberg et al. [2013]] and from hundreds of MHz to more than 2 GHz in satellite receivers [Fang et al. [2015]. As the front end of

a receiver, a RFPGA/VGA must provide broadband input impedance matching to provide good signal power transmission and to properly terminate the off-chip filter too.

A RFPGA/VGA is required to achieve low NF, high gain and large gain range with fine gain steps to condition an incoming signal into a proper level with sufficient SNR. A RFPGA/VGA provides high gain and low NF when the input signal is weak, whereas it should provide high attenuation when the input signal is strong. In addition, the modern communication systems usually adopt the digital modulation with a high number of constellations for high spectral efficiency. For example, the cable receivers uses as 16, 64, and 256 QAM modulation [DVBc2] and the satellite receiver uses QPSK, 8PSK, 16APSK, 32APSK modulation [DVBs2x]. Therefore, the fine gain step less than 0.5 dB is required for those modulation schemes to tolerate the noise burst without visible errors and to prevent upsetting the digital channel decoder.

A RFPGA/VGA is required to have high linearity as well. One of the difficult scenarios for input signals is that the desired channel could be presented with multiple interference channels while the power of the interference could be 30 or 40 dBc higher. Since the second-order inter-modulation distortion of the two in-band interferers in wideband receivers could possibly fall into the frequency range of the desired channel, the second-order input-referred intercept point (IIP2) is as important as the third-order input-referred intercept point (IIP3). In contrast, the narrowband receivers covering frequency bands where the ratio of maximum to minimum frequency is less than two do not significantly consider the IIP2 specification. Since

there are many channels spreading over the broad frequency range in wideband systems, composite second-order (CSO) and composite triple beat (CTB), where RF input signal is modeled by the multi-tones, are typically used to characterize the second-order and third-order intermodulation products, respectively. The CSO and CTB are the ratios expressed in dB of the power of the desired channel to the average power of the 2nd and 3rd distorted components centered at the frequency of the desired channel, respectively. As a matter of fact, the approximated relationship between the CSO and IIP2 and that between CTB and IIP3 are derived in [Matrix-TestEquipment].

In addition, it will be a desired feature that a RFPGA/VGA is able to receive a single-ended input signal. In the single-end mode, a RFPGA/VGA is able to perform a single-end-to-differential conversion, so an off-chip balun can be saved, and its insertion loss and its cost can be avoided as well. However, single-ended circuits usually suffer from common-mode rejection ratio (CMRR), power-supply rejection ratio (PSRR) and even-order distortions, which could cause in-band spurs and degrade the system performance especially in a complicated SoC environment. On the other hand, a RFPGA/VGA in the differential mode needs an off-chip balun, but usually has better CMRR, PSRR and even-order distortion.

This chapter presents comparative analysis for two new architectures for RFPGAs: voltage-mode RFPGA-V and current-mode RFPGA-I. RFPGA-V utilizes multiple-switch-multiple-amplifier configuration and the gain interpolation method to achieve a fine gain step of 0.25-dB over 42-dB gain range for the band of 250 MHz to 2.3 GHz. Meanwhile, RFPGA-I uses current steering method to

achieve a fine gain step of 0.25-dB over 42-dB gain range for even wider band of 250 MHz to 3.4 GHz. Both RFPGA-V and RFPGA-I are able to handle maximum 4.4V peak-to-peak input signal. Two broadband RF front ends for direct sampling receivers, which include either RFPGA-V or RFPGA-I followed by the same 6-dB gain buffer and RF filter, have been implemented. For the RF front-end with RFPGA-V, the measured gain, NF, IIP3 and IIP2 at maximum gain in the differential mode are 29.5dB, 5.2dB, -10.9dBm and 31.4dBm, respectively. With RFPGA-I, they are 30.5dB, 3dB, -10.5dBm and 21.1dBm, respectively. Both RF front ends consume approximated 50 mW and occupy the similar area of 0.32 mm^2 in 28nm CMOS technology.

3.2 Overview of State-of-the-Art Architecture OF RFVGA/PGA

As discussed in Section I, a RFVGA/PGA needs satisfy many specifications such as input impedance matching, NF, gain, programmable gain range, gain step, linearity, single-ended-to-differential conversion, PSRR, CMRR, etc. Meanwhile, the choice of RFVGA or RFPGA depends on the application requirements. RFPGA is conventionally not suitable for the receiver with the fine gain step of less than 0.5 dB, since it usually increases the hardware complexity and degrades the bandwidth due to its parasitics of switches and amplifiers. On the other hand, the requirement of fine gain step can be satisfied easily by filling the coarse gain step of the front attenuator with the fine gain step of VGA. However, when an incoming signal varies a lot and requires the gain change of more than the gain range of VGA, it would take a long time for Automatic Gain Control (AGC) loop to settle due to the slow

ramping of the control voltage in a RFVGA. In this section, several state-of-the-art architectures of RFVGA/PGA will be described, analyzed and compared.

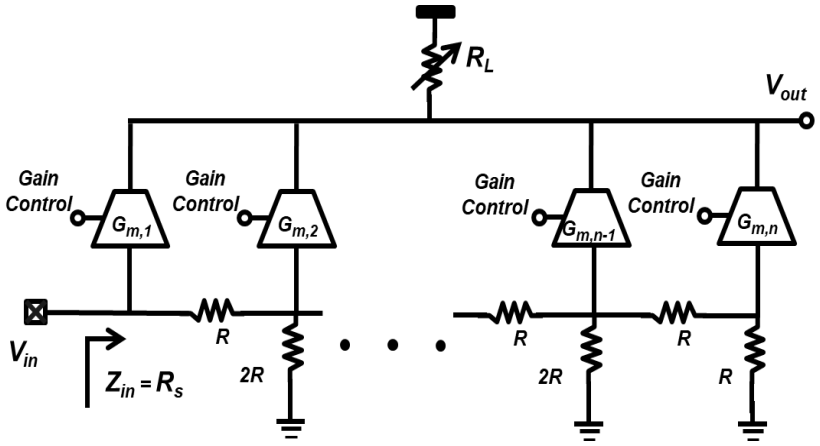

Figure 3.1: Block diagram of the RFVGA with a resistive attenuator.

The first RFVGA architecture is shown in Fig. 3.1 [Manstretta and Dauphinee [2007]][Mehr and et al [2005]]. The single-ended version is drawn for the simplicity, although it could be implemented in a differential version. An R-2R based attenuator provides 6-dB attenuation per stage along the resistive ladder and has good input impedance matching over broad frequencies. The multiple variable-gain amplifiers are connected along R-2R based attenuator. The gain control works as follows. At the maximum gain, only $G_{m,1}$ is turned on, the rest of G_m blocks are off. As gain decreases, the current gradually steers from $G_{m,1}$ to $G_{m,2}$. When all of current goes to $G_{m,2}$, 6-dB gain back-off is achieved. The same way can be applied to other adjacent G_m blocks to realize more gain attenuation. It is worth noting that the steering current needs change in a certain way to achieve dB-linear gain control characteristic by using Taylor's series approximation [Yamaji et al.

[2002]][Christopher [2000]][Liu et al. [2015]]. However, there are two main drawbacks of this architecture: the additional noise from the resistive attenuator results in noise figures greater than 3-dB. Secondly, it also suffers from bandwidth limitation due to excessive parasitics in the multi-amplifier configuration, especially for the large attenuation settings.

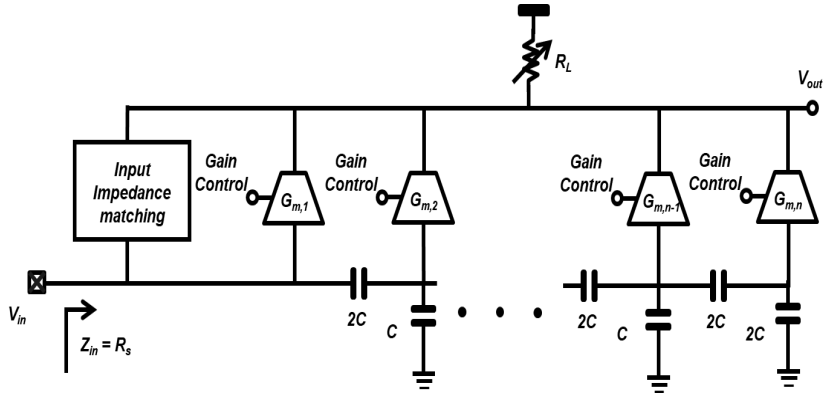

Figure 3.2: Block diagram of the RFVGA with a capacitive attenuator.

To overcome the two drawbacks mentioned above, two improved architectures in the following can be used. The first one [Kim and Kim [2006]][Retz and Burton [2003] uses a capacitive attenuator to replace the resistive attenuator, as shown in Fig. 3.2, so the noise penalty from R-2R attenuator can be avoided and low NF can be achieved. Since the capacitor value in the capacitive attenuator is chosen to have relatively high input impedance for the band of interest, the broadband input impedance matching is satisfied by the shunt-feedback path. However, excessive parasitics in the multi-amplifier configuration still limit its bandwidth.

Second improved architecture [Gatta et al. [2009]][Im et al. [2010]] has used a single amplifier with multiple switches configuration, as shown in Fig. 3.3.

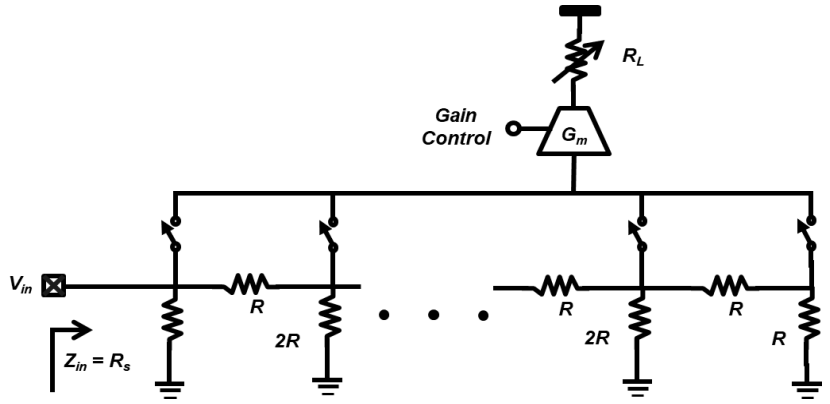

Figure 3.3: Block diagram of the RFVGA with a resistive attenuator and multiple switches.

Since the excessive parasitics from the multi-amplifier is avoided, this architecture is able to achieve higher bandwidth and take less area. The mismatch of different Gm blocks is avoided in this architecture as well. At the same time, the idea of using a capacitive attenuator for low NF and a shunt-feedback path for broadband input impedance matching can still be applied in this architecture too. However, the on-resistance of the tapping switch at V_{in} node results in somewhat NF degradation at the maximum gain setting.

It is worth noting that the above architectures use the voltage divider (R-2R ladder) to realize signal attenuation, which fall into the voltage-mode category. They require the amplifiers having a high input impedance to minimize their loading influence to the attenuator. The input impedance of amplifier along the voltage divider actually reduces the bandwidth of RFPGA/VGA. Fig. 3.4 shows another type of current-mode RFPGA/VGA architecture, which utilizes the current divider to realize signal attenuation [Im et al. [2010]][Mak and Martins [2011]]. The am-

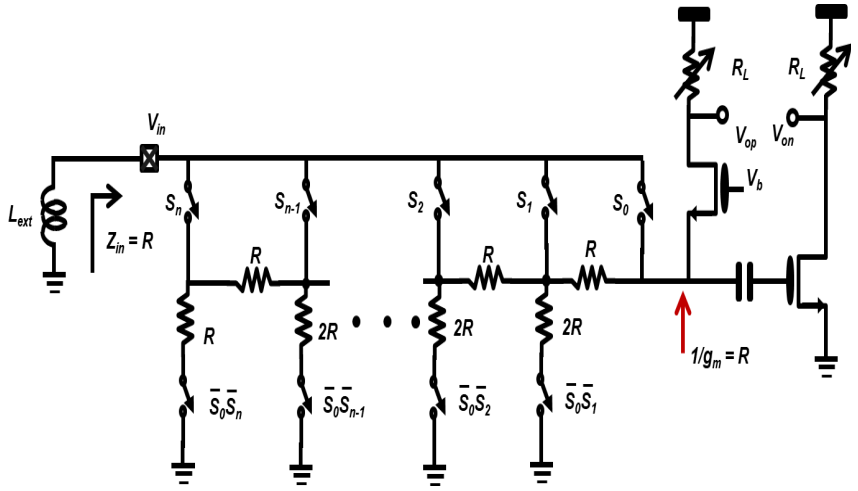

Figure 3.4: Block diagram of the current-mode RFPGA.

plifier includes a common-gate (CG) stage and a common-source (CS) stage, and the amplifier input impedance is mainly determined by the CG stage and equals to $1/g_m$ over a broad frequency range. Supposing $1/g_m = R$, the input impedance of amplifier then can be absorbed into the R-2R resistive attenuator. At the maximum gain mode, the R-2R resistive attenuator is switched off and the entire input signal is directly fed into the amplifier through the switch of S_0. In attenuation modes, the RF input is fed into the R-2R ladder via one of the switches ($S_1, S_2...S_n$), and the signal attenuation is realized by the divided signal current going to the CG stage. In addition, since only one of the switches ($S_0, S_1, S_2...S_n$) connecting to V_{in} node is turned on at different gain settings, the input impedance always equals to R and can be matched to the source impedance over wide frequencies.

There are several advantages in this architecture. Firstly, unlike previous architectures, the input impedance of amplifier is finite and absorbed by the at-

tenuator, which minimizes the loading influence to the attenuator resulting in a very broad frequency range. Then this amplifier can achieve single-to-differential conversion. The CS stage amplifies the input signal to the inverted output signal, while the CG amplifies the input signal with the same phase. Additionally, this architecture also achieves good NF due to noise canceling in the CG-CS amplifier [Blaakmeer and et al [2006]]. At the same time, the switch S_0 passes the signal current to the amplifier and causes little noise penalty. However, there are also several drawbacks of this architecture: firstly, an off-chip inductor is needed especially for low-frequency band. Then the non-ideal OFF switches among ($S_0, S_1, S_2...S_n$) might contribute considerable nonlinearity when the input signal amplitude is large at a high attenuation mode.

3.3 A Wideband RF Front-end with RFPGA-V

The RF front end in the section is designed for the direct sampling satellite receiver satisfying latest DVB-S2X standard. The receiver is required to achieve more than 40 dB gain range and a fine gain step of 0.25dB over the RF band from 250 MHz to 2.3 GHz. As discussed in Section II, a RFVGA is conventionally chosen to achieve this fine gain step for the hardware simplicity reason. However, since the input signal level can vary a lot in the satellite receiver application, a RFPGA with fine gain step is more desirable due to fast AGC loop settling time. In this section, a broadband voltage-mode RFPGA-V with a new gain interpolation scheme will be presented to satisfy the above requirements.

3.3.1 Architecture of RFPGA-V

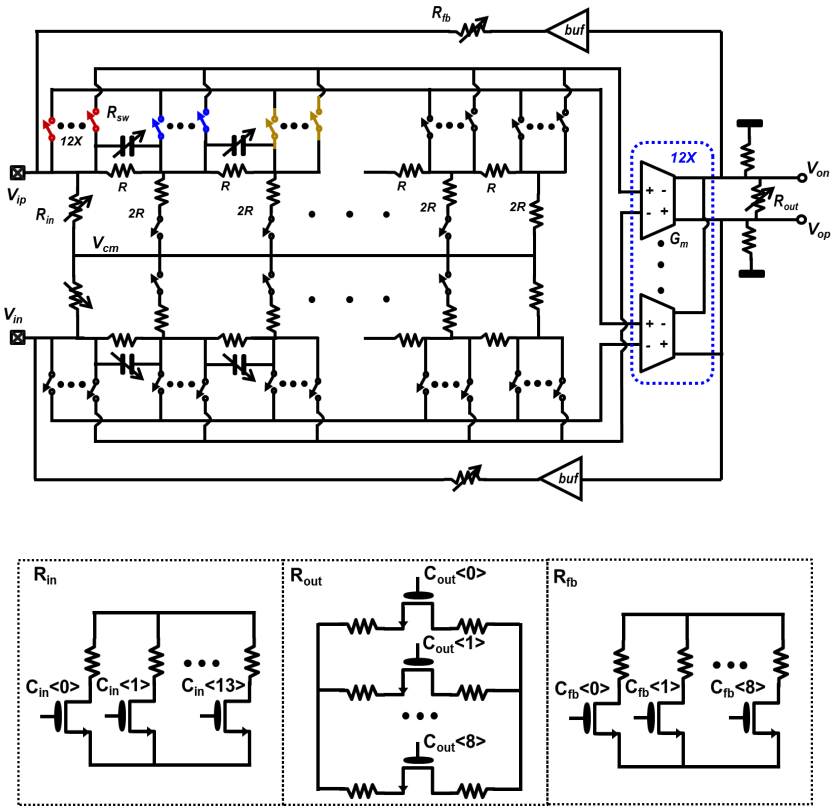

Figure 3.5: Block diagram of RFPGA-V with multiple switches and multiple amplifiers.

Compared with the multiple-amplifier configuration in Fig. 3.1 and the single-amplifier-and-multiple-switch configuration in Fig. 3.3, the proposed RFPGA-V of multiple switches and multiple amplifiers configuration, as shown in Fig. 3.5, can be considered as the hybrid version of both architectures. In this design, a 6-stage R-2R ladder provides total 36-dB attenuation range and 6-dB coarse gain steps. In each stage of R-2R ladder, 12 tapping switches connect between the ladder and the 12 amplifier units. In the maximum gain mode, all 12 amplifier units are

tapped to the first stage of attenuator. In 6dB back-off mode, all 12 amplifiers units are tapped to the second stage. Between the 6-dB coarse steps, the fine gain steps are realized through the new gain interpolation scheme as the follows.

In the 0.5-dB interpolation scheme, the 12 amplifier units are tapped to two adjacent stages in the ladder through the switches, as shown in Fig. 3.6 (a). For example: the configuration of 11 amplifiers tapped to the 1st stage in the attenuator and 1 amplifier tapped to the 2nd stage results in 0.37dB attenuation. The configuration of 10 amplifier slices tapped to the 1st stage and 2 amplifier slices tapped to the 2nd stage, leads to additional 0.39dB attenuation. This interpolation pattern can realize more gain steps until all 12 amplifier units are tapped to the 2nd stage of R-2R ladder. The fine gain step ranges from 0.37dB to 0.64dB. This interpolation scheme can also be applied to other two adjacent stages such as the 2nd and 3rd stage in the attenuator to generate fine gain steps.

In order to realize 0.25-dB gain steps, it is easy to think about increasing the number of the tapping switches and amplifier units from 12 into 24. The 24 amplifier units can be tapped to two adjacent stages in the ladder through the switches. However, this possible interpolation method would significantly increase routing parasitics, which reduces the RFPGA bandwidth. As a matter of fact, the new 0.25-dB interpolation scheme in this design is realized without extra hardware complexity compared with the 0.5-dB interpolation scheme. The 12 amplifier units now are tapped to three adjacent ladder stages through the switches. As shown in Fig. 3.6(b), the first two gain settings are same as those in the 0.5-dB interpolation scheme. The 3rd gain setting is different, where 11 amplifier slices tapped to the 1st

stage in the attenuator and 1 amplifier tapped to the 3rd stage of 12-dB attenuation. The 4th gain setting is again same as the 3rd gain setting in 0.5dB interpolation scheme. Therefore, this 0.25-dB interpolation scheme actually adds one more step between the adjacent steps in the 0.5dB interpolation scheme except the 1st gain step. It achieves the gain step ranging from 0.19dB to 0.37dB. This interpolation scheme can also be applied to other three adjacent stages such as the 2nd, 3rd and 4th stage in the attenuator to generate fine gain steps.

Normalized gain value	gain step (dB)
12 x 1 + 0 x 0.5 = 12.00	0.37
11 x 1 + 1 x 0.5 = 11.50	0.39
10 x 1 + 2 x 0.5 = 11.00	0.40
• • •	• • •
1 x 1 + 11 x 0.5 = 6.50	0.64
0 x 1 + 12 x 0.5 = 6.00	

(a)

Normalized gain value	gain step (dB)
12 x 1 + 0 x 0.5 + 0 x 0.25 = 12.00	0.37
11 x 1 + 1 x 0.5 + 0 x 0.25 = 11.50	0.19
11 x 1 + 0 x 0.5 + 1 x 0.25 = 11.25	0.20
10 x 1 + 2 x 0.5 + 0 x 0.25 = 11.00	0.20
10 x 1 + 1 x 0.5 + 1 x 0.25 = 10.75	0.21
• • •	• • •
1 x 1 + 11 x 0.5 + 0 x 0.25 = 6.50	0.34
1 x 1 + 10 x 0.5 + 1 x 0.25 = 6.25	0.35
0 x 1 + 12 x 0.5 + 0 x 0.25 = 6.00	

(b)

Figure 3.6: Illustration of the gain interpolation scheme (a) 0.5-dB gain step, (b) 0.25-dB gain step

Ideally, even finer gain step can be realized by tapping the 12 amplifier units to more than three adjacent ladder stages through the switches without extra hardware expense. However, the device mismatch and the parasitic mismatch limit the minimum possible gain step especially for high frequency in practice. Besides,

another trick to improve bandwidth is also used in this design. The feedforward capacitors are added along the resistive ladder to boost the bandwidth and can be switched on or off at different gain control codes, as shown in Fig. 3.3. It is worth noting that the tapping switches at the first stage have the largest size to minimize noise penalty from the switch on-resistance at the maximum gain setting; and the other tapping switches are progressively scaled down along the attenuator, which minimizes the parasitics to the resistive ladder for achieving wide bandwidth. Besides, the tapping switches at the first stage are thick-oxide NMOS devices, which allows RFPGA-V to tolerate maximum 4.4V peak-to-peak input signal reliably. The devices in the signal paths including the rest of tapping switches are all thin-oxide devices to reduce parasitics and achieve high operating frequency.

Besides the gain programmability at the RFPGA input, RFPGA output gain can be also programmed by varying the load resistor of Rout and the feedback resistor of R_{fb} to achieve additional 8-dB gain range. According to Fig. 3.3, the gain (G) and the input impedance (R_{in}) and noise figure (NF) for the gain programmability at the RFPGA output gain can be expressed in the following:

$$G = G_m R_{out} \tag{3.1}$$

$$R_{in} \approx \frac{R_{fb}}{G} = \frac{R_{fb}}{G_m R_{out}} \tag{3.2}$$

$$NF = 1 + \frac{R_{sw}}{R_s} + \frac{V_{in,gm}^2}{4KTR_s} + \frac{R_{out} + R_{fb}}{G_m^2 R_{out}^2 R_s} + \frac{V_{in,buf}^2}{G_m^2 R_{out}^2 4KTR_s} \tag{3.3}$$

where G_m is the total effective transconductor of the amplifier, $V_{in,buf}$ is the input referred noise of the buffer in the feedback path. Therefore, according to Eq. 3.2, Rout and R_{fb} change in a similar manner to keep the input impedance same for the different gain control codes at RFPGA output. Compared with the gain-NF relation for the input programmable gain where 1-dB gain attenuation causes 1-dB NF degradation, RFPGA output gain attenuation causes little NF degradation due to $G_m R_{out} >> 1$ according to Eq. 3.3. As a result, the system SNR can be further improved when the incoming signal is large enough to back off the RFPGA output gain.

As mentioned above, the broadband impedance matching for RFPGA output gain programmability is provided by the shunt feedback loop, where the input resistor ladder is switched off to minimize the noise penalty. As RFPGA gain decreases and the input attenuation start working, the input resistors R_{in} are gradually switched on to satisfy input impedance matching. As RFPGA gain decreases further where the input signal swing is fairly large, the feedback resistors Rfb are gradually switched off, otherwise, the large input current would inject into the buffer output in the feedback path and cause significant nonlinearity. The input impedance in the low-gain or attenuation mode is completely provided by the resistors R_{in}. For the large signal scenarios, the noise penalty from Rin has negligible impact to the system SNR.

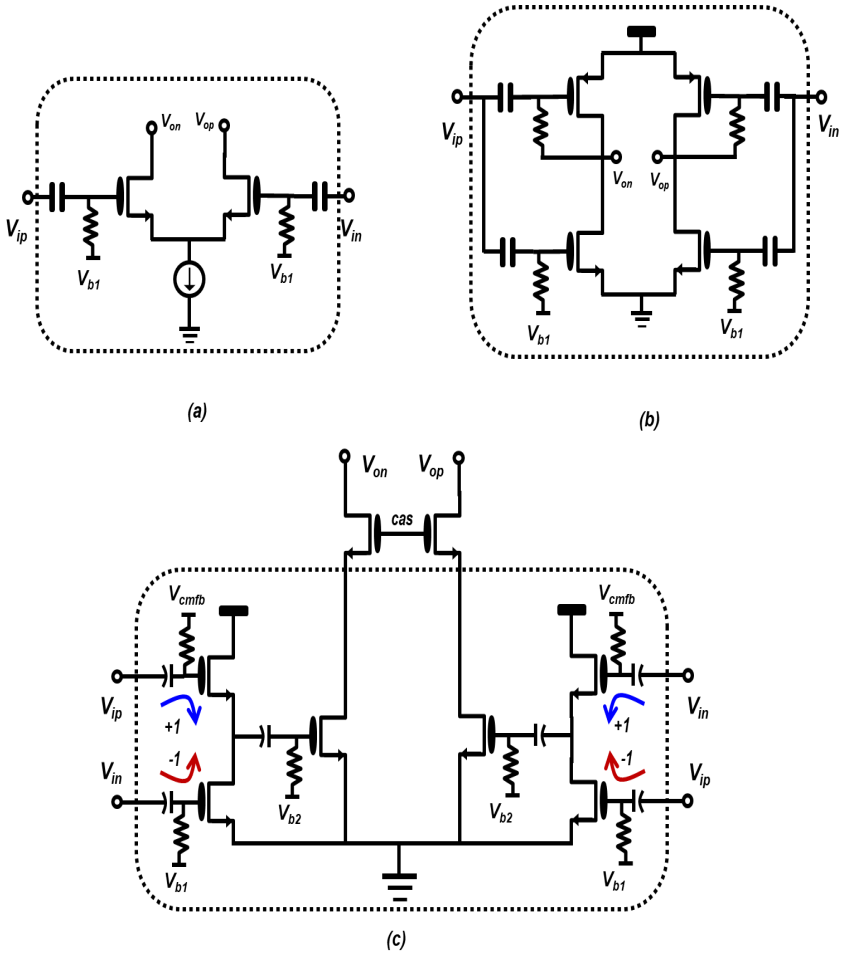

Figure 3.7: Diagram of the amplifier in RFPGA (a) input-pair amplifier, (b) inverter-like psudo-differential amplifier, (c) the proposed amplifier

3.3.2 Design of Amplifier

Fig. 3.7 shows several possible amplifier topologies used in RFPGAs. Fig. 3.7(a) is a fully differential input-pair amplifier, which is able to support both differential and single-ended input signal. For the single-ended mode, this amplifier topology can also work as a wideband active balun to perform single-ended-to-

differential conversion. However, there are two disadvantages for this topology in the single-ended mode. Firstly, the tail current is an additional noise source degrading NF. Secondly, the finite output impedance of the tail current can cause the signal leakage especially at the high frequency, which results in the phase and magnitude imbalance of this active balun. Another commonly used inverter-like amplifier is shown in Fig. 3.7(b). Its class AB structure, where both PMOS and NMOS provide trans-conductance, saves about half current. However, it is not suitable for the single-ended mode due to lack of a non-inverting path.

As shown in Fig. 3.7(c), the proposed amplifier in this design has two gain stages. The first stage has two signal paths: a non-inverting path of a source follower, and an inverting path of a common-source stage. Here the four NMOS transistors are chosen to be the same size, so the both paths have unity gain over a wide bandwidth. Particularly, in a single-ended mode, this stage can work as a broadband active balun to perform single-end-to-differential conversion with 6-dB gain without any off-chip inductor. Another advantage is that it is suitable to the low-voltage operation due to only two stacked transistor in this stage. It implies that applying more current at a low voltage supply to this stage, can achieve lower noise figure with less power penalty. The second stage of amplifier is a simple common-source stage and provides the majority of the gain. To be noted that the boxed part in Fig. 3.7(c), actually has 12 identical units, which are used for the gain interpolation scheme mentioned earlier.

3.3.3 Design of RF filter and Buffer

As shown in Fig. 2.10 , a gain buffer and RF filter follow the RFPGA/VGA in a direct sampling receiver. Although most of out-of-band contents are rejected by an off-chip filter, the out-of-band noise and distortion induced by RFPGA needs to be suppressed by an RF filter before digitizing the entire RF band. Otherwise, the RF front-end noise in the frequency above half of ADC sampling frequency (F_s) would be folded back to the band of interest and this noise folding equivalently causes 3-dB NF increase for the receiver. The RF filter in this design is required to provide 6-dB attenuation from the upper bound of the band of interest (F_{high}) to $F_s - F_{high}$, which results in less than 1-dB noise penalty due to the noise folding. At the same time, a fixed 6-dB gain is added in the next stage of RFPGA to reduce RFPGA output swing, which relaxes the linearity requirement for RFPGA. The gain buffer needs provide sufficient linearity performance to handle the full scale signal of ADC. As a result, the noise and linearity specifications of RF front end are separated into two different blocks of RFPGA and the gain buffer.

The detailed implementation of the gain buffer and RF filter is shown in Fig. 3.8(a). The gain buffer consists of two paths: a source follower and a common-source stage, which is same as the first stage of the amplifier in the RFPGA. The next stage is a 3rd-order elliptic LC filter, where a class-AB source follower is used to drive the LC filter for saving power consumption. The bias circuit for Vcmfb2 and Vcmfb2 in the push-pull source follower is realized by the common-mode feedback loop with the diode connected transistor M5 and M6 [Huijsing [2001]]. Besides, the input impedance of the next stage ADC, which can be modeled as a

parallel resistor and capacitor in the boxed part, is absorbed into the filter parameters to provide a low-pass response. The notch of filter can be tuned to provide sufficient attenuation, and the slight peaking from inductor compensates the gain roll-off from the proceeding stages. Fig. 3.8(b) shows the measured filter frequency response with three different bandwidth settings.

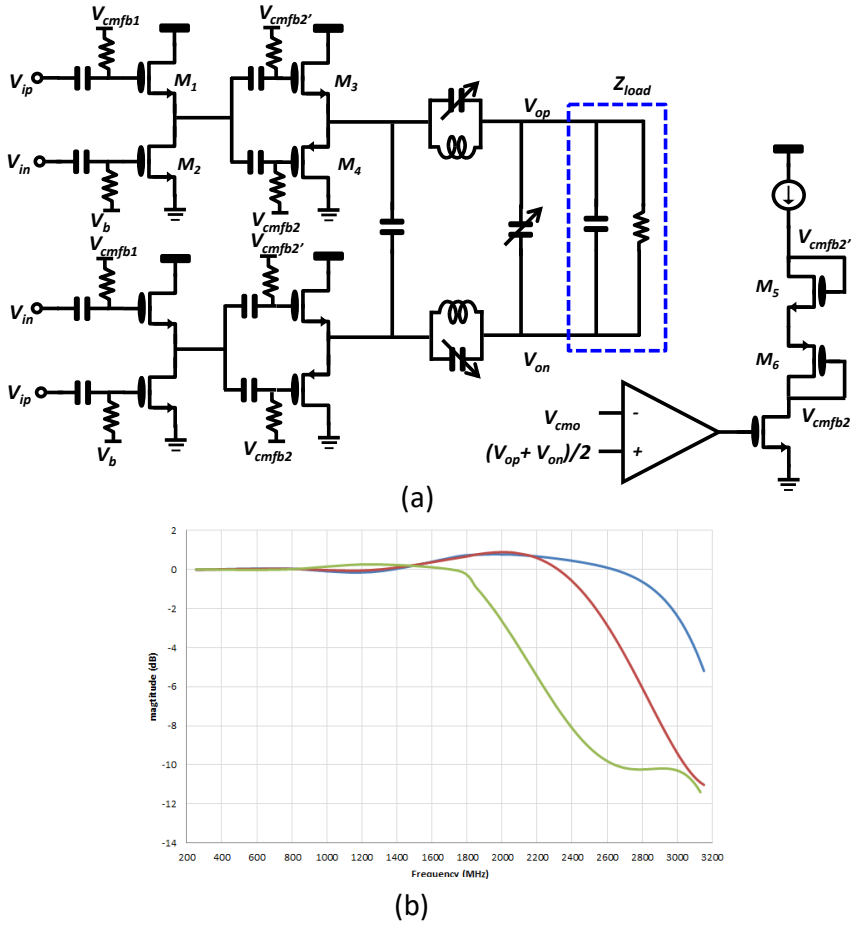

Figure 3.8: Gain buffer and RF filter (a) Simplified schematic; (b) magnitude response

3.3.4 Measurement results

The measurement results are shown in Fig. 3.9. The RF front-end achieves 42dB RF gain range with 0.25dB per step ranging from 250MHz to 2.3Hz. In the differential mode, the measured gain, NF, IIP3 and IIP2 at maximum gain setting are 29.5dB, 5.2dB, -10.9dBm and 28.4dBm, respectively. At the minimum gain, IIP3 and IIP2 are greater than 25.9dBm and 58.3dBm, respectively. As shown in Fig. 3.9, as LNA output programmable gain decrease, NF keeps almost flat; as LNA input programmable gain attenuates 1 dB, NF increases 1 dB. Besides, LNA gain decreases 1 dB, IIP3 improves 1 dB. It is worth noting that the measured non-uniform gain steps, which should be distinguished from the "wiggle-like" non-linearity in Fig. 2.5, do not degrade the system performance as long as the largest gain step would not cause excessive Amplitude Modulation(AM) error in the constellation plot during the gain change and gain steps are monotonic.

In the single-ended mode, an external 50-ohm resistor is added at the other side RF input, which will help reject the board noise pickup in the complicated SoC environment. The measured gain, NF, IIP3 and IIP2 at the maximum gain for this mode are 26.5dB, 8.2dB, -7.6dBm and 28.6dBm, respectively. The 3dB degradation for NF is due to that the noise sources effectively are doubled and the half-circuit in the differential circuits can no longer be used in the singled-ended mode for noise analysis. At the minimum gain, measured IIP3 and IIP2 are greater than 26.6 and 48dBm, respectively. The high IIP2 demonstrates the effectiveness of the circuit to convert single-ended signals to differential signals over wide frequency range.

This RF front end also has been tested in the direct sampling receiver with

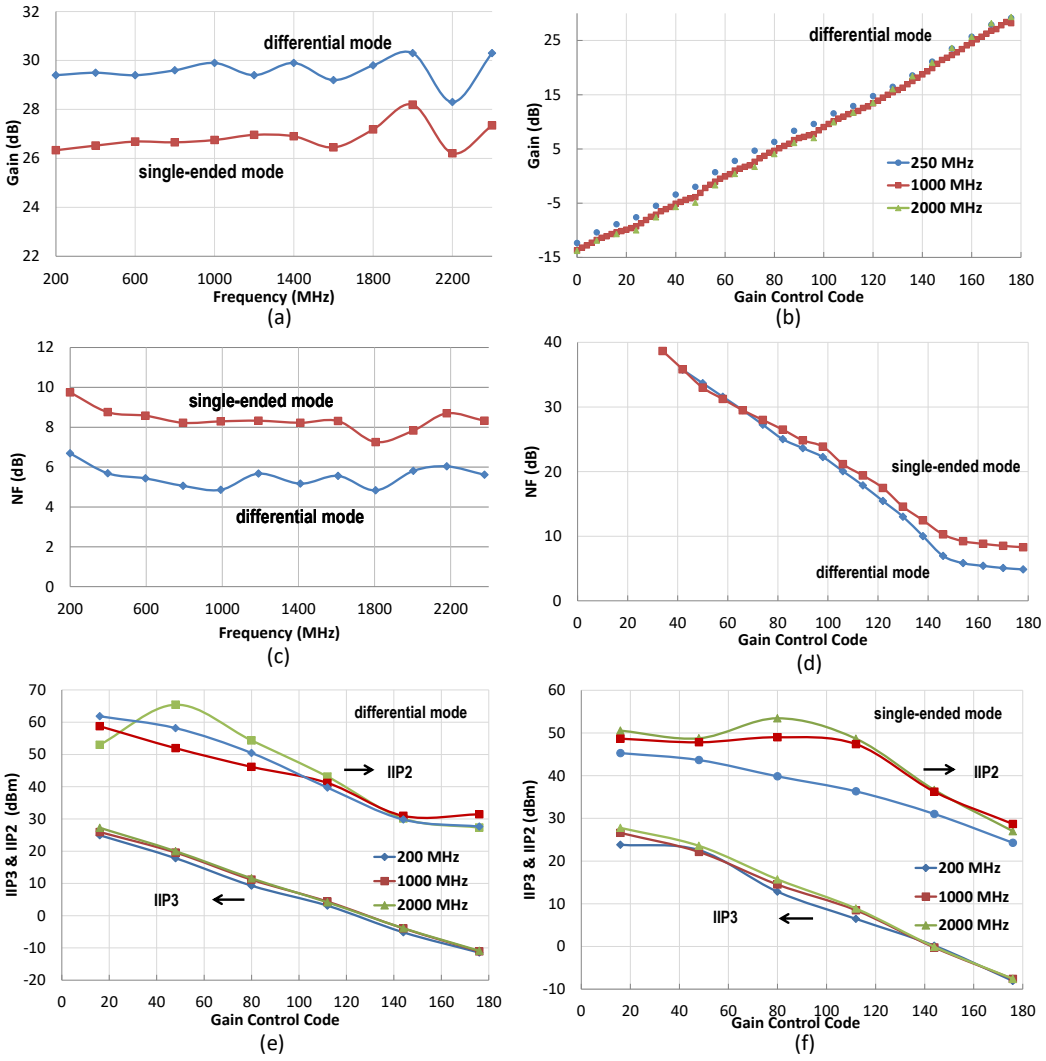

Figure 3.9: Measurement results (a) max gain; (b) gain programmability; (c) NF at max gain; (d) NF vs gain control code; (e) IIP3/ IIP2 vs gain control code in differential mode; (f) IIP3/ IIP2 vs gain control code in single-ended mode

a digital demodulation, as depicted in Fig. 2.10. Applying a -55dBm sinusoidal waveform to mimic the desired channel at 1255MHz and aggregated 30dB-higher adjacent channel interference (ACI) into the RF input, which is shown in Fig. 3.10,

system SNDR achieves 25.4dB at 30MHz symbol rate for 8PSK modulation. Moreover, sweeping the total input power up to 3 dBm with 30-dB ACI and 15-dB Peak-to-Average ratio (, which is equivalent to 4.4V peak-to-peak amplitude), the system SNDR remains the same, indicating that the RF front-end has high dynamic range.

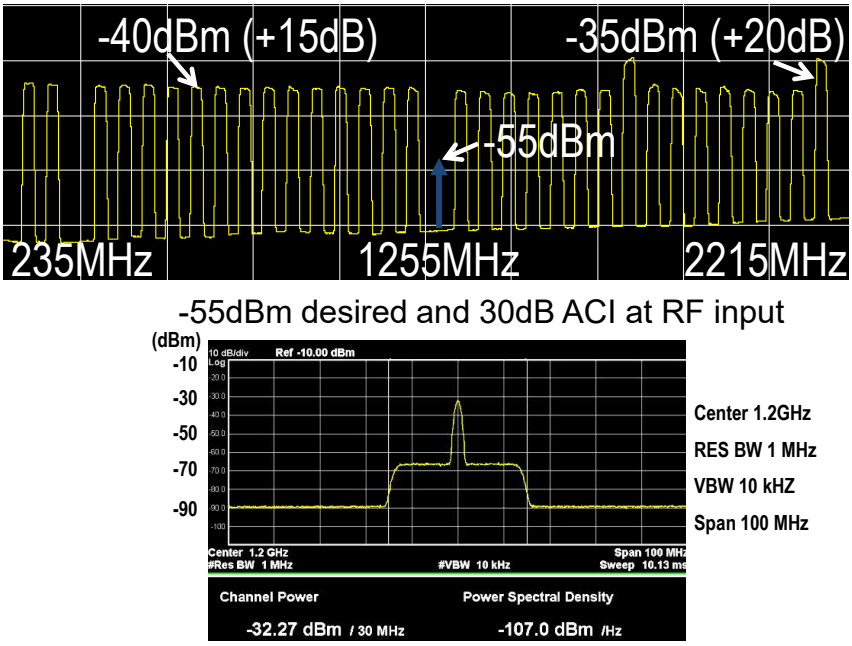

Figure 3.10: Measured SNDR with 30dB-higher ACI

Fig. 3.11 shows the micrograph of RF front end fabricated in 28nm CMOS process, occupying area of 0.32 mm^2. It only consumes 56mW from 1.3/1.8V supplies, while demonstrating a wide gain range with a fine step, a superior linearity and a low noise figure for a broad band.

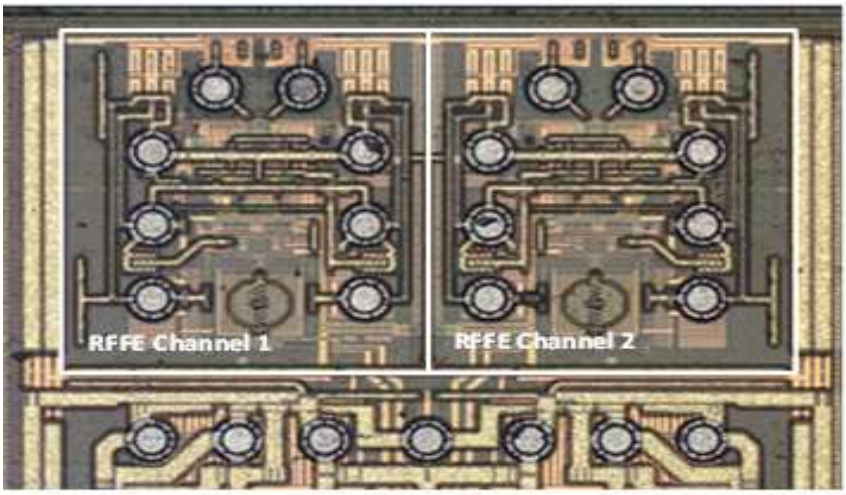

Figure 3.11: Die micrograph of RF front-end with RFGPA-V

3.4 A Wideband RF Front-End with RFPGA-I

As previously discussed, the amplifier input impedance along the attenuator limits the high frequency range in a voltage-mode RFGPA. In contrast, the amplifier input impedance can be absorbed by the attenuation and cause much less loading influence in a current-mode RFPGA, as shown in Fig. 3.4. In this session, new current-mode RFPGA-I achieving a fine gain step of 0.25-dB over 42-dB gain range for even wider band of 250 MHz to 3.4 GHz will be presented.

3.4.1 Architecture of RFPGA-I

As shown in Fig. 3.4.1, the proposed wideband current-mode architecture of RFPGA-I mainly composes of a resistive DAC and a trans-impedance amplifier (TIA). In the low-frequency band, the inductor is too larger to be integrated in a chip. Compared with the previous current-mode RFPGA architecture in Fig.3.4,

RFPGA-I uses a TIA to replace the combination of a CS stage and a CG stage for avoiding an off-chip inductor, especially in low-frequency band. At the maximum gain, the resistive DAC is bypassed by turning on switch S_0 and TIA provides broadband gain and input impedance matching. The input impedance is equal to R_o/A, where A represents the open-loop gain of the amplifier. At low-gain or attenuation mode, TIA provides a low-swing node for current summation. As a result, the signal attenuation is realized by steering the signal current from TIA input to the common node Vcm through the switches ($S_1, S_2...S_{12}$) in the resistive DAC. Since those switches ($S_1, S_2...S_{12}$) only handle small signal swing, they will not cause linearity degradation. Moreover, the bypass switch S_0 is turned off at the large attenuation mode, where a large input signal swing needs to be isolated from TIA input. In this design, a T-type switch is implemented for the switch S_0 to minimize the signal leakage to the TIA input due to parasitic capacitance which includes the switch Cds and the routing parasitic capacitance. The first switches connecting V_{ip} or V_{in} inside the T-type switch S_0 are the only thick-oxide devices in the signal path, so RFPGA-I is able to tolerate maximum 4.4V peak-to-peak input signals without compromising the 3.4 GHz operating frequency.

RFPGA-V used the gain interpolation scheme via multiple switches and multiple amplifiers in RFPGA-V for fine gain step of 0.25-dB over large gain range. In contrast, RFPGA-I utilizes a 12-b segmented resistive DAC, which composes of a 6-b binary resistor array and a 6-b R-2R ladder, for the similar function. The segmented architecture for the DAC, where R is chosen to a value close to the unity sheet resistance of a poly resistor, reduces the resistor spread leading to a small area

and good matching. It is worth noting that the resistor matching in the attenuator is not required to be 12-bit accuracy, since the most communication system usually allows a bit variation of the gain step as long as the gain monotonicity can be guaranteed.

In addition, similar to RFPGA-V, the output gain in RFPGA-I can be also programmed by varying the feedback resistor of R_o to achieve additional 8 dB gain range. The output gain back-off cause little NF degradation.

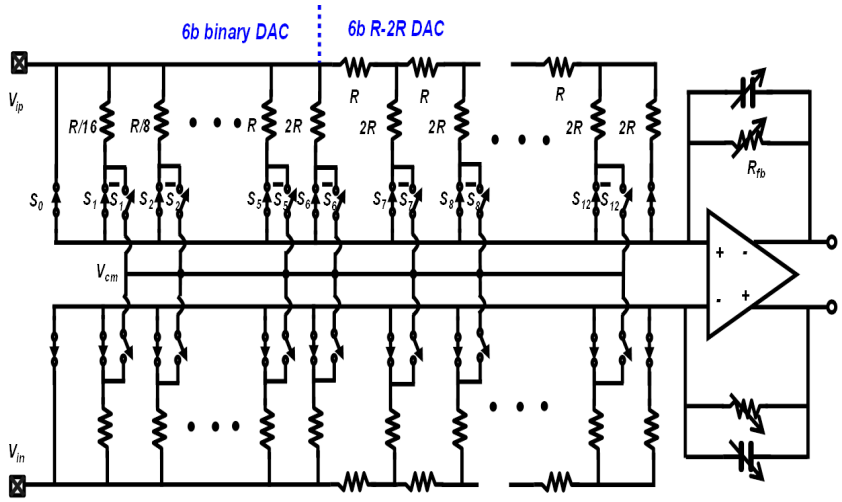

Figure 3.12: Block diagram of current-mode RFPGA-I.

For a clear illustration of RFPGA-I, the detailed analysis including the equivalent circuits for RFGPA-I at the different gain settings will be discussed in the following:

1) At the maximum gain setting, all the switches ($S_0, S_1 ... S_{12}$) in the input attenuator are turned on and the RFPGA equivalent circuits can be drawn in Fig. 3.13(a). The input impedance is mostly provided by the TIA, which is equal to

about R_o/A, where A represents the open-loop gain of the amplifier. Since the input impedance is a function of the gain of the amplifier, the input matching depends upon process and temperature as most of wideband LNA topologies do [Razavi [2010]]. In addition, the equivalent resistor value of 12-b resistive DAC and switch S_0 is small and the signal current entirely goes through them without any leaking path, so the input attenuator contributes little noise penalty. As a result, noise figure is mainly determined by the input equivalent noise of the amplifier. According to this feedback configuration, the maximum gain is simply determined by R_o/R_s, which has to be closed to the amplifier open-loop gain of A to satisfy the input impedance matching condition.

2) For the output gain programmability of RFPGA-I, gain and input impedance of TIA decrease with R_o. In this case, the input impedance is equal to the sum of the equivalent impedance of the resistive DAC and input impedance of TIA. In order to keep input impedance matching as gain decreases, the bypass switches S_0 are gradually turned off. At the minimum output gain setting, the equivalent circuit of RFPGA-I can be drawn in Fig. 3.13(b), where the output resistor becomes $R_o/2.5$ and switch S_0 in the input attenuator is completely switched off. Besides, since all signal current goes to the TIA input, noise figure only increases slightly.

3) For the input gain programmability of RFPGA-I, the input signal attenuation is realized by steering the signal current from TIA input to the common node V_{cm}. The equivalent circuit is shown in Fig. 3.13(c). The resistive DAC can be modeled by R_1 and R_2, where R_1 represents the path of the input signal current flowing to TIA input and R_2 represents the path of the input signal current flowing

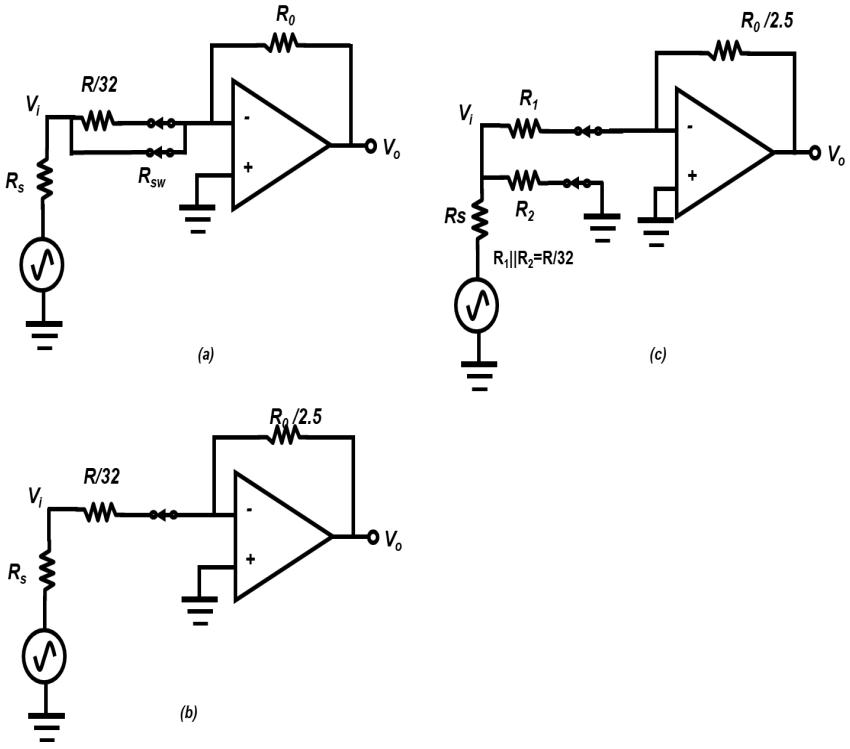

Figure 3.13: RFPGA-I equivalent circuits (a) at the maximum gain; (b) at the minimum output gain; (c) at input gain back-off.

Table 3.1: Parameters summary for different gain settings of RFPGA-I

Gain setting of RFPGA-I	Gain	R_{in}	β	NF
Max gain	$\frac{R_o}{R_s}$ or A	$\frac{R_o}{A}$	$\frac{R_0}{R_s+R_o}$	$1+\frac{R_s}{R_o}+\frac{R_{in,a}^2}{4KTR_s}$
Min output gain	$\frac{R_o/2.5}{R_s}$ or A/2.5	$\frac{R}{32}+\frac{R_o}{2.5A}$	$\frac{R_s+R/32}{R_s+R/32+R_o/2.5}$	$1+\frac{R/32}{R_s}+\frac{R_s}{R_o/2.5}+\frac{R_{in,a}R_s}{4KT(R_s+R/32)^2}$
Input gain back-off	$\frac{R_o/2.5A}{R_1+R_o/2.5A}$	$R_2\|\|(R_1+\frac{R_o}{2.5A})$	$\frac{R_s\|\|R_1+R_2}{R_s\|\|R_1+R_2+R_o/2.5}$	approx. dB-by-dB increase as input gain decreases

to the common node V_cm. Therefore, the signal attenuation is determined by the ratio of R_1 and R_2 and the resistance of R_1 and R_2 in parallel is equal to R/32. Since the signal is attenuated at the input, 1-dB attenuation causes 1-dB NF degradation in this case.

From these equivalent circuits in Fig. 3.13, gain (G) and input impedance (R_{in}) and loop feedback ratio (β) and noise figure (NF) of RFPGA-I at the different gain settings has been derived and summarized in Table 3.1. Taking the example of the equivalent circuit in Fig. 3.13(c), where the input gain of RFPGA-I is programmed, R_in and V_o can be expressed as:

$$R_{in} = R_2||(R_1 + \frac{R_o}{2.5A}) \approx R_s \tag{3.4}$$

$$V_o = -\frac{V_i}{R_s}\frac{R_2}{R_2 + R_1 + \frac{R_o}{2.5A}}\frac{R_o}{2.5A} \tag{3.5}$$

From equation Eq. 3.4 and Eq. 3.5, gain can be expressed as:

$$G = \frac{V_o}{V_i} = \frac{-1}{R_s(R_1 + \frac{R_o}{2.5A}}\frac{(R_1 + \frac{R_o}{2.5A})R_2}{R_2 + R_1 + \frac{R_o}{2.5A}}\frac{R_o}{2.5A} = -\frac{Ro/2.5A}{R_1 + R_o/2.5A} \tag{3.6}$$

From Table 3.1, many important insights for RFPGA-I can be obtained. Listed in column R_{in}, RFPGA-I input impedance is a function of the open-loop gain of the amplifier for different gain settings. Therefore, a high-speed amplifier is required to keep input impedance matching over wide bandwidth. Then, according to the column β, feedback factor of this shunt feedback structure increases as the

gain decreases. When RFPGA-I in the setting of the output gain programmability, the feedback factor is small and the loop stability can be easily achieved. Then the feedback factor goes to maximum for the minimum gain setting, where the loop stability needs to be carefully checked. Besides, from the column NF, noise figure keeps relatively constant for the output gain programmability due to small value of R_s/R_o, where $V_{in,a}$ is the input referred noise of the amplifier. The noise figure expression for the input gain programmability is a little lengthy and not listed in Table I, but basically 1-dB gain attenuation at the input causes 1-dB NF degradation.

3.4.2 Design of Amplifier

The schematic of high-speed amplifier used in RFPGA-I is shown in Fig. 3.14. This amplifier includes two stages: the first stage is an inverter-based class-AB CS amplifier, which provides the most of gain in the amplifier. Since the low-band of this application is at 250-MHz instead of DC, a simple diode-connected PMOS through a resistor is used for its common-mode biasing. The second stage is the combination of a source follower and a common-source stage, same structure as the gain buffer in Fig. 3.8. It provides additional several-dB gain, and drives the feedback resistor array of R_{fb} and the next gain-buffer stage.

In term of the frequency response of this two-stage amplifier, the dominate pole is at its first stage output due to the high output impedance of CS stage. The small capacitance at the first stage output pushes the dominate pole to a high frequency. The non-dominate pole is at its second stage output due to the small output impedance of source follower. Since this topology separates the heavier loading

from the high output impedance of the first stage, it achieves wider bandwidth, compared with the one-stage inverter-based CS amplifier in Fig. 3.7(b). In addition, since this is a two-pole system, the loop stability needs to be carefully checked, especially at the minimum gain setting, where the feedback factor of RFPGA-I is maximum according to Table 3.1.

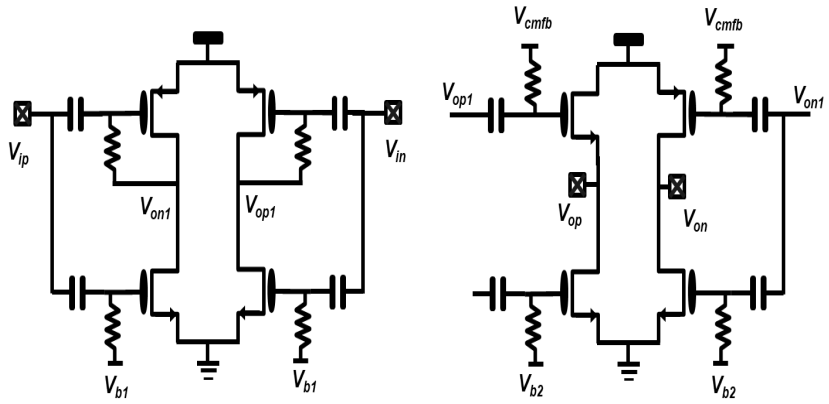

Figure 3.14: Schematic of the amplifier in RFPGA-I.

3.4.3 Measurement results

The RF front end with RFPGA-I is designed for the direct sampling satellite receiver as well. The following stage of the anti-alias filter and gain buffer in subsection 3.3.2 is re-used here. The measurement results are shown in Fig. 16. The RF front-end with RFPGA-I extends the high band to 3.4 GHz. It achieves 41dB gain range with 0.25-dB per step. The measured S11 is less than -10dB from 100 MHz to 3.4 GHz. The measured gain, NF, IIP3 and IIP2 at the maximum gain are about 30dB, 3dB, -10.5dBm and 21.1dBm, respectively. IIP3 and IIP2 are greater than 30dBm and 58.2dBm at the minimum gain setting, respectively. Both IIP2 and

IIP3 improve 1dB as LNA gain decreases 1dB. RFPGA-I achieves better noise performance at the maximum gain setting than RFPGA-V for two reasons: no tapping switches and higher gain in the first stage of amplifier.

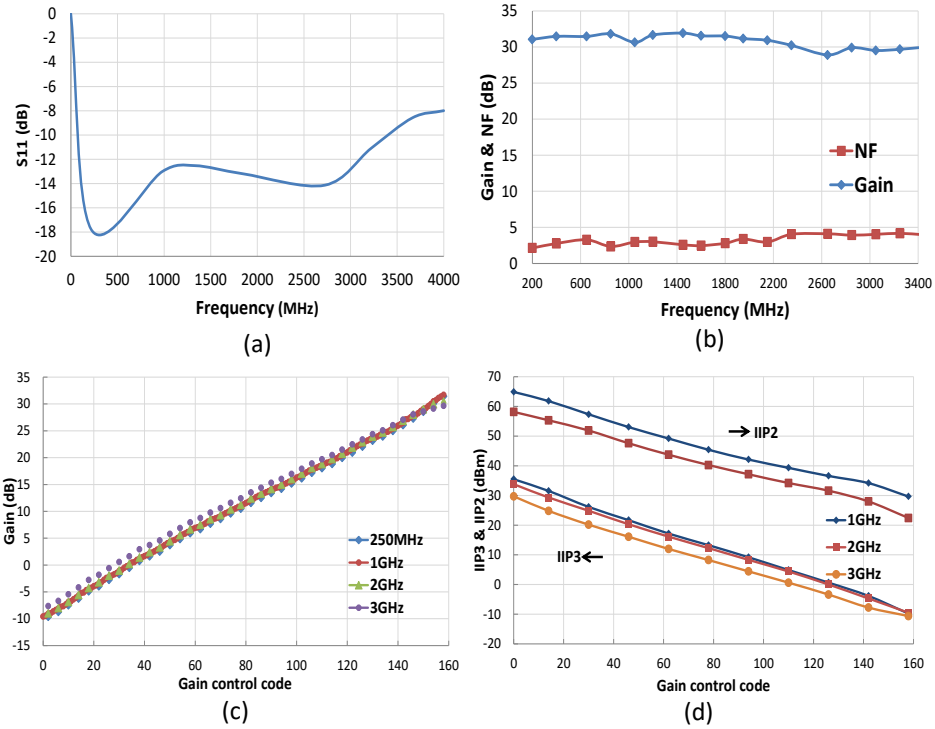

Figure 3.15: Measurement results (a) S11; (b) max gain and NF at max gain; (c) gain programmability; (d) IIP3 & IIP2 vs gain control code.

Fig. 3.15 shows the micrograph of the front end with RFPGA-I fabricated in 28nm CMOS process. The left part is the RF front end and the right part is the testing buffer, which connects the output of RFPGA-I. In order to reuse the testing board, the ball configuration is kept same as the RF front end in section III. The area of the RF front end is limited by the balls and is 0.32 mm^2. It only consumes 50mW from 1.2/1.8V supplies, while demonstrating a fine gain step of 0.25-dB over 41-dB

Table 3.2: Measured performance summary and comparison with state-of-the-art

Parameters	This work with RFPGA-V	This work with RFPGA-I	Murphy et al. [2015]	Greenberg et al. [2013]	Im et al. [2012]	Mak and Martins [2011]
Frequency (MHz)	200-2300	200-3400	200-3300	40-1002	48-860	170-1700
Diff/balun	diff/balun	diff	diff/balun	balun	diff	balun
Gain step (dB)	0.25	0.25	NA	1	0.25	6
Gain range (dB)	42	42	fixed gain	51	58	18
NF @ max gain (dB)	5.2	3	1.7	3	6	4
IIP3 @ max gain (dBm)	-10.9	-10.5	NA	-13	-13	-3.4
IIP2 (dBm)	28.4	21.1	NA	20	NA	32
Receiver architecture	Direct sampling	direct sampling	single-conversion	single-conversion	single-conversion	single-conversion
External inductor for LNA	N	N	N	Y	N	Y
Power [mW]	56	50	36-62	113	115.2	55
Area [mm^2]	0.32	0.32	5.2	5.6	NA	0.57
Technology	28nm	28nm	28nm	80nm	180nm	65nm

gain range in the band of 200 MHz to 3.4 GHz.

Table 3.2 is summary of the front end performance in comparison with the state-of-the-art. Both presented RF front-ends in this chapter show fine gain step, large gain programmability, and low noise over wide frequency range and occupy a small area. Thanks to the high bandwidth of the current steering, RFPGA-I has wider frequency range than RFPGA-V. Meanwhile, it is convenient to use gain in-

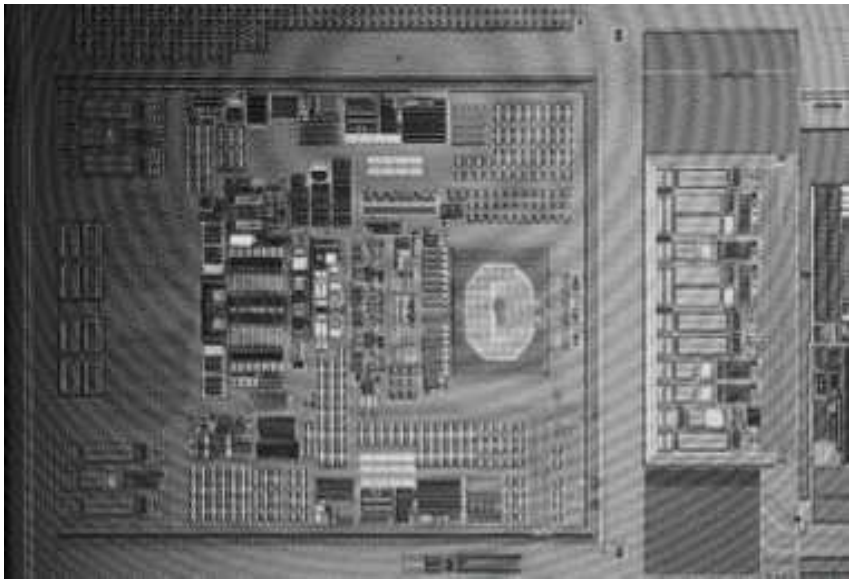

Figure 3.16: Die micrograph of RF front-end with RFGPA-I.

terpolation for RFPGA-V to realize even finer gain step for relatively low frequency applications, as discussed in **??**. Therefore, either RFPGA-V or RFPGA-I could be a better candidate for different applications. Besides, no off-chip inductor is needed in either RFPGA-V or RFPGA-I.

3.5 Conclusion

This paper presents comparative analysis between two new architectures of RFPGAs: voltage-mode RFPGA-V and current-mode RFPGA-I. RFPGA-V utilizes multiple-switch-multiple-amplifier configuration and gain interpolation method to achieve a fine gain step of 0.25-dB over 42-dB gain range from 250 MHz to 2.3 GHz. Meanwhile, RFPGA-I uses current steering approach to achieve a fine gain step of 0.25-dB over 41-dB gain range for even wider frequency range from 250

MHz to 3.4 GHz. In addition, both RFPGA-V and RFPGA-I are able to handle maximum 4.4V peak-to-peak input signal. The presented broadband RF front-end with either RFPGA-V or RFPGA-I significantly simplifies hardware complexity and reduces the power consumption.

Chapter 4

High-speed Time-interleaved SAR ADC

This chapter presents a 5-GS/s 12-way 10-b time-interleaved SAR ADC for direct sampling receivers. Proper signal and clock distribution along the multiple channels are utilized to mitigate inter-channel bandwidth and timing mismatches. A digitally-assisted calibration is introduced to remove the inter-channel offset, gain and timing mismatch. The T-type bootstrapped sampling switches minimize the inter-channel crosstalk among top-plate sampling SAR channels and the signal-dependent leakage current during SAR conversion cycles. The power efficiency of this ADC is significantly improved by many design techniques. The merged capacitor switching algorithm leads to high switching efficiency and smaller area. The modified reference voltage scheme optimizes input common-mode voltage of the comparators. The optimal sub-radix-2 CDAC results in low-power reference buffers and higher conversion speed. This ADC achieves 49 dB SNR, 52 dB THD and 42 dB SNDR up to Nyquist frequency at 5 GS/s, consumes 76 mW from 1 V supply, and occupies 0.57 mm^2 in 28 nm CMOS technology. The implemented ar-

[0]This chapter is a partial reprint of the publication: Jie Fang, Shankar Thirunakkarasu, Xuefeng Yu, Fabian Silva-Rivas, Chaoming Zhang, Frank Singor, Jacob Abraham, "A 5GS/s 10b 76mW Time-interleaved SAR ADC in 28nm CMOS," IEEE Transactions on Circuits and Systems I: Regular Papers vol. 64, no. 7, pp. 16731683, July 2017. I thank all the co-authors for their valuable advice in designing and testing of the prototype.

chitecture also demonstrates high scalability to advanced CMOS technology nodes and has even higher power efficiency potential.

This chapter is organized as follows: an introduction of existing high speed SAR ADC design techniques is first presented. The proposed SAR ADC architecture is shown next. Finally, the detailed prototype ADC implementation and measurement are presented.

4.1 Introduction

A low-noise amplifier (LNA) amplifies the incoming signals, passes it to an anti-aliasing filter (AAF) which restricts the out-of-band content, such as LNA noise and distortion. The properly conditioned signal is then sent to a wideband ADC that digitizes the entire spectrum from DC to Nyquist, where channel selection and demodulations can be performed efficiently in the digital domain. The architecture creates a great challenge to the dynamic range requirements of the ADC. As shown in Fig. 4.1, the ADC dynamic range should be large enough to handle the undesired blockers, the peak-to-average ratio (PAR), and still satisfy the signal-to-noise ratio (SNR) requirement for a communication system. It is worth noting that in the SNR calculation, the noise should be integrated over the channel bandwidth instead of the entire Nyquist band.

Time-interleaved (TI) ADCs are popular architectures that satisfy multi-GS/s and high-resolution requirements in recent literatures [Doris et al. [2011]][Stepanovic and Nikolic [2012]][Janssen et al. [2013]][Dortz et al. [2014]][Fang et al. [2015]][Sung et al. [2015]][Hong et al. [2015]][Sahoo and Razavi [2013]][Wu et al. [2013]][Bran-

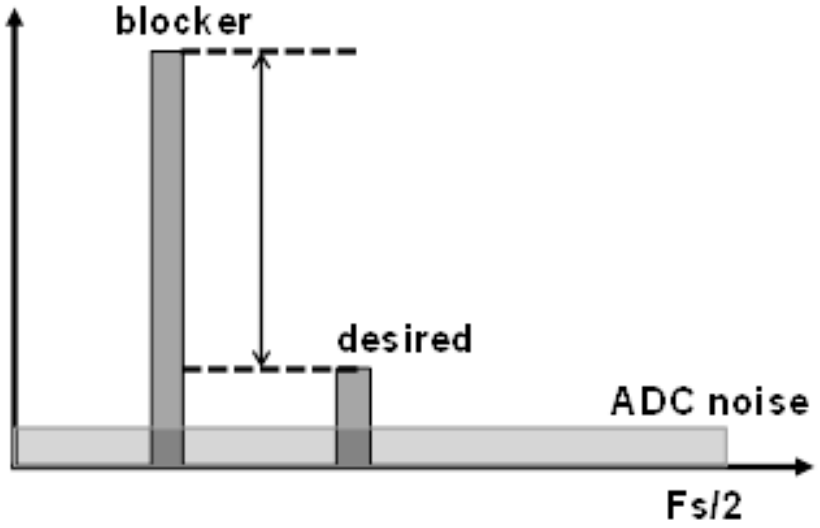

Figure 4.1: Requirement of ADC dynamic range.

dolini et al. [2015]]. It is well known that inter-channel timing, bandwidth, offset, gain and linearity mismatches generate undesired artifacts, which limit the performance of TI ADCs. In order to mitigate those non-ideal effects, proper clock and signals distribution to all sample/hold (S/H) circuits in ADC channels and digitally-assisted calibration schemes are needed. In addition, linearity and clock jitter at high frequency are also critical limits for high-speed ADC performance. Especially when the incoming signal has a fully loaded spectrum, significant broadband noise due to clock jitter and broadband distortion due to circuit nonlinearity are generated, both of which are strongly dependent on the spectral power at higher frequencies.

In terms of individual ADC channels in high-speed TI ADCs, successive approximation register (SAR) ADCs [Doris et al. [2011]][Stepanovic and Nikolic [2012]][Janssen et al. [2013]][Dortz et al. [2014]][Fang et al. [2015]][Sung et al.

[2015]][Hong et al. [2015]][Sahoo and Razavi [2013]][Wu et al. [2013]] and pipelined ADCs [Wu et al. [2013]][Brandolini et al. [2015]][van der Goes et al. [2014]] are the two main structures. Pipelined ADCs generally provide higher resolution, but SAR ADCs with digital calibration for capacitor mismatches can achieve high resolution as well [Stepanovic and Nikolic [2012]][Inerfield et al. [2014]][Chang et al. [2013]]. Thanks to their digital-friendly nature, SAR ADCs are superior in aspects of power efficiency and are highly scalable to an advanced CMOS technology [Hariprasath and et al [2010]][Liu et al. [2010]][Inerfield et al. [2014]][Chang et al. [2013]]. First, as supply voltage shrinks in advanced technologies, the small signal swing requires a large sampling capacitance to achieve high SNR at the expense of large current consumption. However, due to no closed-loop circuit in S/H circuits, SAR ADCs can easily accommodate high-swing signals, which means a smaller sampling capacitance is sufficient for a high SNR. In addition, capacitance matching and density also improve continuously with the evolution in technologies. Further, the small sampling capacitance for TI ADCs also reduces the overhead in distributing the sensitive incoming signals to all channels and increases the bandwidth of the analog front-end buffer. In addition, digital SAR logic benefits dramatically in terms of speed, area and power with technology scaling. On the other hand, in order to improve the speed of SAR ADCs, some papers [Hong et al. [2015]][Chan and et al [2012]][Kull et al. [2013]] used multiple comparators and multiple reference voltages to determine 2 or 3 bits per conversion cycle at the cost of power consumption for each channel which reduces the number of channels and simplifies the time-interleaved S/H networks. After all, SAR ADCs achieve high

power efficiency and low cost, therefore they are very popular choices for TI ADCs in advanced CMOS technologies.

In this work [Fang et al. [2015]], a 12-channel 10b time-interleaved SAR ADC is demonstrated. The inter-channel offset, gain, bandwidth and timing mismatches in the TI ADC are mitigated by both careful signal and clock distribution along the multiple SAR channels and an elaborate digitally-assisted calibration method. The issues in the sample/hold network (S/H) such as the inter-channel crosstalk and the signal-dependent leakage current during SAR conversion cycles are eliminated by T-type bootstrapped sampling switches. In order to improve the ADC power efficiency, many design techniques are applied. First, the merged capacitor switching algorithm leads to high switching efficiency and small area. Then an optimized reference voltage scheme reduces the common-mode voltage of the PMOS-input pair in comparators to achieve high speed and low noise. Further, the sub-radix-2 CDAC is optimized not only to provide robustness for SAR conversions, but also results in low-power reference buffers and higher conversion speed. The measurement shows that this ADC achieves 49dB SNR, 52dB THD and 42dB SNDR up to Nyquist frequency at 5GS/s, consumes 76mW from a 1V supply, and occupies $0.57mm^2$ in 28nm CMOS technology.

4.2 TI ADC Architecture

The overall architecture of the 12-way TI synchronous SAR ADC is shown in Fig.4.2. In the ADC, an input signal is distributed to the 12 SAR channels via an on-chip input buffer in order to limit kickback noise back to the RF front end.

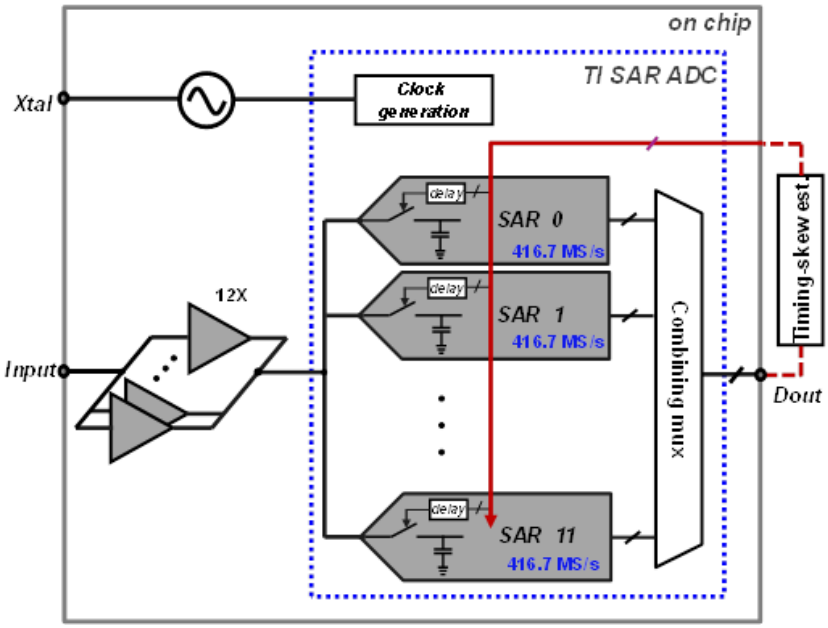

Figure 4.2: Overall architecture.

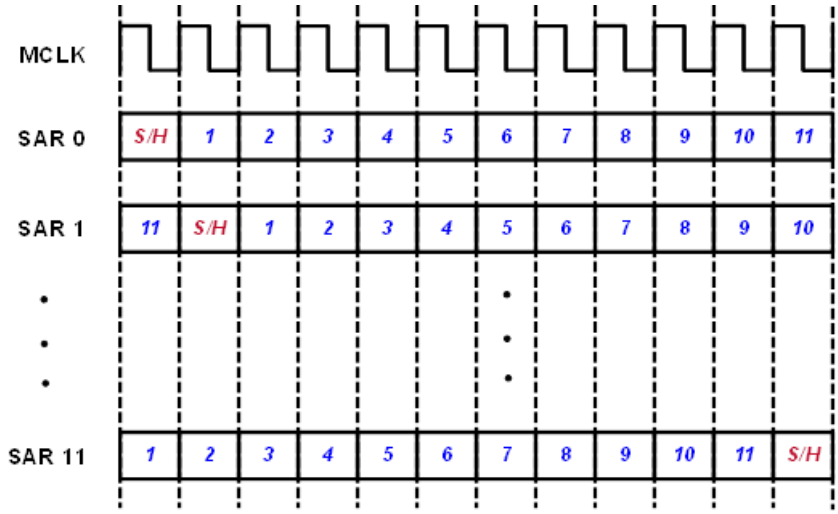

Figure 4.3: Timing diagram of the TI ADC.

The input differential signal has a maximum swing of 1.2 V peak-to-peak, which is limited by the input buffer with 1.0 V power supply. The input buffer has 12 parallel units, whose layout pitch matches that of the individual SAR channel for easy signal distribution along the SAR arrays with good inter-channel matching. Each SAR channel converts data at the speed of 416.7 MS/s; the 12-way interleaved channel results in the 5 GS/s conversion rate. An on-chip digital calibration engine for each ADC channel removes gain and offset mismatches, and realizes the non-binary to binary mapping on the output data. The inter-channel timing mismatch is estimated offline, and then corrected by tuning the programmable delay of the sampling clock in each ADC channel. Lastly, a combining multiplexer selects 12 channel outputs in a rotated manner and outputs data with a decimation ratio of 13. Therefore, the complete sampled spectrum is folded on 1/13th of the Nyquist frequency, which allows measuring all spectral artifacts of the converter and overcomes the data acquisition speed limitation of the setup.

The timing diagram of this TI ADC is described in Fig. 4.3. First, a single 5 GHz master clock is generated from an integer PLL with low jitter [Shen et al. [2013]]. The clock generation block, which mainly consists of barrel shifters, receives the master clock and then generates 12 clocks with phases 0, 30, 60 ..... 330. Each of 12 clocks operate at 416.7 MHz with a duty-cycle of 1/12, triggers each individual SAR channel to sample and hold the input signal at equally spaced time instants, thus the 12-way interleaved operation is realized. Further, each SAR channel also uses 12 master clock cycles: one for S/H and eleven for bit conversion, and outputs 11b data every 12 cycles. The SAR conversion steps are all synchronous to

a single 5 GHz master clock for the simplicity of the SAR logic.

4.3 Sample/Hold Network

4.3.1 S/H Issues in the TI ADC

In this work, a top-plate sampling SAR ADC is used in each channel. As shown in Fig. 4.4, the S/H network in this TI ADC consists of the input buffer array, a sampling switch and the sampling capacitors in each SAR channel. Several issues in the S/H network should be carefully considered here. First, the signal-path mismatch from the buffer input to each SAR channel will cause bandwidth and phase mismatch, which degrades ADC performance. Proper signal distribution along the channels is needed. Second, the crosstalk among the top-plate nodes of the sampling capacitors could cause sampling errors in each SAR channel during the S/H cycle, and conversion errors in the other channels. Third, the leakage current of the sampling switch leaks the hold charge of the CDAC during conversion cycles, leading to conversion error. In addition, the nonlinear input capacitor of the comparator could cause THD issue, since the nonlinear capacitor ”takes away” or ”inject” a portion of the charge that are nonlinearly dependent to the comparator input during SAR conversion.

4.3.2 Input Buffer

The single-ended version of input buffer is shown in Fig.4.5, although the actual implementation is a differential version. It consists of 12 parallel units, and each unit has dual signal paths: the main path of source follower stage, and the

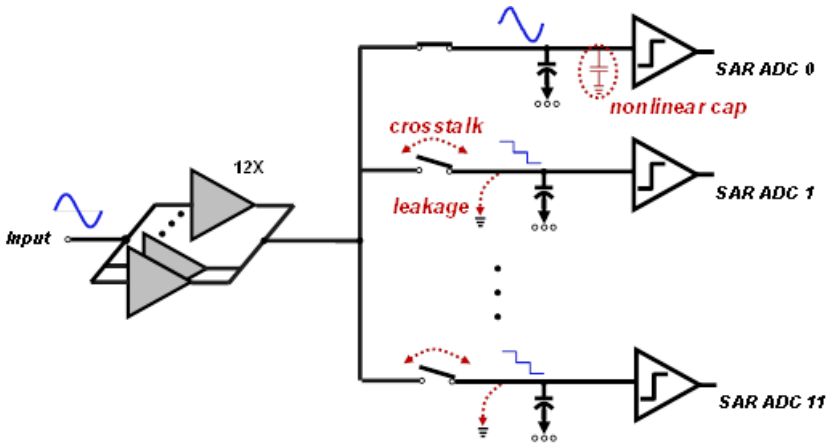

Figure 4.4: Sample/hold network in the TI ADC.

auxiliary path of the common source stage. The -1 block in Fig. 4.5 represents the cross-coupled wire connection in the actual differential implementation. The auxiliary path provides a little extra gain to compensate the loss from the main path of source follower to achieve overall unity gain. Without this auxiliary path, the loss of input buffer would require the larger output swing at its front stage, which is RF front-end in direct sampling receiver as shown in Fig. 4.1. Thus, the linearity requirement for the output stage at RF front-end would be more difficult. Besides, since the pole of each path is at high frequency, the combination of the two paths will induce the pole-zero doublets at the high frequency. This input buffer remains wide bandwidth.

The signal distribution needs to be carefully considered to minimize bandwidth and phase mismatches among the channels. First, the outputs of all buffer units are shorted together, so the mismatch of buffer units will not contribute inter-channel mismatches and all buffer units are used for the S/H settling in each SAR

channel. Then, each buffer unit has a layout pitch matching that of each SAR channel for easy signal distribution and good inter-channel matching, as shown in Fig. 4.6. It can be seen that a tree-type routing is used to distribute the signal of Vin to each buffer unit input achieving an equal delay for the input signal. In addition, a ring-type routing for Vo is applied to equalize the buffer loadings among the central channels and the channels in the both edges.

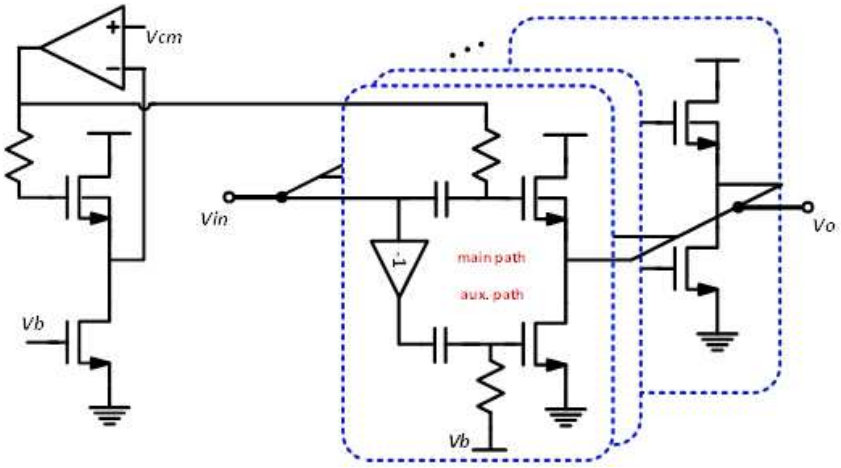

Figure 4.5: Simplified schematic of the input buffer.

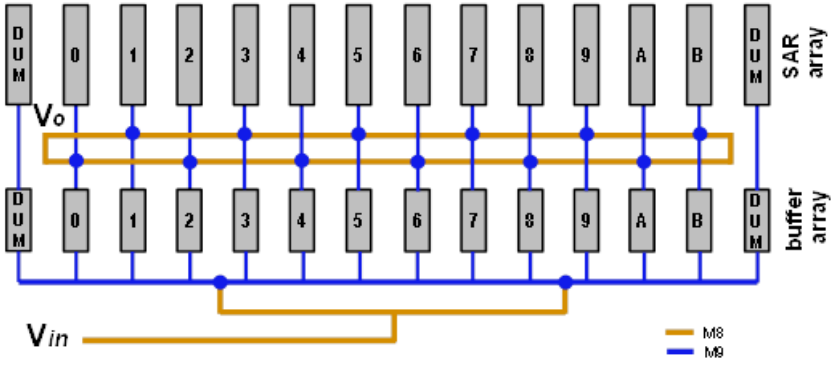

Figure 4.6: Layout floor plan of the TI ADC.

4.3.3 Sampling Switch

For this high-speed IT ADC, a single conventional sampling switch with long channel length and/or high threshold voltage is not good enough to prevent inter-channel crosstalk due to parasitic capacitance C_{ds} which is composed by the drain source capacitor of the sampling transistor and the routing parasitic capacitance. To address the issues of the inter-channel crosstalk and the charge leakage during SAR conversion phases, a T-type sampling switch with the combination of a low-Vth transistor (LVT) and a high-Vth transistor (HVT) is applied. Its concept is illustrated in Fig. 4.7. During the conversion phases, M3 is shorted to Vcm, and both M1 and M2 are turned off, so this T-type switch provides good isolation to prevent the inter-channel crosstalk. During the sampling phases, both M1 and M2 are bootstrapped to achieve good linearity and to reduce the switch on-resistance for fast settling. In addition, in order to minimize the signal-dependent leakage current during the conversion cycles, M2 is implemented using a HVT transistor for small leakage current when it is off; and M2 bulk is dynamically biased as well. The M2 bulk voltage of Vb is generated by a charge-pump-like circuit: when ϕ_a is high, Vb is tied to ground; when ϕ_a changes from high to low, Vb goes to a negative value, which is set by the capacitor ratio of C_3/C_4. Therefore, M2 bulk is switched between ground and around -500 mV during on and off, respectively. The negative body biasing increases the threshold voltage and reduces the leakage current. In order to clearly define the sampling instant, ϕ_a is slightly earlier than ϕ to assure the falling edge of the clock for M2 is the only critical clock transition.

The basic principle of the bootstrapping is illustrated in Fig. 4.7 as well. The

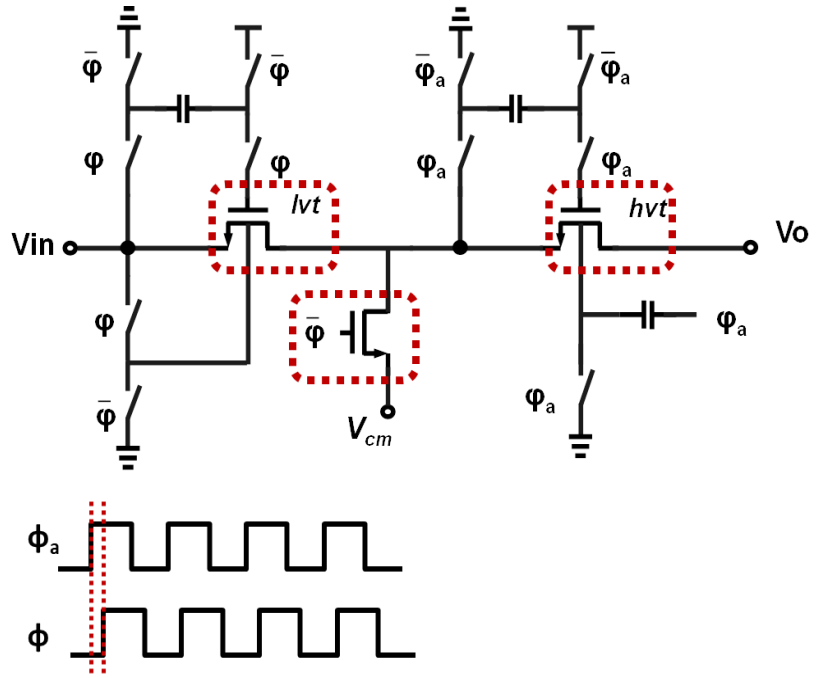

Figure 4.7: Conceptual T-type sampling switch.

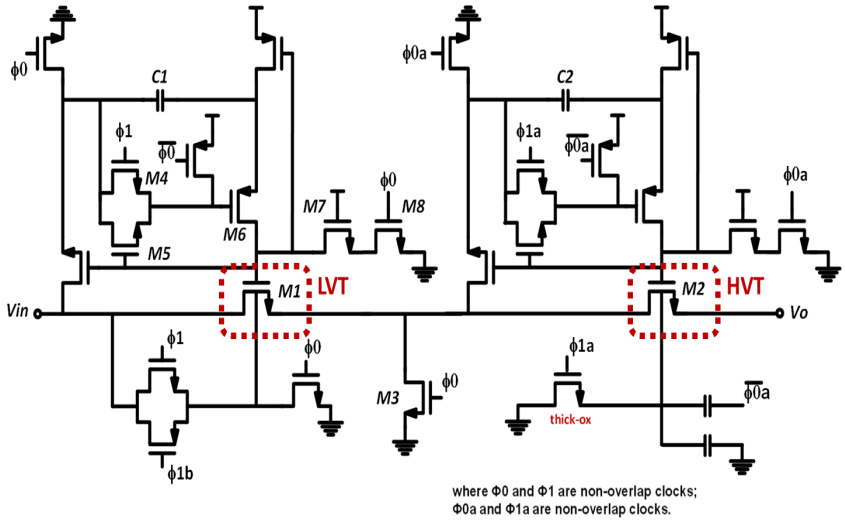

Figure 4.8: Detailed implementation of the sampling switch.

capacitor C1 is pre-charged to Vdd initially. Then the pre-charged C1 is applied onto V_{gs} of the sampling switch to achieve a constant voltage regardless of the input voltage in the hold phase. However, there are two issues associated with this operation. First, the associated parasitics capacitance cause V_{gs} of M1 modulated by the input signal, and also limits the bootstrap bandwidth, degrading linearity at high frequencies. Second, while an input signal approaches Vdd, the gate voltage at M1 rise to 2Vdd causing MOS reliability problems, for instance, dielectric breakdown, hot electron, punch-through.

For this design, the detailed implementation of the T-type sampling switch is depicted in Fig. 4.8, where the bootstrapping implementation is similar to [Dessouky and Kaiser [2001]]. In the consideration of bootstrapping switch of M1, C1 is pre-charged during ϕ_0. At the beginning of ϕ_1, M4 and M6 turn on first and M1 gate starts to rise, and then M5 and M7 turn on. At the end of ϕ_1, M1 gate rises to Vin+Vdd. M7 has been added to prevent Vgd of M8 from being overstressed while it is off. This implementation consists of almost entirely of thin-oxide transistors except M10, which needs to handle 1.5V V_{gs} right after ϕ_{1a} goes high. Therefore, both the parasitics issue and the reliability issue are significantly alleviated, and a high-speed highly linear switch is achieved.

4.4 SAR ADC Implementation

4.4.1 SAR ADC channel

An individual channel of a 10b SAR ADC consists of an analog and a digital part. A simplified schematic of the analog part of the ADC channel is shown in

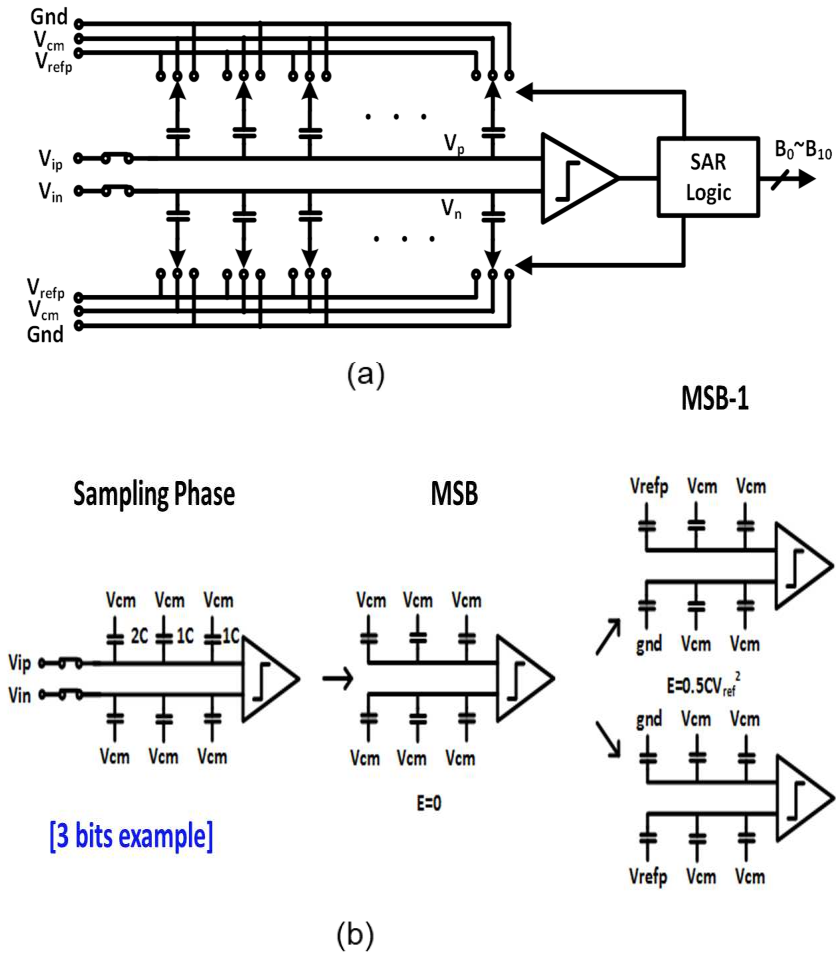

Figure 4.9: (a)Simplified schematic of the analog part in a SAR channel; (b)Merged capacitor switching algorithm.

Fig. 4.9 (a). Top-plate sampling circuit with merged capacitor switching algorithm [Hariprasath and et al [2010]] is chosen for its high switching efficiency and less total capacitors. The detailed operation will be explained in the next paragraph. In addition, in bottom-plate sampling SAR ADCs, the charge sharing between the comparator input capacitance and the sampling capacitor attenuates the sampled

signal, or equivalently amplifies the comparator noise, which is usually one of the dominant noise sources. This top-plate sampling SAR ADC avoids this effect. The 11b sub-radix-2 with 1b redundancy in the capacitive DAC (CDAC) is applied to tolerate decision errors arising from noise, reference settling, etc. The redundancy is implemented in the first 6 MSBs with the capacitance ratio of approximately 1.75, since most of reference settling errors happen in the MSB conversion cycles. The capacitance ratio for the rest of LSBs is still binary. Detailed discussion to optimize the capacitor ratio in CDAC will be explained in Section IV.C. A compact customized M4-M6 metal finger capacitor is used to reduce the area while preserving good ratios between the capacitors. The unit capacitor is around 2 fF to achieve better than 10-bit matching accuracy. Actually, in terms of matching accuracy, the unit capacitor size can be even smaller according to the recently published papers [Inerfield et al. [2014]]. Outputs of the analog part of the channel are raw output bits. Then the digital part of each channel removes gain and offset mismatches, and realizes the non-binary to binary mapping on the output data. In addition, SAR logic majorly consists of shift registers to realize a synchronous SAR timing for its simplicity and small power consumption.

The operation of top-plate sampling with merged capacitor switching algorithm can be illustrated in Fig. 4.9(b), where a 3-bit CDAC is used as an example. During the MSB cycle, the bottom plate of CDAC is connected to Vcm while the top plate is holding the input signal, Vin. Apparently, the MSB can be determined right after the sampling phase without consuming any switching energy due to no charge redistribution. Depending on the value of MSB, the bottom plate of first

capacitor will switch from Vcm to either Vrefp or ground. The rest of conversion cycles will follow the same scheme. Besides the efficient MSB conversion, the 3-level reference: Vcm, Vrefp and ground, halves the voltage step at the bottom plate of CDAC and significantly minimizes the switching energy during the conversion cycles compared to conventional 2-level reference, since the energy consumption is proportional to CV^2.

4.4.2 Optimization for Input CM Voltage of Comparator

As for the selection of the reference levels, Vcm is typically set to $V_{refp}/2$, so the input common-mode voltage of the comparator will keep same as the common-mode voltage of the input buffer output during the conversion cycles, as depicted in Fig. 4.10(a). However, the comparator can be at better operating region when its input common-mode is less than the half of 1.0 V power supply, since it has a PMOS input pair. In order to obtain this, Vcm is not equal to $V_{refp}/2$. Actually, $V_{refp} = 0.6V$ and $V_{cm} = 0.4V$ in this design. As a result, the input common-mode voltage of the comparator gradually moves from the initial 0.5 V to 0.4 V during the conversion process, as shown in Fig. 4.10(b). The relatively large decision errors during MSB conversion cycles, where the input CM of comparator is about 0.5V, could be recovered by the redundancy in CDAC. The last LSB conversion cycles with binary capacitor ratio are more critical, where the input CM of comparator moves to 0.4V, a better operating region for a PMOS input pair. However, lowing input-common voltage of the comparator will cause the offset voltage to vary during SAR conversion cycles. This issue can be solved by the design and will be

discussed in the Section IV.D.

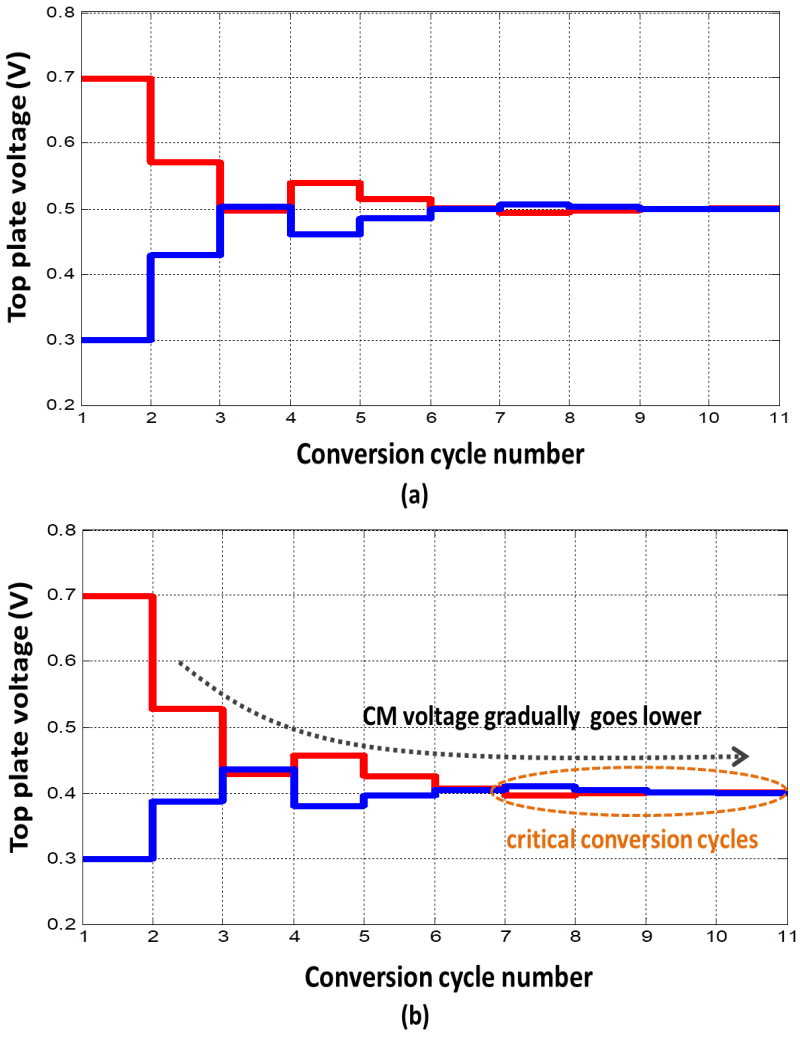

Figure 4.10: The waveform of the top-plate CDAC in a SAR ADC (a) $V_{cm} = V_{refp}/2$, (b) $V_{cm} \neq V_{refp}/2$

4.4.3 Reference Buffer and Related CDAC Optimization

Typically placing large capacitors at the reference voltages would have a low-power advantage, because it only consumes the switching energy, but no quiescent current as class-A or class-AB reference buffers have. However, a TI ADC requires large off-chip capacitors to minimize inter-channel crosstalk through the reference voltages. In this design, the fast reference buffers are separated for each SAR channel. The simplified schematic of V_{refp} buffer is shown in Fig. 4.11, where 12 buffer units are all biased by a replica unit; and each buffer unit is a super source follower, which includes a feedback loop to minimize the output resistance for fast settling when the SAR algorithm is applied. The feedback loop gain and stability can be controlled by the resistor connected to the ground in this design. Sometimes the resistor could be replaced by a current source, and then the frequency compensation may be added for the loop stability. Obviously, the device mismatches among the 12 buffer units will cause the full-scale mismatch among 12 SAR channels meaning inter-channel gain mismatch, which needs to be removed by each individual digital calibration engine discussed in Section V. At the same time, Vcm buffer is implemented using a similar topology, but using NMOS instead. In addition, since ground is used as a reference level, one reference buffer is saved for each SAR channel, achieving better power efficiency.

Each SAR channel poses a settling requirement for the feedback loop, which consists of a comparator, SAR logic, CDAC and reference buffers, as shown in Fig. 4.9. Since each SAR channel has a V_{refp} buffer and a V_{cm} buffer, the power consumption of the reference buffers are not insignificant. Therefore, there is a trade-

off between speed and power consumption for the reference buffers. Fig. 4.12 illustrates the output voltage and the output current for a reference buffer during the conversion cycles. Obviously, the voltage ripples are significantly large in MSB conversion cycles, which would also induce large setting errors affecting ADC accuracy unless a power-hungry buffer is used. In order to avoid large power penalty or severe ADC performance degradation, the redundancy is applied in the first 6 MSBs in the CDAC array, where the capacitance ratio is approximately 1.75 in this design. At the same time, a binary capacitor ratio is used in the rest of LSBs without adding extra ADC conversion cycles due to the much smaller voltage step and the RC time constant in the loop.

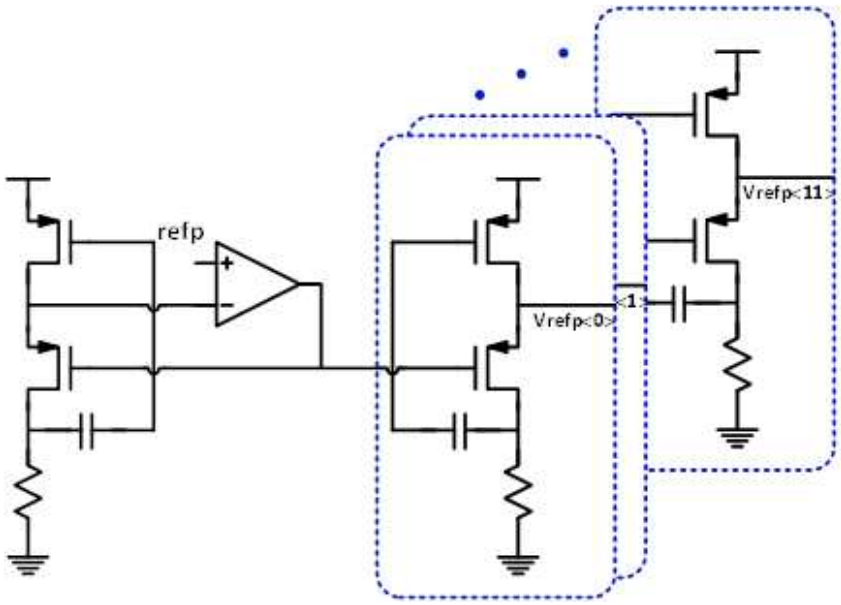

Figure 4.11: Schematic of the reference buffer.

Further, let us look at the output current of the reference buffer, as shown in Fig. 4.11. The MSB conversion will cause the largest output current spike for

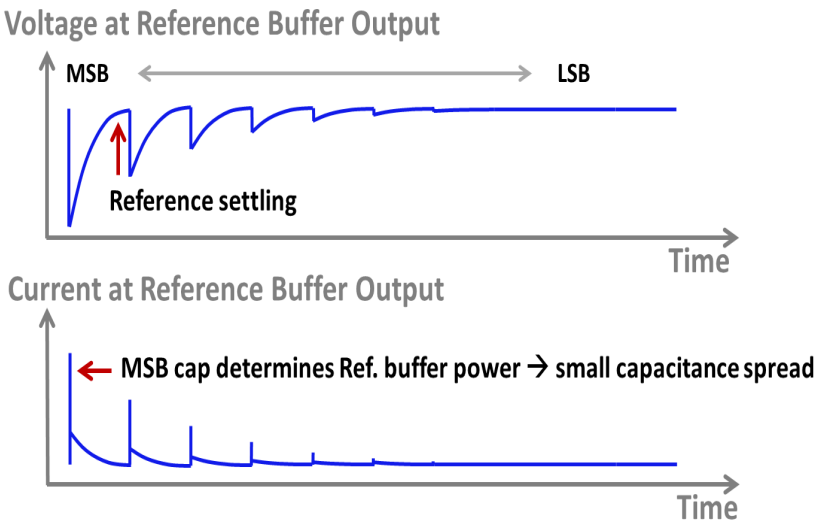

Figure 4.12: Output voltage and output current of the reference buffer.

a reference buffer, which actually determines its power consumption. This observation implies that the MSB capacitor in CDAC should be as small as possible for power efficiency, which gives a guidance to choose one of two commonly used schemes for the capacitor ratio for redundancy: Option 1 of [32 16 8 8 4 2 1 1] and Option 2 of [26 18 12 8 4 2 1 1]. This example has 8-bit CDAC with 1 extra bit redundancy. First, option 1 may have a bit more redundancy range since it puts all redundancy on the single 4th bit, which helps recover all the conversion errors happening at the first 4 MSBs. However, option 2 distributes the redundancy into the 4 MSBs progressively and achieves a smaller capacitor spread, which leads to lesser power consumption of the reference buffers and lesser settling error for the MSB conversion. Therefore, the option 2 scheme for the capacitor ratio is used in this design.

4.4.4 Comparator

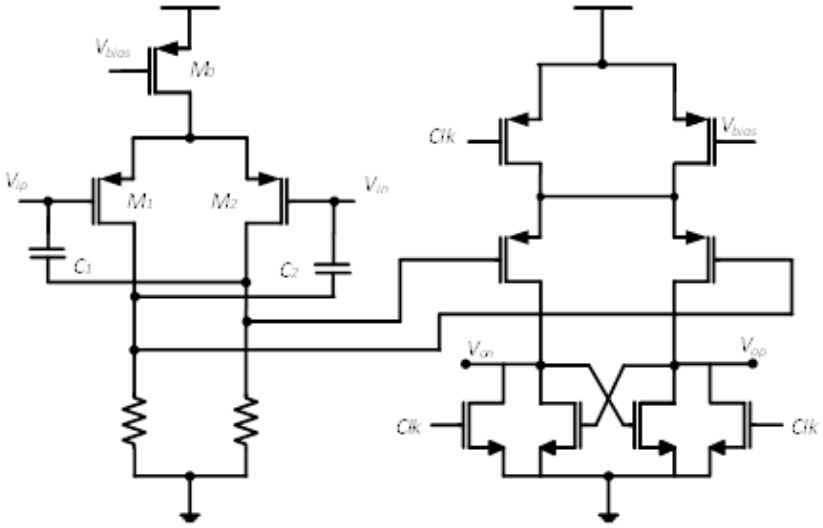

Figure 4.13: Schematic of the comparator.

The comparator comprises a static pre-amplifier and a dynamic latch, as shown in Fig. 4.13. The pre-amplifier has been designed for low noise and moderate gain to improve the comparator noise performance, to reduce its offset, and more importantly, to limit the kick-back noise from the dynamic latch. The input capacitance of comparator needs to be small for (a) the charge sharing between the preamplifier input capacitance and the sampling capacitor attenuates the sampled signal, hence increasing the gain of the preamplifier noise on the total SNR; (b) the comparator input capacitance Cgs is signal-dependent and will cause a distortion issue in the sampling when a large input signal causes the input transistors of M1 and M2 to trip between saturation and linear or cut-off region. In this design, the cross-coupled capacitors C1 and C2 are added to linearize and neutralize the input capacitance of the comparator in order to alleviate this sampling error and to in-

crease the pre-amplifier bandwidth. The following dynamic latch has the clocked tail PMOS and a small tail current ensuring the latch is in a weak conduction state when the clock is high, which makes the comparator recover faster from the reset state. The reset devices then eliminate the memory effect at the internal nodes of the comparator.

As discussed previously, lowing input-common voltage of comparator makes the pre-amplifier of PMOS input-pair work at a better operating region, which not only improves the comparator speed, but also reduces the comparator noise at LSB conversions. However, the offset voltage will vary due to different input common-mode voltages. The offset voltage of this comparator can be expressed as [Liu et al. [2010]]:

$$V_{os} = \Delta V_{th1,2} + \frac{(v_{GS} - v_{th})_{1,2}}{2}(\frac{\Delta S_{1,2}}{S_{1,2}} + \frac{\Delta R}{R}) \tag{4.1}$$

Where $\Delta V_{th1,2}, (V_{GS} - V_{th})_{1,2}, \Delta S_{1,2}$ is the threshold voltage offset, the effective voltage and the physical dimension mismatch of the differential pair M1 and M2, respectively. ΔR is the loading resistance mismatch induced by the resistor loading and the following dynamic latch stage. The second term of Eq.4.1 is a signal-dependent dynamic offset since $(V_{GS} - V_{th})_{1,2}$ varies with the input common-mode voltage.

Actually, the dynamic offset has a minor influence on the conversion linearity in this work. First, as discussed in Section IV.B, the input common-mode voltage of comparator only changes from 0.5V to 0.4V, which is much smaller than

that in [Liu et al. [2010]]. Then, the tail current M0 keeps relatively constant current even with V_{ds} changes of M0, which causes the effective voltage of input pair nearly constant. In addition, this small offset variation can be fully recovered by the CDAC redundancy, as discussed in Section IV.C. Finally, since the comparator input common-voltage always goes to 0.4V at the end of SAR conversion cycles, the comparator offset with 0.4V input common-mode voltage is eventually removed in the digital domain with the digital offset calibration in Section V.

4.5 Digitally-Assisted Circuits

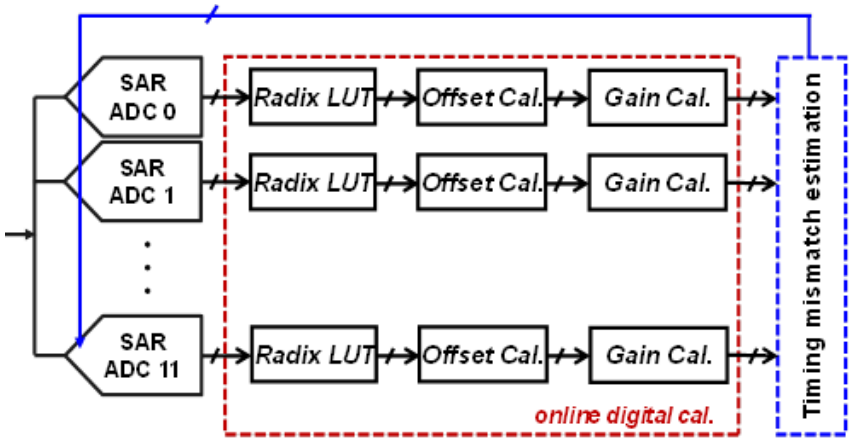

Figure 4.14: Diagram of digital calibration in the TI ADC.

The performance of TI ADCs suffers from inter-channel timing, bandwidth, offset and gain mismatches. In section IV, several analog design techniques are introduced to alleviate these non-ideal factors. Now digitally-assisted calibration schemes will be discussed in this section to further enhance the performance of TI ADCs. As shown in Fig. 4.14, each SAR channel has the digital part, which in-

cludes a radix look-up table to convert the sub-radix-2 data into a twos complement format, and then offset and gain calibration engines to remove inter-channel gain and offset mismatches. In the end, inter-channel timing mismatch is estimated offline, and is corrected by tuning the programmable delay of the sampling clock in each ADC channel.

Fig. 4.15 shows the diagram of digital offset calibration on the left and the diagram of digital gain calibration on the right. First of all, since both offset and gain are changing slowly, a down-sampling operation can be performed first to reduce power consumption substantially. DC offset can be easily calculated by averaging the digital output at node In. Then DC offset at each SAR channel is removed by subtracting the average from the digital output. Furthermore, an accumulate-and-dump sinc filter is an efficient architecture to perform down-sampling operation and averaging operation in digital calibration. After removing the DC offset, the average power for each SAR channel can be calculated and kept updated by performing a square operation and a leaky integrator operation. In each SAR channel, a common digital value called Threshold sets as a power reference. By adjusting the gain of each channel, the power at node Out at each channel will be equal to Threshold. Therefore, the inter-channel gain mismatch is corrected.

In multi-GS/s and high-resolution TI ADCs, the inter-channel timing and bandwidth mismatch due to interconnect mismatch, device mismatch, IR-drops in supplies and bias lines, etc. is a more difficult issue. This design requires achieving 0.5ps timing accuracy, a very challenging task. [Doris et al. [2011]][Gupta et al. [2006]] proposed a pure analog solution of inserting a common full-speed front-end

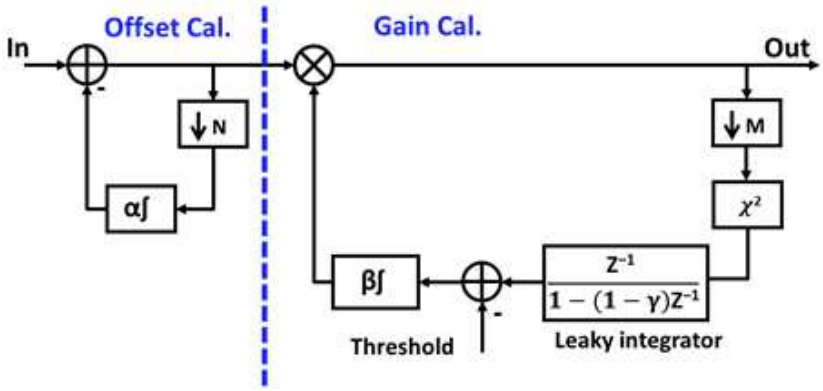

Figure 4.15: Diagram of offset and gain digital calibration.

sampler at expense of a power and noise penalty, because the sampled voltage needs to be resampled in the individual SAR channel. A pure digital timing correction has been proposed in [Doris et al. [2011]][Dortz et al. [2014]][et al [2002]][Prendergast et al. [2004]]. This technique uses fractional delay filters, which are realized by multirate filter banks, to reconstruct the nonuniformly sampled signal. Since the filters are quite complex and run at the ADC sampling clock, it results in substantially high power consumption. Typically, the most power-efficient approaches estimate the timing mismatch, and then tune the programmable delay of the sampling clock at each ADC channel. There are many methods to estimate the timing mismatches. In [Greshishchev et al. [2010]], FFT processing and calibration DACs were used to estimate the timing mismatch. In [Greshishchev et al. [2010]][Stepanovic and Nikolic [2012]][Wu et al. [2013]][et al [2009]], the difference between each channel and an additional reference channel were used to estimate the timing mismatch. In [Sahoo and Razavi [2013]], the correlation of the adjacent channel outputs is calculated to determine the timing mismatch. In [Sung et al. [2015]][Lee et al.

[2015]], the ADCs have a hybrid structure of a flash ADC and TI SAR ADC channels. The difference between the full speed flash and each SAR channel are used for the timing estimation.

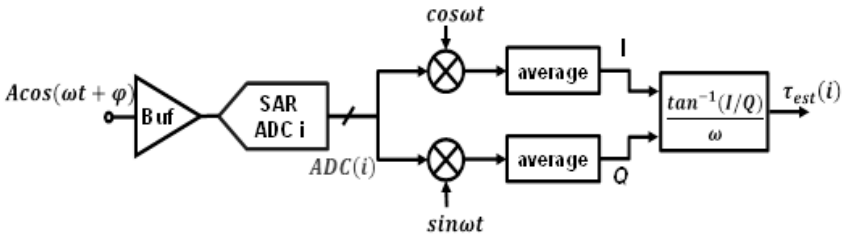

Figure 4.16: Diagram of timing mismatch estimation.

In this design, the principle of the timing mismatch estimation is illustrated in Fig. 4.16. Firstly, a pilot tone generated from a calibration DAC in direct digital frequency synthesis or a PLL with filters or off-chip, is fed to the ADC input. The digital output of each SAR channel can be expressed as:

$$ADC(i) = Acos(\omega(t+\tau(i))+\phi)+q+e \tag{4.2}$$

where τ is the time delay induced by each ADC channel, e is circuit noise, q is ADC quantization noise. Next the digital output is multiplied by a digital I/Q sinusoidal waveform, which has the same input signal frequency. After an averaging operation, the output at I and Q can be expressed as:

$$I = \overline{(Acos(\omega(t+\tau(i))+\phi)+q+e)\cdot cos(\omega t)} = 0.5Acos(\omega\tau(i))+\phi) \tag{4.3}$$

$$Q = \overline{(Acos(\omega(t+\tau(i))+\phi)+q+e)\cdot sin(\omega t)} = 0.5Asin(\omega\tau(i))+\phi) \quad (4.4)$$

Lastly, the relative timing skew induced by each ADC channel can be obtained by employing an inverse tan function, expressed as:

$$\tau_{est}(i) = \frac{tan^{-1}(Q/I)-\phi}{\omega} \quad (4.5)$$

Based on the estimation results, the programmable delay at each SAR channel can be tuned to correct the timing skew. The advantage of this estimation scheme is that it is not sensitive to the interference from noise and nonlinearity terms, and not sensitive to varying signal amplitude and dc offset, although they can easily be removed by the digital calibration shown in Fig. 4.14.

4.6 Measurement Results

The prototype IC, which includes a PLL, input buffer and the SAR ADC as shown in Fig. 4.2, is implemented in 28nm CMOS technology. A die micrograph of the TI ADC is shown in Fig. 4.17, occupying an area of $0.57mm^2$. It should be noted that the multiplexer, which selects 12 channel outputs in a rotated manner with a decimation ratio of 13, causes the content of the complete sampled spectrum to fold on 1/13th of the Nyquist frequency and allows measuring all spectral artifacts of the converter. The TI ADC consumes 76mW from 1.0V supply while sampling at 5.0GS/s with the digital calibration.

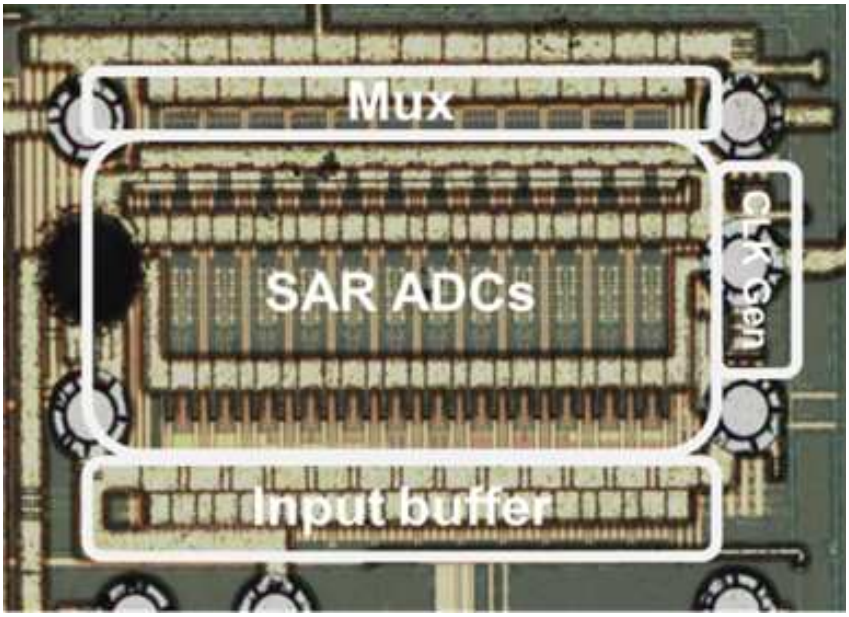

Figure 4.17: Die micrograph.

To evaluate the effectiveness of the timing calibration algorithm, dc offset mismatch and gain mismatch are removed first. Fig. 4.18 shows the measured ADC output spectral plots with and without and the timing calibration for a -3dBFS 2.001 GHz input sinusoidal signal sampling at 4.968GHz. An input signal full-scale is $1.2V_{pp-diff}$, which is limited by the input buffer of 1.0V supply. Before the timing calibration, the artifacts from timing mismatch are dominant. The SFDR and SNDR are 38.4dB and 33.3dB, respectively. After the timing calibration, the 3rd harmonic becomes the dominant spur, and SFDR and SNDR improve to 54.5dB and 41.7dB, respectively. The SNR is 49dB for a -3dBFS signal, which is extrapolated from small-input measurement results for minimizing clock phase noise influence.

After the timing calibration, there are still many relatively small spurs in

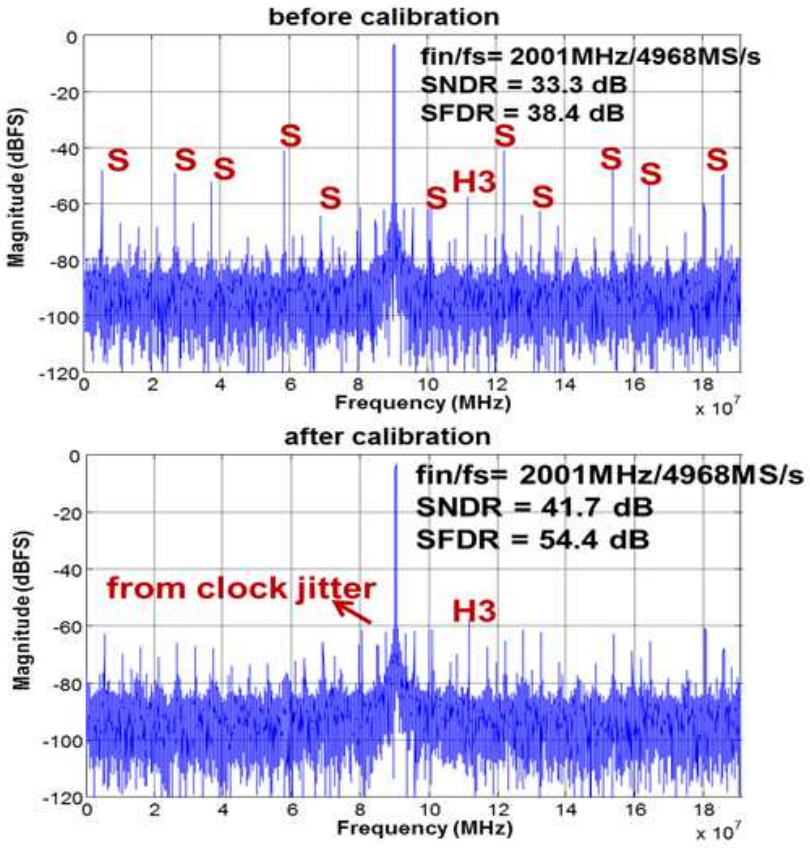

Figure 4.18: Measured ADC output spectral plots without and with timing calibration for 2001MHz signal (decimated by 13).

Fig.15. First, several spurs are due to the circuit nonlinearities from the non-ideal input buffer, non-ideal sampling switch, finite setting time in S/H cycles, finite loop settling in conversion cycles, kickback noise from the comparator. Second, the capacitor mismatch of CDAC in each sub-ADC channel degrades also ADC linearity and induces spurs. Due to the design target of 50dB THD, the calibration for the capacitor mismatch is not implemented in this work. In addition, the artifact residue of the timing mismatch due to the granularity of the programmable delay also has

some impact to the SNDR result.

To verify performance of the ADC across different input frequencies, the input signal frequency has been swept from 100MHz to 2300MHz. The measured SNDR and THD versus input frequency at 4968MS/s sampling rate are plotted in Fig. 4.19. The SNDR at low frequencies is determined by the harmonic distortion and thermal noise. Without the timing calibration, the artifacts due to timing mismatch at a high frequency limit the SNDR performance. After the timing calibration, SNDR gradually decreases with signal frequency due to clock jitter effect.

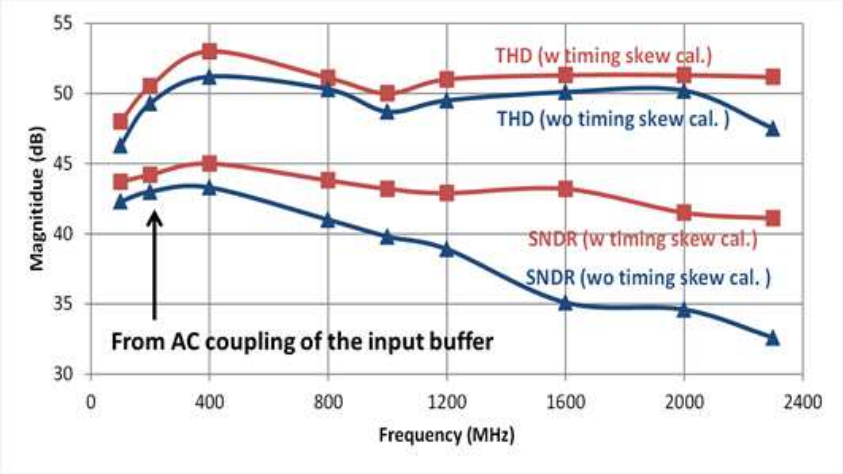

Figure 4.19: Measured SNDR and THD versus input frequency.

The power consumption breakdown is shown in Fig. 4.20. It can be seen that the comparator and the SAR logic take the two largest portions of power consumption. Using a fully dynamic Strong-Arm comparator with the foreground offset calibration could significantly improve the power efficiency in the future. The larger kickback noise needs be taken care of by making the impedance at the com-

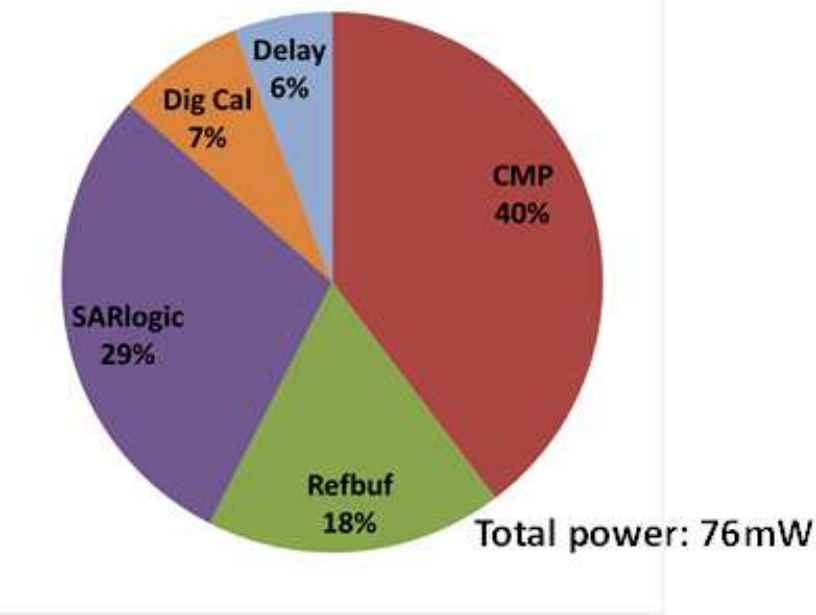

Figure 4.20: Power breakdown.

parator inputs matched as much as possible. Further, asynchronous SAR logic could reduce the power of the dynamic comparator because only one or two of 11 comparison cycles need long time for the meta-stability cases. Besides, a smaller unity capacitor with capacitor mismatch calibration can be used in the design to achieve better power efficiency and performance. Since the MOM capacitor mismatch in CDAC is almost static, a foreground or slow background digital calibration for capacitor mismatch can be used for almost zero or very small power consumption [Stepanovic and Nikolic [2012]][Inerfield et al. [2014]][Chang et al. [2013]][Kull et al. [2013]][McNeil et al. [2011]].

A comparison with state-of-the-art ADCs with similar conversion rate and resolution is made in Table 1. The Walden figure of merit (FoM) is 165 fJ/conversion-

step calculated with high-frequency ENOB. A Walden FOM comparison to the prior-art ADCs with sampling frequencies higher than 3 GHz and SNDR larger than 30dB published at ISSCC and VLSI conferences from 1997 to 2015 [Mur [2017]] is shown in Fig. 4.21. This work achieves the lowest FoM among ADCs with $Fs > 3GHz$ and SNDR$> 40dB$.

Table 4.1: Performance comparison

	Dortz et al. [2014]	Janssen et al. [2013]	Wu et al. [2013]	Brandolini et al. [2015]	This work
Architecture	TI SAR	TI SAR	TI Pipleline	TI SAR	TI SAR
Technology	40nm	65nm	28nm	32nm SOI	28nm
Supply voltage [V]	1.1	1.2	1.0	1.0	1.0
Fs [GS/s]	1.62	3.6	5.4	8.8	5
SNDR(Nyq) [dB]	48	50	50	37	42
Resolution [bit]	9	11	12	8	10
Power [mW]	93	795	500	35	76
FOM [fJ/step]	279	855	358	68.9	165
Active area [mm^2]	0.83	7.4	0.4	0.025	0.57

4.7 Conclusion

This chapter presents a 5GS/s, 10b, 12X time-interleaved SAR ADC for direct sampling receiver applications. The issues of inter-channel offset, gain and timing mismatches in a TI ADC are minimized by careful signal and clock distribution along the multiple channels, and the digitally-assisted calibration. The inter-channel crosstalk and the signal-dependent leakage current during SAR conversion cycles are mitigated by proposed T-type bootstrapped sampling switches.

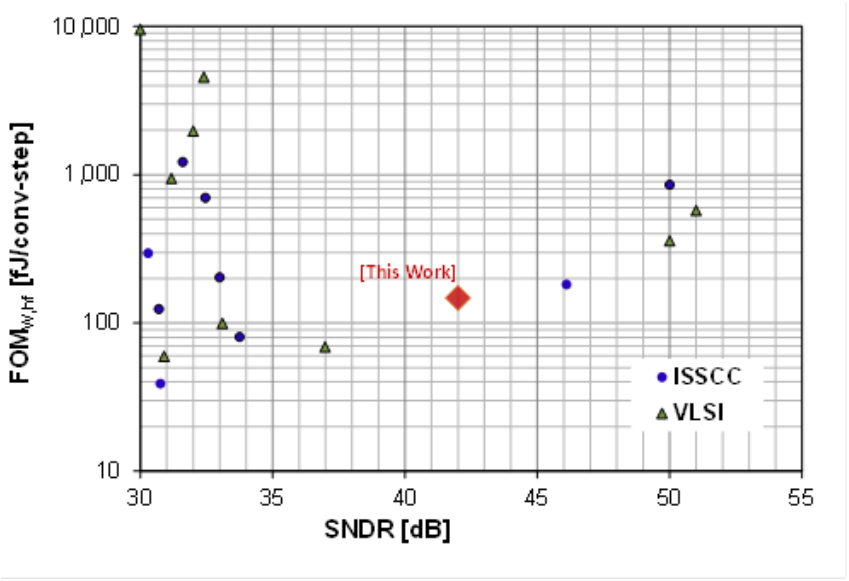

Figure 4.21: Walden FOM Comparison for ADC with Fs>3GHz and SNDR>30dB.

The ADC power efficiency is significantly improved by many design techniques: the low-energy CDAC switching scheme, optimized input common-mode voltage for comparator, optimal sub-radix-2 capacitor ratio for low-power reference buffers and higher conversion speed, etc.

Measurements show that this ADC achieves 49dB SNR, 52dB THD and 42dB SNDR in the Nyquist band while consuming 76mW from 1V supply and occupying $0.57mm^2$ in 28nm CMOS technology. The experiment results demonstrate the proposed architecture is highly scalable to an advanced CMOS technology and also has even higher power efficiency potential.

Chapter 5

Conclusion and Future Directions

5.1 Conclusion

This thesis investigates the analog design of a DS receiver, which mainly consists of a broadband RF front end and a wideband ADC. Thanks to the flexibility of digital signal processor, A DS receiver is very efficient for the simultaneous reception of multiple channels with much less hardware complexity comparing with the parallelism of superheterodyne receivers.

Two broadband RF front ends for direct sampling receivers, which include either RFPGA-V or RFPGA-I followed by the same 6-dB gain buffer and RF filter, has been demonstrated. Especially, two new architectures of RF programmable-gain amplifier (RFPGA): voltage-mode RFPGA-V and current-mode RFPGA-I, has been presented and comparatively analyzed. RFPGA-V and RFPGA-I utilize an innovative interpolation method and current steering approach, respectively, to achieve a fine gain step over wide gain range for a broad frequency band. RFPGA-I has wider frequency range than RFPGA-V. However, it is convenient to use RFPGA-V architecture to realize even finer gain step for relatively low frequency applications. Besides, with innovative design, no inductor is needed in either RFPGA.

A 5-GS/s, 10b, 12X time-interleaved SAR ADC for direct sampling re-

ceivers is presented. The issues of inter-channel offset, gain and timing mismatches in a TI ADC are minimized by careful signal and clock distribution along the multiple channels, and the elaborate digitally assisted calibration. The inter-channel crosstalk and the signal-dependent leakage current during SAR conversion cycles are mitigated by proposed T-type bootstrapped sampling switches. The ADC power efficiency is significantly improved by many design techniques: the low-energy CDAC switching scheme, optimized input common-mode voltage for comparator, optimal reduced radix-2 capacitor ratio for low-power reference buffers and higher conversion speed, etc.

5.2 Future Directions

The presented broadband RFPGA-I can receive a broadband differential signal. It would be desirable to receive a single-ended signal as well avoiding an off-chip balun. For the single-ended mode, the opamp in RFPGA-I should be a broadband active balun, performing single-ended-to-differential conversion. Besides, the resistive DAC in RFPGA-I needs to be modified to support a single-ended as well.

Communication in mm-wave band is gaining lots of attention. For example, new access radio in 5G mobile standard includes wide-range mm-wave band. Ku band (12.2-12.7 GHz) and Ka band (17.3-20.2 GHz) are widely used in the satellite communication. Currently, most of mm-wave RF front-ends are implemented in III-V technologies. An mm-wave integrated RF front end in a CMOS technology would be an interesting direction.

Improving power efficiency of a SAR ADC is always a direction for many

applications. To reduce power further in a single-slice SAR ADC in the prototype, several methods can be used. Smaller unity capacitor will result in lower power, but worse mismatch. One-time capacitor mismatch calibration can be utilized to calibrate the mismatch without extra power, since MIM capacitor is insensitive temperature or voltage variation. Fully dynamic Comparator with offset calibration and Asynchronous SAR logic are also commonly effective method to lower the power. If extra pins in the silicon are available, power supplies can be used as reference to avoid the power of reference buffers.

Driving an ADC into higher sampling rate and higher resolution has been a technology trend for many years. Besides time-interleaved SAR ADCs, a hybrid structure is a good direction to explore. For example, in a Flash-SAR ADC, a flash ADC can be used in the first several MSB conversions to improve the speed of ADC. In a pipelined-SAR ADC, the gain of MDAC in first (several) stage(s) can improve the ADC noise performance or resolution.

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Vita

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