The Dissertation Committee for Kunhee Cho
certifies that this is the approved version of the following dissertation:

Integrated Circuits for Efficient Power Delivery using Pulse-Width-Modulation

Committee:

Ranjit Gharpurey, Supervisor

Jacob Abraham

Michael Orshansky

Deji Akinwande

Lei Ding

Integrated Circuits for Efficient Power Delivery using Pulse-Width-Modulation

by

Kunhee Cho, B.S., M.S.

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To my beloved wife and parents

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Integrated Circuits for Efficient Power Delivery using Pulse-Width-Modulation

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Circuits and architectures for efficient power delivery have become crucial in emerging smart systems. Switching power amplifiers (PA) are very attractive for such applications, because they exhibit better efficiency compared to linear PA designs, due to saturated operation. Switching PAs also allow for utilization of deep submicron CMOS technologies, due to which these designs can be easily integrated with digital circuits, and can benefit from process scaling, in performance as well as in area.

Pulse-width-modulation (PWM) is commonly used with switching PAs. A PWM signal typically employs a high-frequency switching pulse waveform as a carrier signal, wherein the pulse-width or duty-cycle of each pulse is modulated by a given low-frequency input signal. The carrier frequency can vary from several kHz to GHz, and is typically determined by the target application.

In this thesis, efficient power-delivery circuits that use PWM with switching class-D stages are presented. Advanced circuit techniques, as well

as architectures for PWM are proposed to enhance efficiency and circumvent the limitations of conventional architectures.

A digitally-intensive transmitter using RF-PWM with a class-D PA is described in the first part of the thesis. The use of carrier switching for alleviating the dynamic range limitation that can be observed in classical RF-PWM implementations is introduced. The approach employs the full carrier frequency for half of the amplitude range, and the second harmonic of half of the carrier frequency, for the remainder of the amplitude range. This concept not only allows the transmitter to drive modulated signals with large peak-to-average power ratio (PAPR), but also improves the back-off efficiency due to reduced switching losses in the half carrier-frequency mode. A glitch-free phase selector is proposed that removes the deleterious glitches that can occur at the input data transitions. The phase-selector also prevents D flip-flop setup-and-hold time violations. The transmitter has been implemented in a 130-nm CMOS process. The measured peak output power and power-added-efficiency (PAE) are 25.6 dBm and 34%, respectively. While driving 802.11g 20-MHz 64-QAM OFDM signals, the average measured output power is 18.3 dBm and the PAE is 16%, with an EVM of -25.5 dB.

The second part of the thesis describes a high-speed driver that provides a PWM output using a class-D PA. A PLL-based architecture is employed which eliminates the requirement for a precise ramp or triangular signal generator, and a high-speed comparator, which are typically used for PWM generation. Multi-level signaling is proposed to enhance back-off as well as

peak efficiency, which is critical for signals with high PAPR. A differential, folded PWM scheme is introduced to achieve highly linear operation. 3-level operation is achieved without the requirement for additional supply source or sink paths, while 5-level operation is achieved with additional supply source and sink paths, compared to 2-level operation. The PWM driver has been implemented in a 130-nm CMOS process and can operate with a switching frequency of 40-to-170 MHz. For 2/3/5-level PA operation, with a 500 kHz sinusoidal input and 60 MHz switching frequency, the measured THD is -61/-62/-53 dB and corresponding efficiency is 71/83/86% with 175/200/220 mW output power level, respectively. Performance has also been verified for 2/3-level PA operation with a high PAPR signal with 500 kHz bandwidth. While intended as a general purpose amplifier, the approach is well-suited for applications such as power-line communications (PLC).

The final part of the thesis introduces an efficient buck/buck-boost reconfigurable LED driver that supports PWM and PFM operation. The driver is based on peak current control. Rectified sin as well as $\sin^2$ functions are employed in the reference signal to improve the power factor (PF) and total harmonic distortion (THD) of the buck and buck-boost converters. The design ensures that the peak of the inductor current maintains a constant level that is invariant for different AC line voltages. The operating mode of the design can be changed between PWM and PFM. The LED driver has been implemented in a 130-nm CMOS process. PF and THD are improved when the proposed reference is employed, and peak PF and lowest THD are

0.995/0.983/0.996 and 7.8/6.2/3.5% for the buck (PWM), buck (PFM), buck-boost (PFM) cases, respectively. The corresponding peak efficiency for the three cases is 88/92/91%, respectively.

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Chapter 1

Introduction

Growth in worldwide consumer electronics and the home automation market with smart technologies, where an object can communicate autonomously and become a node in a network, is accelerating rapidly. Smart technologies are leading to a convergence of diverse electronic systems for computing, communications and consumer applications. Efficiency is critical in several smart applications, which has fueled a demand for efficient power conversion and delivery techniques.

Deep sub-micron CMOS scaling has enabled integration of functionality, reduction of cost and also enhanced efficiency of digital circuits, through voltage scaling. Classical analog design techniques do not typically benefit from process scaling, due to lower supply voltages. Thus the use of digitally-intensive switching circuits and techniques is preferable, when possible.

This research investigates the design of integrated circuits for power delivery using switching techniques, spanning switching frequencies from tens of kHz to GHz. The proposed techniques are based on pulse-width-modulation (PWM) and include the applications such as LED drivers, base-band signal amplifiers for audio applications and power-line communications, and wireless

RF systems.

1.1 ICs for Efficient Power Delivery in Home Automation Applications

Home automation is an example of a smart system (Fig. 1.1). Such a system could, for instance, be used to control the ambient temperature and light levels in a home automatically by observing the real-time environment. In addition, the user can also observe the outside as well as the inside of a house from anywhere, in real-time. Remote access and control can be accomplished through a smart phone or a mobile device by using wireless communications. The appliances in the home automation system can also communicate using power-line communications as well as wireless communications.

For such an application, different kinds of efficient power delivery ICs are required. Efficient wireless transmitters are required for the communication systems that are employed, e.g., in home Wi-Fi systems and smart phones. These are also required in appliances such as televisions, refrigerators and dryers, that have recently started to support Wi-Fi capability for smart functionality. The wireless systems typically employ GHz frequencies to deliver signals up to several tens of MHz bandwidth.

Efficient baseband signal amplification and power delivery techniques are critical in audio applications and power-line communication (PLC) transmitters. The PLC system employs existing power lines for bi-directional communications. PLC is an integral part of the smart-grid concept that intelli-

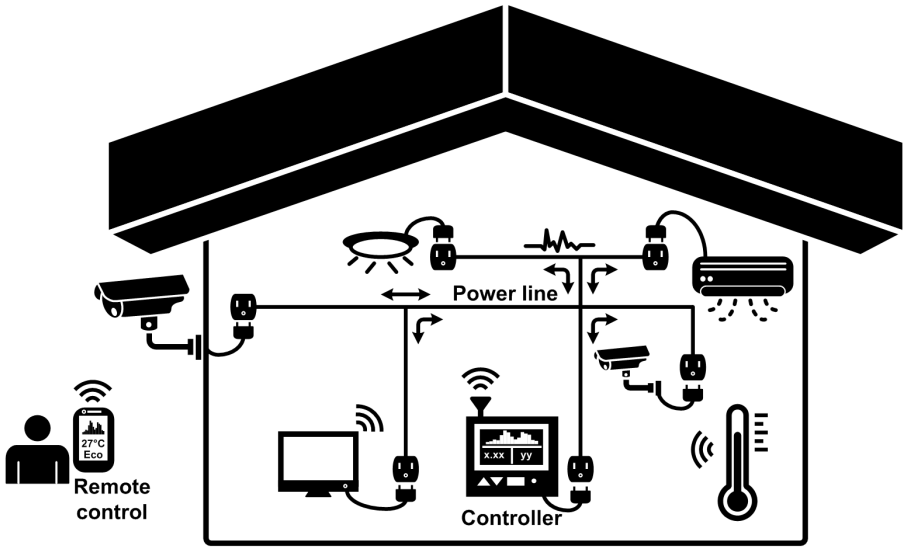


Figure 1.1: An example of a home automation system.

gently monitors and communicates information regarding energy flow, in order to enhance the efficiency and reliability of power delivery. The signal bandwidth of narrowband PLC is up to 500 kHz and it is intended for applications that require long-range communication with data rates of the order of kbps to several hundreds of kbps. An audio system drives a modulated signal of bandwidth up to 20 kHz and requires high dynamic range (DR) to provide high quality sound. Thus, a switching-type base-band signal amplifier employs switching frequencies that range from a few hundreds of kHz to a few tens of MHz.

Another example of an application requiring highly efficient amplification is smart lighting, e.g., for LED drivers. Home appliance applications usually employ power factor correction (PFC) circuits and DC-to-DC converters

to provide the desired DC supply voltage. Power factor (PF) is an important metric that determines how efficiently electrical power from an AC outlet is being used. In addition, total harmonic distortion (THD) is another important metric. A high THD is not acceptable since it causes interference with other electronic systems and also shortens the life span of equipment. The switching frequency for LED lighting drivers is usually several tens of kHz since the input voltage signal is the 110Vac or 220Vac supply that employs sinusoidal signals with 50-60 Hz carrier frequency.

1.2 Power Amplifiers

Power amplifiers (PA) are a critical part of power delivery in many applications, and are also the dominant factor in determining the efficiency of the implementation. The efficiency challenge is even more severe in systems where the instantaneous amplitude of the signal can vary over a large range, for example in modern communication systems, high-order modulation schemes such as orthogonal frequency division multiplexing (OFDM) are often used that have a large peak-to-average power ratio (PAPR). In such cases, PA efficiency in back-off operation as well as at peak power is important. The PA can be a linear type or a switching type design. Linear PAs such as class-A and class-B designs provide good distortion performance and moderate peak efficiency. However these are not well-suited for applications with high PAPR since efficiency degrades rapidly as the output power is backed-off. Class-A designs have an efficiency that degrades as the square of the amplitude, while

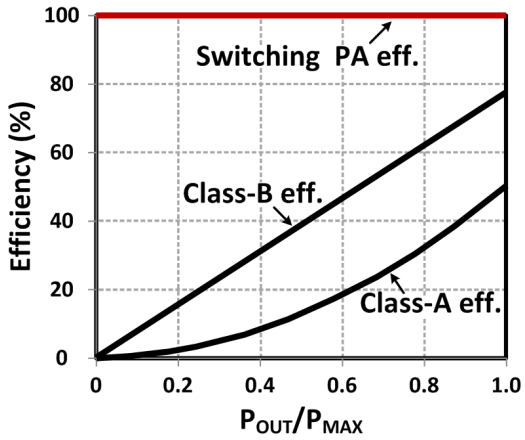


Figure 1.2: Theoretical efficiency of PAs.

reaching a peak value of 50% with an inductive load. The efficiency of class-B designs degrades in proportion to the output amplitude, with a theoretical peak efficiency of 78%.

Digitally-intensive switching PAs have better efficiency than linear PA designs due to saturated operation, and hence are very attractive. Theoretically, switching PAs achieve 100% efficiency regardless of back-off power level (Fig. 1.2). However, in practice, the efficiency is degraded by (a) the switching loss caused by parasitic capacitance; (b) the conduction loss due to finite on-resistance of switches; and (c) shoot-through current from power to ground. Nevertheless, switching PAs still show higher efficiency than linear PAs. Furthermore the designs allow for utilization of deep sub-micron CMOS technologies and enables integration of PAs along with digital circuits. Digital approaches also benefit from process scaling, in performance as well as in area.

1.2.1 Linear PAs

Fig. 1.3 shows the types and operation of linear PA. In a class-A PA, the transistor (M_1), which can be BJT, FET, or IGBT, conducts current at all times, in order to achieve high linearity. The bias voltage at the input of the transistor has to be chosen to be larger than the threshold or ON voltage of the transistor in order to ensure that the amplifier provides linear gain. However, as the transistor is always ON, it is constantly conducting current, which causes a continuous dissipation of power in the amplifier.

A class-B PA is biased around the threshold of the transistor and only conducts current for half of the cycle. Unlike a class-A PA, there is no DC bias-current, due to which the static power loss is reduced. By employing a push-pull configuration (Fig. 1.3b), which can be implemented using two transistors with complimentary inputs, a complete waveform can be driven at the output.

The two complimentary transistors in a class-B push-pull design cannot turn ON and OFF seamlessly, due to the threshold voltages of the transistors, which causes a dead-zone. The dead-zone leads to distortion at the zero-crossing point of the waveform. A class-AB PA is commonly used to avoid the crossover distortion at the zero-crossing point. A class-AB PA conducts current for a duration that is slightly more than the half-cycle that is employed in class-B designs. However this duration is much less than the full cycle of conduction that is employed in class-A amplifiers.

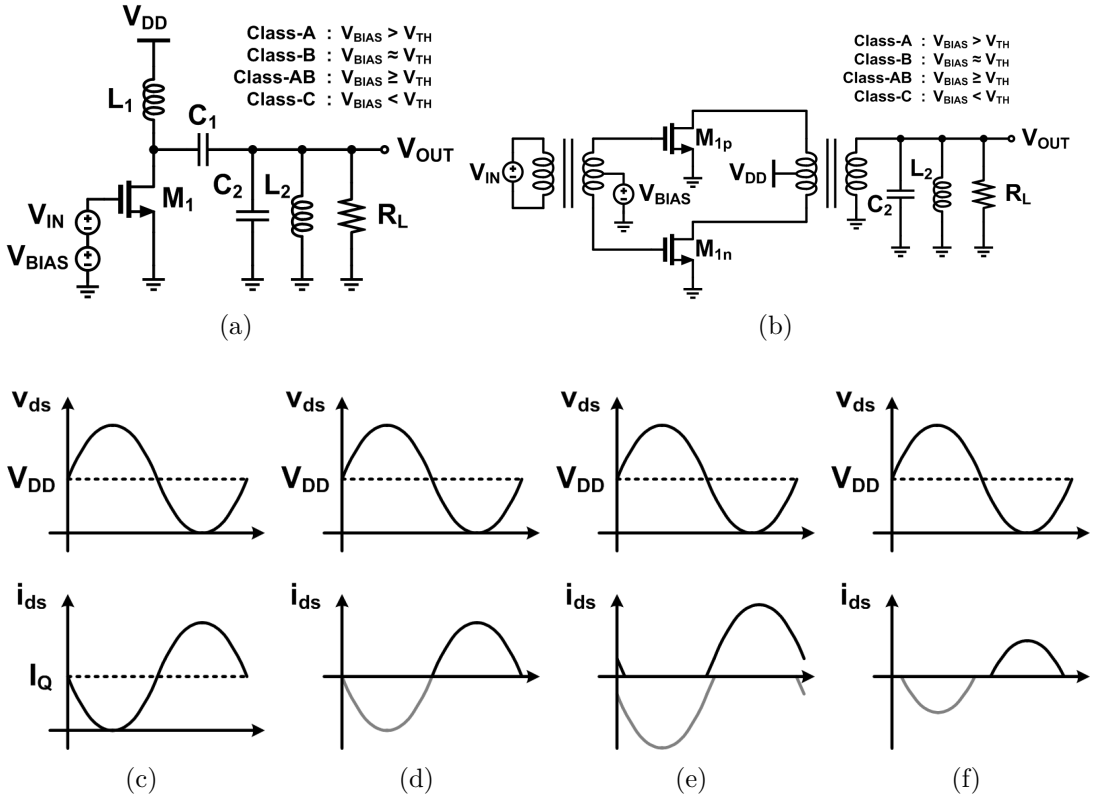


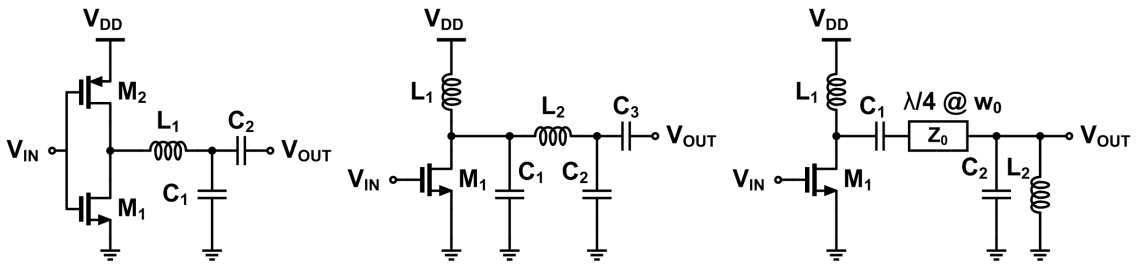
Figure 1.3: (a) Linear PA. (b) Push-pull linear PA. (c) Class-A operation. (d) Class-B operation. (e) Class-AB operation. (f) Class-C operation.

In a class-C PA, the input of the transistor is biased lower than the threshold voltage and conducts current for less than half of the cycle. A class-C PA design can achieve the highest efficiency of all linear PA topologies, however, it also exhibits the worst linearity. Thus, it suitable for constant amplitude modulation schemes such as frequency modulation (FM), or phase modulation (PM). Furthermore, higher efficiency is achieved as the output power is reduced.

1.2.2 Switching PAs

Fig. 1.4 shows the types of switching PAs. In each case, the input of the switching PA is a pulse-train which switches between the supply voltage (VDD) and the ground reference (GND). The class-D amplifier (Fig. 1.4a) is the simplest configuration that consists of a sourcing transistor (M_2) and a sinking transistor (M_1), followed by a low-pass filter for baseband amplifier applications, or a band-pass filter for RF transmitter applications. A class-D PA is commonly used for PWM operation because it guarantees high efficiency regardless of duty-cycle. However, the efficiency is degraded at high switching frequencies because the output node is charged and discharged through the transistors in each cycle.

A class-E PA (Fig. 1.4b) employs zero voltage switching, which ensures that the drain voltage and current waveforms do not overlap in time. Thus, it does not suffer from switching loss at the output node. However, the peak drain voltage of the transistor in a class-E PA increases significantly due to



(a) (b) (c)

Figure 1.4: Switching PA. (a) Class-D. (b) Class-E. (c) Class-F.

the shaping provided by the resonant network. Consequently, due to device breakdown considerations, a class-E PA cannot use the maximum supply voltage that is available in a given CMOS process, leading to a decrease in the output power.

A class-F PA (Fig. 1.4c) employs an output matching network that presents the device with a high impedance at odd harmonics and a low impedance for even harmonics of the switching frequency. Ideally, the switching transistor, M_1, in a class-F PA does not dissipate power since a square voltage waveform is observed at the drain, and the half-wave rectified output current only flows when the drain voltage is low. In practice, only a limited number of harmonic frequencies can be terminated since the harmonic termination network requires a large area. This imposes a practical limit on the efficiency enhancement available in class-F designs.

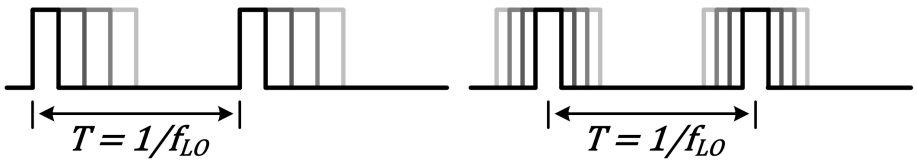
Class-E and class-F PAs show optimal performance for a constant duty-cycle input. For PWM signaling, a class-D PA topology is the most suitable, since it can ideally operate for any input duty-cycle.

1.3 Pulse-Width-Modulation

A switching PA provides constant-amplitude output levels. Thus pulse-width modulation (PWM) with discrete signal levels, where the signal information is encoded in the pulse-width, or duty-cycle, is often used with switching PAs. PWM can be employed for baseband as well as RF signal amplification. In a typical PWM signal, the amplitude information of the input is represented by the local duty-cycle of a periodic pulse waveform that has a much higher frequency than the signal information. The duty cycle is varied while keeping the leading or falling pulse edge of the PWM pulse train periodic as shown in Fig. 1.5a. As such the waveform lacks phase information. The output signal is observed in the baseband component of the pulse train, and other harmonics are removed by a low-pass filter (LPF).

In RF-PWM, the pulse train is synchronized at the mid-point of the pulses and both amplitude and phase are variable, as depicted in Fig. 1.5b. The amplitude is varied by varying the fractional pulse-width, or duty-cycle, relative to the mid-points of periodic pulses, while the phase is varied by changing the pulse position, relative to the prior pulse [1, 2]. The output is observed directly at the fundamental frequency of the pulse train and other harmonics are removed by a band-pass filter (BPF).

Both PWM and RF-PWM can be used for baseband signal amplification because the DC component in both types of signals is proportional to the duty-cycle. However, only RF-PWM is appropriate for up-converting the baseband signal to RF. Assuming an input signal of X_{IN}, and a carrier



(a) (b)

Figure 1.5: (a) Typical PWM. (b) RF-PWM.

switching frequency of f_{LO}, the PWM component at f_{LO} can be represented as below,

$$V_{OUT-PWM}^{(f_{LO})} = K_1 \cdot \sum_{m=\pm 1}^{\infty} \frac{J_1(\pi|X_{IN}(t)|)}{m\pi} \cdot sin(\frac{m\pi}{2}) \cdot cos(2\pi f_{LO}t + mX_{IN}(t)) \quad (1.1)$$

where J_1 is the 1$^{\text{st}}$-order Bessel function, and K_1 is a constant factor related to the supply voltage. It can be observed that the output contains several intermodulation terms at harmonics of $X_{IN}(t)$.

RF-PWM at f_{LO}, on the other hand, has only a sine relationship between X_{IN} and V_{OUT} that can be represented as below,

$$V_{OUT-RFPWM}^{(f_{LO})} = K_2 \cdot sin(X_{IN}(t)) \cdot cos(2\pi f_{LO}t) \quad (1.2)$$

where K_2 is a constant factor representing the supply voltage. Thus, RF-PWM signal is appropriate for an RF-signal driver because the RF-PWM signal directly upconverts the baseband signal to f_{LO}, if the baseband signal is pre-distorted with an arc-sin function, and does not contain distortion products

of the input signal, around the carrier frequency.

Fig. 1.6 shows the FFT results of PWM and RF-PWM at DC and f_{LO}. A 100 kHz baseband sinusoidal input is modulated by PWM as well as RF-PWM and observed at DC. Both cases show the 100 kHz baseband tone and a relatively flat out-of-band noise level because the DC output is proportional to the duty cycle. In Fig. 1.6c and Fig. 1.6d a 10 MHz baseband signal is modulated using PWM and RF-PWM with arcsin predistortion, respectively, and observed at f_{LO}. RF-PWM shows the RF signal at $f_{LO} \pm 5MHz$ with relatively clean out-of-band noise while PWM exhibits a large number of harmonics around the signal bandwidth.

1.4 PWM Applications

PWM is employed in multiple applications and it can be categorized by the I/O signal type and switching frequency, as shown in Fig. 1.7. The I/O signal type can be a time-varying signal such as the AC line, or a modulated signal, or it can be a DC value.

If the I/O signal is DC, power efficiency and dynamic response of the input, and output regulation are important factors. Switching frequency is determined by the I/O voltage level in order to enhance the efficiency. If the input DC voltage is high, e.g., $>$ 50V, in order to provide a correspondingly high power, a low switching frequency is used which is below hundreds of kHz, because of large switching loss caused by the high voltage input. In this case, large passive components such as inductors and capacitors are required.

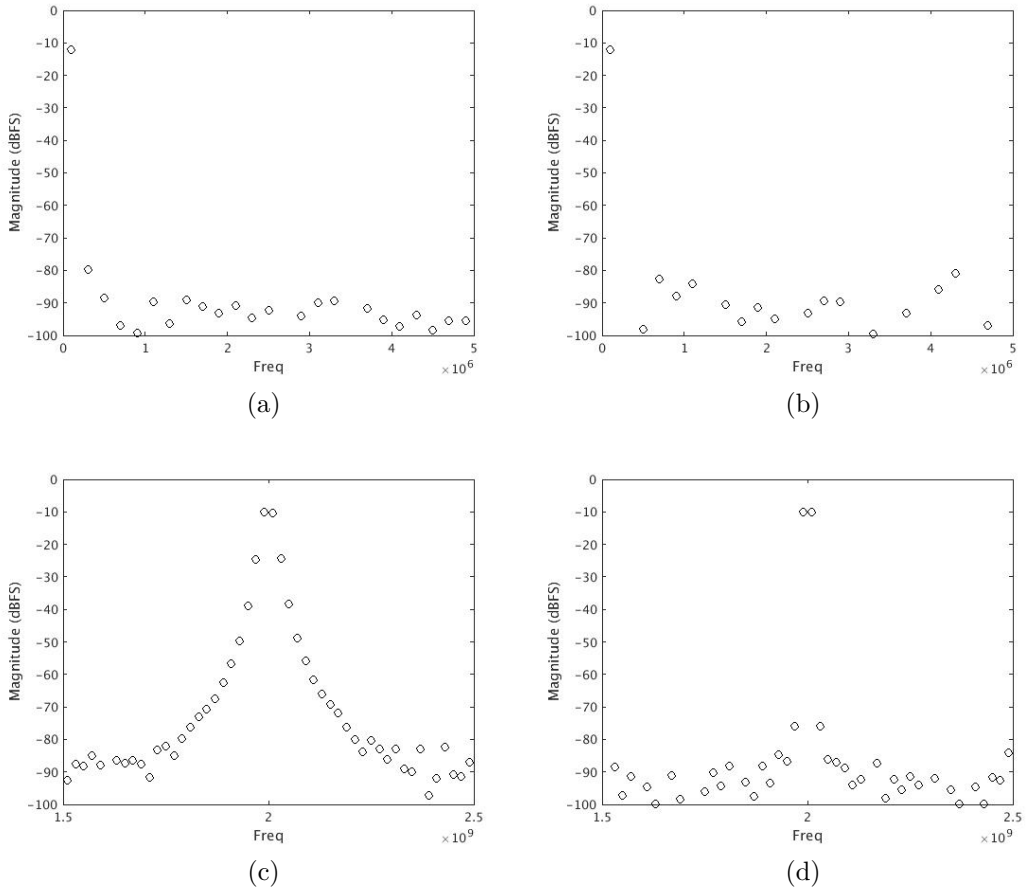


Figure 1.6: PWM vs. RFPWM. (a) PWM at DC (100 kHz sinusoidal input, no predistortion). (b) RF-PWM at DC (100 kHz sinusoidal input, no predistortion). (c) PWM at f_{LO} (10 MHz sinusoidal input, arcsin predistortion). (d) RF-PWM at f_{LO} (10 MHz sinusoidal input, arcsin predistortion).

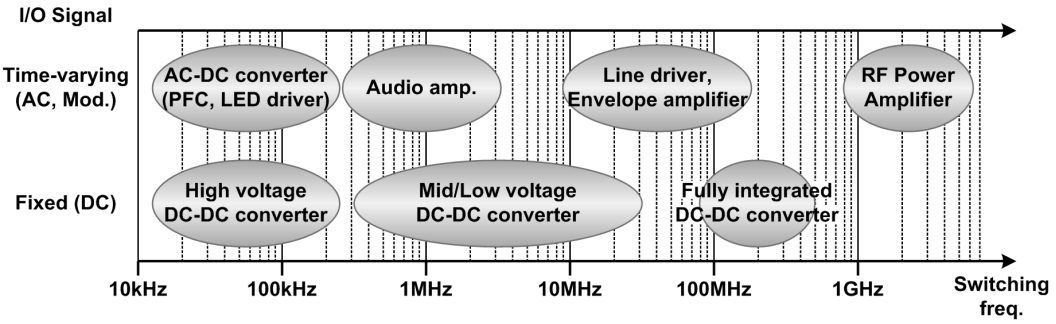


Figure 1.7: PWM applications vs. Switching frequency.

Mid/Low voltage DC-to-DC converter usually switch from hundreds of kHz to tens of MHz. This voltage range is commonly used for internal supplies in consumer electronics products. A high switching frequency around or above 100 MHz is used for fully integrated monolithic DC-to-DC converters because high switching frequency operation can help to reduce the size of the peripheral circuits and make the design easy to integrate. The power level is such designs is typically the lowest.

With I/O signals that are time-varying, power-efficiency, system-linearity, and wide bandwidth operation are important and the switching frequency is usually determined by the input voltage level and the bandwidth of the input. AC-to-DC converters which are used to convert the AC outlet voltage (e.g. 110Vac or 220Vac) to a DC output, employ a low switching frequency because of the high input voltage level. Audio amplifiers employ switching frequencies around or below 1 MHz, since the bandwidth of sound is up to 20 kHz. A switching frequency above 10 MHz is required for wider bandwidth applications such as power-line communications or envelope amplifiers for RF

transmitters. Achieving sufficiently low distortion at such high switching frequencies can be challenging. A switching-frequency around or above a GHz is used for RF power amplifiers. The switching frequency is determined by the specification of communication standards.

1.5 Thesis Contributions

The main emphasis of this research is on exploring circuit techniques and architectures for power delivery ICs using PWM in order to improve the efficiency and circumvent the limitations of conventional architectures. Class-D PAs are used in the proposed architectures which benefit from process scaling and also offer ease of integration. Moreover, class-D PAs are the most suitable configuration for PWM because they provide high efficiency regardless of duty-cycle.

PWM architectures using different frequency ranges from kHz to GHz are explored. Different PWM techniques are proposed for wireless transmitters in the GHz range, baseband amplifiers in the MHz range, and LED drivers in the kHz range.

A digitally-intensive transmitter using RF-PWM with a class-D PA is described in chapter 2 [2, 3]. The use of carrier switching for alleviating the dynamic range limitation that can be observed in classical RF-PWM implementations is introduced. The approach employs full carrier frequency for half of the amplitude range, and the second harmonic of half of the carrier frequency, for the remainder of the amplitude range. This concept not only allows

the transmitter to drive modulated signals with large PAPR but also improves back-off efficiency due to reduced switching losses in the half carrier-frequency mode. A glitch-free phase selector is proposed that removes the deleterious glitches that can occur at the input data transitions. The phase-selector also prevents D flip-flop setup-and-hold time violations. The transmitter has been implemented in a 130-nm CMOS process. The measured peak output power and power-added-efficiency (PAE) are 25.6 dBm and 34%, respectively. While driving 802.11g 20-MHz 64-QAM OFDM signals, the average output power is 18.3 dBm and the PAE is 16% with an EVM of -25.5 dB.

A high-speed driver that provides a pulse-width modulated output while using a class-D PA is described in chapter 3 [4]. A PLL-based architecture is employed which eliminates the requirement for a precise ramp or triangular signal generator, and a high-speed comparator, which are typically used in PWM generation. Multi-level signaling is proposed to enhance back-off as well as peak efficiency, which is critical for signals with high PAPR. A differential, folded PWM scheme is introduced to achieve highly linear operation. 3-level operation is achieved without the requirement for additional supply source or sink paths while 5-level operation is achieved with an additional supply source/sink path compared to 2-level operation. The PWM driver has been implemented in a 130-nm CMOS process and can operate with a switching frequency of 40-to-170 MHz. For 2/3/5-level PA operation, with a 500 kHz sinusoidal input and 60 MHz switching frequency, the measured THD is -61/-62/-53 dB and corresponding efficiency is 71/83/86% with

175/200/220 mW output power level, respectively. Performance has also been verified for the 2/3-level PA with a high PAPR signal with 500 kHz bandwidth. While intended as a general purpose amplifier, the approach is well-suited for applications such as PLC.

An efficient buck/buck-boost reconfigurable LED driver that supports PWM and PFM operation is introduced in chapter 4. The driver is based on peak current control. Rectified sin as well as $\sin^2$ functions are employed in the reference signal to improve the PF and THD of the buck and buck-boost converters. The design ensures that the peak of the inductor current maintains a constant level that is invariant for different AC line voltages and the number of LEDs. The LED driver has been implemented in a 130-nm CMOS process and operating mode can be changed between PWM and PFM. PF and THD are improved when the proposed reference is employed, and peak PF and lowest THD are 0.995/0.983/0.996 and 7.8/6.2/3.5% for buck (PWM), buck (PFM), buck-boost (PFM) cases, respectively. In addition, the peak efficiency is 88/92/91% for buck (PWM), buck (PFM), buck-boost (PFM) cases, respectively.

Chapter 5 provides conclusions, and suggests open problems for future research related to this work.

Chapter 2

A RF-PWM Wireless Transmitter with a Class-D Power Amplifier[1]

2.1 Introduction

Monolithic RF system-on-chip (SOC) implementations are highly desirable for reducing component size and enhancing efficiency in portable wireless communication systems. Most RF circuits can be readily implemented in deep submicron CMOS. Power amplifier (PA) implementations are however challenging due to the requirements for high breakdown voltage and high output power. Furthermore, in modern digital communication systems, high-order modulation schemes such as orthogonal frequency division multiplexing (OFDM) are often used that have a large peak-to-average power ratio (PAPR). Consequently, PA efficiency in back-off operation as well as at peak power is important. While linear-mode PAs such as class A and class B designs provide good distortion performance and moderate peak efficiency, these are not well-suited for applications with high PAPR since efficiency degrades rapidly as the

[1]This chapter is based on reference [2] (K. Cho and R. Gharpurey, "A digitally intensive transmitter/PA using RF-PWM with carrier switching in 130 nm CMOS," IEEE J. Solid-State Circuits, vol. 51, pp. 1188-1199, May 2016, ©2016 IEEE). Kunhee Cho was responsible for the design, implementation and measurement of the transmitter IC described in this publication.

output power is backed-off. Class-A designs have an efficiency that degrades as the square of the amplitude, while reaching a peak value of 50% with an inductive load. The efficiency of class-B designs degrades in proportion to the output amplitude, with a theoretical peak efficiency of 78%[2].

Digitally-intensive switching power amplifiers are very attractive because they have better efficiency compared to linear power amplifier designs due to saturated operation. Switching PAs also allow for utilization of deep submicron CMOS technologies and enable integration of RF PAs along with digital baseband and application processors. Digital approaches also benefit from process scaling, in performance as well as in area.

Switching PAs operate with discrete amplitude levels. To accommodate a time-varying amplitude, transmitter techniques such as elimination and restoration (EER) and Polar architectures can be employed. These techniques decompose the input into amplitude and phase components [5, 6, 7]. The input to the switching PA is simply the phase-modulated signal, while the supply voltage of the PA contains information regarding the amplitude-modulated component of the input. In theory, such techniques can significantly enhance efficiency over basic quadrature (I-Q) modulators, since the PAs can be operated in saturation, and hence provide high efficiency. A key challenge in these approaches is that they require additional digital-to-analog converters (DAC) and high-efficiency supply modulators with adequate bandwidth, to provide

[2]We note that the practically achievable peak efficiency of class-A and class-B designs at RF bands is significantly lower than the theoretical maximums.

the amplitude information on the supply. A major challenge also arises from the difficulty in aligning the amplitude and phase path delays, especially over wide frequency-bands.

To avoid the requirement for DACs and supply modulators, digitally-modulated (digital polar) PA approaches have been proposed [8, 9, 10, 11, 12]. The envelope information is represented by varying the number of PAs instead of employing DACs and supply modulators. However, this also faces the requirement for amplitude and phase alignment.

An efficient alternative is a Digital Outphasing architecture. In this approach, the PA input signal is decomposed into two constant amplitude components that are applied to independent switching PAs, whose outputs are combined [13, 14, 15, 16]. This approach does not require alignment of phase and amplitude signals in the two paths, which is key advantage compared to the above architectures. On the other hand, it requires an efficient combiner network after the PA. Moreover, a pair of PAs is required to generate a single RF output.

RF pulse-width-modulation (RF-PWM) is a concept wherein the amplitude and phase components of an input signal are represented by the pulse width and pulse position of a periodic pulse train, respectively [1, 17, 18]. This scheme can be implemented using outphasing by placing the combiner before the PA as shown in [1]. Unlike typical digital outphasing architectures, the combiner circuit can be easily implemented using digital logic. RF-PWM does not require efficient, high-bandwidth supply modulators either. The dynamic

range of RF-PWM on the other hand, can decrease as the carrier frequency is increased, since the signal pulse-width can become sufficiently narrow that the duty cycle at the output of the switching PA stage is unable to linearly track the input duty-cycle. This limits the PAPR of the modulation that can be applied to the PA for a required distortion level. This issue arises due to parasitic capacitance at the output of driver and PA stages. As the carrier-frequency increases, the minimum pulse-width becomes a larger fraction of the switching period. Thus the maximum PAPR that can be handled by the RF-PWM output stage degrades with increasing frequency. In any given technology node, this introduces a trade-off between the maximum carrier-frequency and the PAPR of the modulation scheme.

In this chapter, we describe an RF-PWM transmitter architecture that avoids the problem of narrow-pulses, and the related dynamic range limitation, by employing carrier-switching [2, 3]. The RF-PWM signal employs the fundamental component of the carrier frequency (f_{LO}), similar to classical RF-PWM, for large amplitudes. For small-amplitudes, where the narrow-pulse issue can arise, the transmitter switches to employing the 2^{nd} harmonic of half of the carrier frequency ($f_{LO}/2$), which is also at f_{LO}. The RF-PWM generator drives class-D PA stages, which are reconfigured based on the amplitude level to provide either the fundamental or the second harmonic of the output. As described below, the minimum amplitude that can be observed in the system is significantly smaller in this case. A second benefit provided by the approach is that for low-power operation, since the transmitter operates at half of f_{LO},

the switching loss is also reduced. This boosts the efficiency for low output power levels.

Since RF-PWM is employed, and the duty-cycle is not constant, a class-D switching stage is employed instead of class-E. This reduces the matching requirement on the output stage. This aspect of the class-D output can be exploited for multi-band and multi-mode operation.

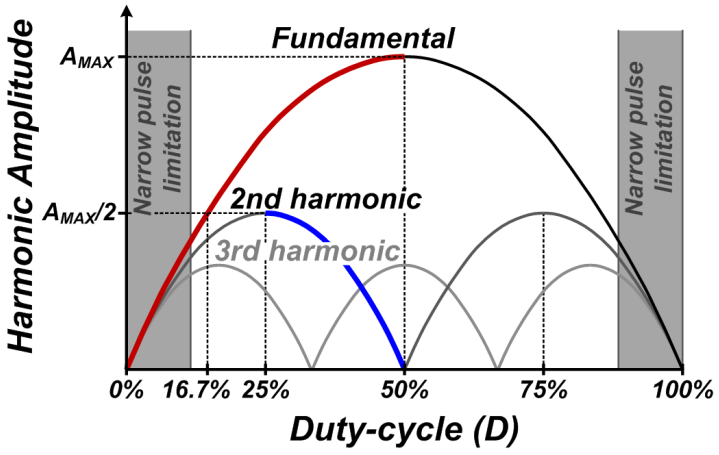
2.2 RF-PWM with Carrier Switching

2.2.1 RF Pulse-Width-Modulation

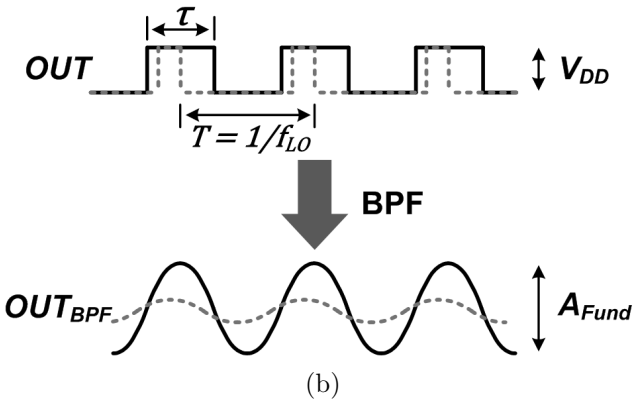
In baseband PWM, the amplitude information of the input is represented by the local duty cycle of a periodic pulse waveform that has a much higher frequency than the signal information. The duty cycle is varied while keeping the leading or falling pulse edge, or the mid-point of the PWM pulse train periodic. As such the waveform lacks phase information. The output signal is observed in the baseband component of the pulse train.

In RF-PWM, both amplitude and phase are variable. Amplitude is varied by varying the fractional pulse-width, or duty-cycle, relative to the mid-points of periodic pulses, while the phase is varied by changing the pulse position, relative to the prior pulse [1]. The output is observed directly at the fundamental frequency of the pulse train.

The amplitude of specific harmonics as a function of the duty-cycle (D) of RF-PWM is shown in Fig. 2.1a. The amplitude of the N^{th} harmonic



(a)



(b)

Figure 2.1: (a) Harmonic amplitude of periodic pulse train. (b) RF pulse-width-modulation.

component of the PWM signal with carrier frequency f_{LO}, for a duty-cycle of D between 0 and 100% can be represented by,

$$A_N^{(f_{LO})} = \frac{4}{N\pi} V_{DD} \times sin(N\pi \cdot D) = \frac{A_{MAX}}{N} \times sin(N\pi \cdot D) \tag{2.1}$$

where V_{DD} is the amplitude of pulse train. The amplitude is independent of the carrier frequency f_{LO}. In classical RF-PWM, only the fundamental term is used and the other harmonics are removed by a bandpass filter. The amplitude of the fundamental term in the RF-PWM output is given by,

$$A_1^{(f_{LO})} = \frac{4}{\pi} V_{DD} \times sin(\pi \cdot D) \tag{2.2}$$

The peak output power is achieved when the duty-cycle is 50%. This corresponds to the amplitude $A_{MAX} = (4/\pi)V_{DD}$. For smaller and larger values of the duty-cycle, the output power decreases following the sinusoidal relationship of Eq. 2.2. Fig. 2.1b depicts amplitude modulation (AM) generation by changing the duty-cycle, and phase modulation (PM) by varying the pulse position. For a carrier frequency significantly greater than the modulation bandwidth, both amplitude and phase information can be represented with high accuracy.

2.2.2 Dynamic Range Limitation in RF-PWM

In theory, RF-PWM can employ a duty-cycle in the range from 0 to 50% to span an amplitude from 0 to A_{MAX}. In an ideal PA, the duty-cycle of the output is identical to that of the input RF-PWM signal. However, in a practical PA, as the input duty-cycle becomes smaller, the output duty-cycle is unable to follow linearly. This is due to parasitic capacitance, and finite current drive capability of the PA devices. This narrow pulse limitation not only limits the peak-to-average of RF-PWM signal and but also degrades linearity in high PAPR signals. The narrowest achievable pulse width is determined by the effective fan-out[3] of the driver and the output stage, as well as the process. A small fan-out makes it possible to drive a narrow pulse width, however, this leads to a lower efficiency. Employing an advanced process node on the other hand, improves both the dynamic range and the efficiency. Fig. 2.2 shows the calculated dynamic range of RF-PWM when the available minimum pulse width is 50ps. The dynamic range is reduced as the carrier frequency is increased because the minimum duty-cycle of the output, or equivalently the minimum output power, is increased. The calculated dynamic range is 8.7 dB at 2.4 GHz carrier frequency.

[3]The effective fan-out of a switching-stage is given by the ratio of the size of the stage it drives, to its own size.

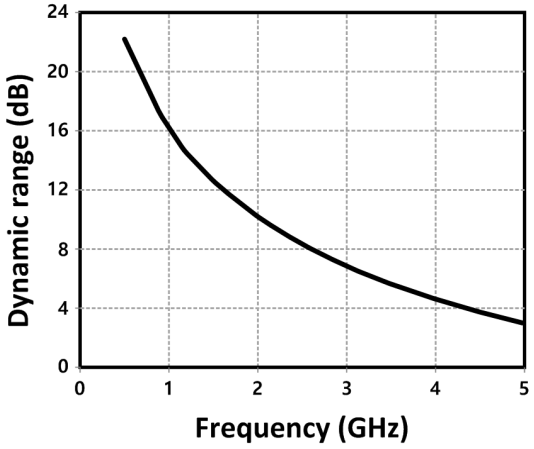


Figure 2.2: Calculated dynamic range of RF-PWM (Minimum pulse width of 50ps).

2.2.3 RF-PWM with Carrier Switching

RF-PWM with carrier-switching is proposed to avoid the narrow pulse limitation of RF-PWM. The carrier -switching concept employs not only the fundamental components at f_{LO}, but also the 2$^{\text{nd}}$ harmonic of the carrier frequency $f_{LO}/2$, which also coincides with f_{LO}. The 2$^{\text{nd}}$ harmonic is given by,

$$A_2^{(f_{LO})} = \frac{2}{\pi} V_{DD} \times sin(2\pi \cdot D) \tag{2.3}$$

From Fig. 2.1a, we observe that:

1. The peak amplitude of the 2$^{\text{nd}}$ harmonic of $f_{LO}/2$, $A_2^{(f_{LO}/2)}$, is the same as half of the peak amplitude ($A_{MAX}/2$) of the fundamental component for a carrier-frequency at f_{LO}, $A_1^{(f_{LO})}$;

2. For D in the range from 0 to 1/4, $A_2^{(f_{LO}/2)}$ is identical for a duty-cycle

of D and $0.5 - D$; and

3. The fundamental amplitude with a carrier of f_{LO}, $A_1^{(f_{LO})}$, for $D = 1/6$ or 0.167 is $A_{MAX}/2$, which equals $A_2^{(f_{LO}/2)}$ for $D = 0.25$.

Based on the above, the following approach is used to avoid the narrow-pulse limitation:

RF amplitude from $A_{MAX}/2$ to A_{MAX}: The transmitter employs the fundamental component of the carrier frequency f_{LO}. The RF amplitude is given by,

$$A_1^{(f_{LO})} = A_{MAX} \times sin(\pi \cdot D) \tag{2.4}$$

where the duty-cycle D varies from 0.167 to 0.5.

RF amplitude from 0 to $A_{MAX}/2$: The transmitter employs the 2nd harmonic with a carrier frequency of $f_{LO}/2$. For a duty-cycle of D with the carrier at $f_{LO}/2$, the RF amplitude is given by,

$$A_2^{(f_{LO}/2)} = \frac{A_{MAX}}{2} \times sin(2\pi \cdot D) \tag{2.5}$$

where D varies from 0.5 to 0.25. Fig. 2.3 shows the input amplitude versus duty-cycle and pulse-width of the PWM signal using carrier switching.

The output in either mode is observed at f_{LO}. By using the above approach, the output signal path never experiences a pulse width with a duty

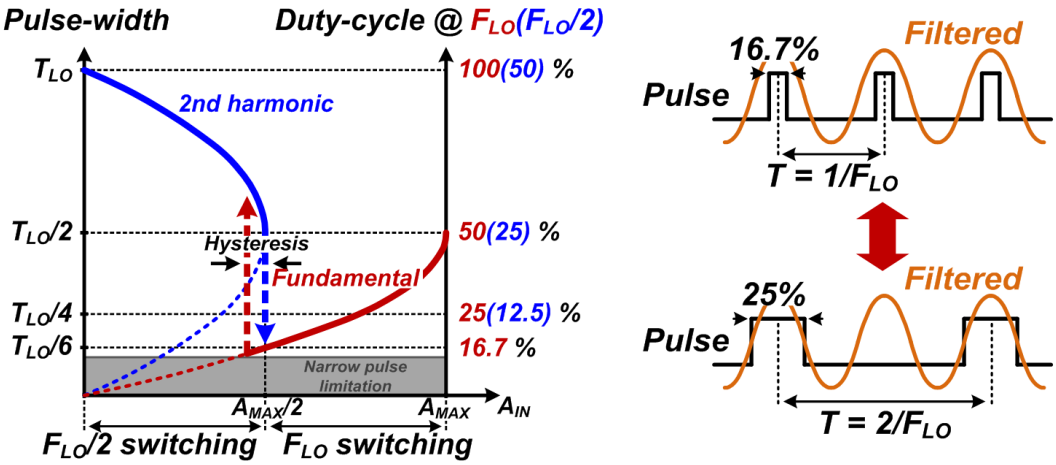


Figure 2.3: RF-PWM with carrier switching.

Mode	Full-carrier switching mode	Half-carrier switching mode
Amplitude range	A_{MAX}–$A_{MAX}/2$	$A_{MAX}/2$–0
Operating frequency	f_{LO}	$f_{LO}/2$
Harmonic component	Fundamental	2^{nd} harmonic
Duty-cycle range (%)	16.7-50	25-50
Pulse-width range	$T_{LO}/6 - T_{LO}/2$	$T_{LO}/2 - T_{LO}$

Table 2.1: Description of mode-switching.

cycle approaching zero. In fact, the smallest pulse width is $0.167 \cdot T_{LO}$. Furthermore, for small amplitudes, the output stage switches at a lower frequency. As such the switching loss, fCV_{DD}^2, is halved. Thus the approach also enhances efficiency. Table 2.1 provides a summary of the operating conditions for each switching mode.

2.2.4 Predistortion

The RF amplitudes at f_{LO} in the half and full-carrier modes both have a non-linear dependence on the duty-cycle D. For ensuring linear modulation, both $A_1^{(f_{LO})}$ and $A_2^{(f_{LO}/2)}$ must be linearly dependent on the baseband amplitude, termed A_{BB}, in their respective modes. The RF-PWM duty-cycle D is predistorted, and made to depend non-linearly on A_{BB}, in order to ensure a linear transmitter response at the output.

A_{BB} from $A_{MAX}/2$ to A_{MAX} (full-carrier switching mode): The duty cycle is predistorted such that

$$D = \frac{1}{\pi} sin^{-1}(V_{BB}/V_{MAX}). \tag{2.6}$$

This ensures, based on Eq. 2.2, that the fundamental RF-PWM component, $A_1^{(f_{LO})} \propto A_{BB}$ is in the range from $0.5A_{MAX}$ to A_{MAX}, and D is in the range from 0.167 to 0.5.

A_{BB} in the range 0 to $A_{MAX}/2$ (half-carrier switching mode): The RF-PWM duty cycle is predistorted such that,

$$D = \frac{1}{2} - \frac{1}{2\pi} sin^{-1}(2V_{BB}/V_{MAX}). \tag{2.7}$$

This ensures, from Eq. 2.3, that $A_2^{(f_{LO}/2)} \propto A_{BB}$ is in the range from 0 to $0.5A_{MAX}$, and D is in the range from 0.5 to 0.25.

The above discussion assumes a single transition point between the two

modes. In practice, the transition involves a hysteresis, wherein the transmitter is kept in the full-carrier mode for an output that is slightly smaller than $A_{MAX}/2$, before it is switched to the half-carrier mode. The full-carrier mode predistortion function of Eq. 2.6 is also applied to the output range in the hysteresis region.

2.3 Complete Transmitter Architecture

Two topologies have been proposed to generate a RF-PWM signal. One is based on the use of an analog comparator [18] while the other is based on digital outphasing [1]. RF-PWM generation based on an analog comparator has the benefit that the signal is not quantized and hence there is no associated out-of-band quantization noise. However, this architecture requires a very high-speed and accurate analog comparator which is difficult to implement in CMOS technologies for driving signals in the GHz frequency-range. Furthermore, the signal bandwidth is limited. Therefore, outphasing is employed to implement RF-PWM with carrier switching. Fig. 2.4 shows the principle of the outphasing scheme [19]. The output is obtained by combining two 50% duty-cycle phase-modulated square-wave signals (Φ_1 and Φ_2). Each of outphased signals is generated by a phase modulator. In the architecture described here, a single phase modulator, with two phase selector paths, generates Φ_1 and Φ_2 simultaneously.

Typical digital outphasing architectures combine the two outphased signals after the PAs, which requires an efficient combiner network (Fig. 2.5a)

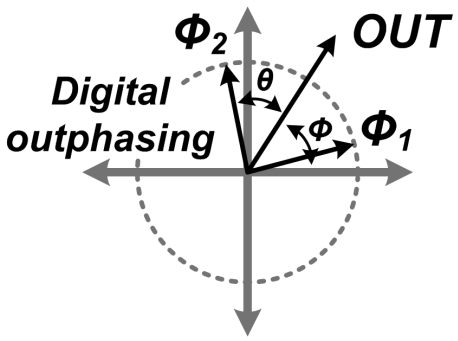


Figure 2.4: Digital outphasing.

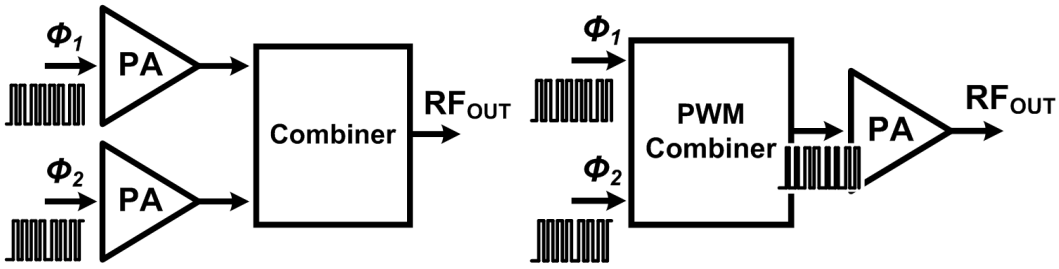


Figure 2.5: Outphasing-based architectures. (a) Direct digital outphasing PA. (b) Digital outphasing scheme in RF-PWM PA.

[13, 14, 15, 16]. Additionally, two PAs are required to generate a single RF output. However, if the digital outphasing scheme is used in the RF-PWM transmitter, the combiner can be easily implemented using simple digital logic, and a single PA can generate a single output as shown in Fig. 2.5b [1], [3].

Fig. 2.6 shows the application of digital outphasing for generating RF-PWM in the time domain. Two 50% duty-cycle pulses with different phases are used to adjust the duty-cycle and the phase of the output, to modulate the amplitude and the phase of the carrier, respectively. Amplitude information

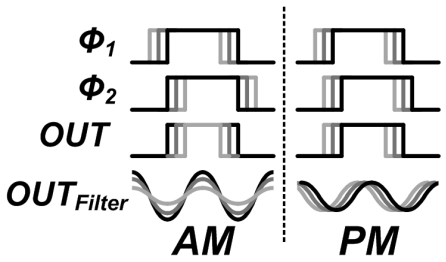


Figure 2.6: Generation of RF-PWM using digital outphasing.

is related to the difference between the pulse edges, that corresponds to the duty-cycle. Phase modulation is achieved by moving the pulse edges in the same direction.

The complete architecture of the implemented transmitter is shown in Fig. 2.7. The transmitter consists of the phase modulator with a glitch-free phase selector, a digital RF-PWM combiner and a class-D PA. In the approach, two outphased phase-modulated signals are generated in response to the input signal, using a delay-locked loop (DLL) and a phase interpolator. The RF-PWM combiner based on digital logic subsequently combines the two outphased signals and generates the RF-PWM signal. The conversion between full-carrier switching and half-carrier switching modes is implemented in this part of the transmitter, by using a pulse arbitrator. A class-D PA is then employed at the output to drive the RF-PWM signal.

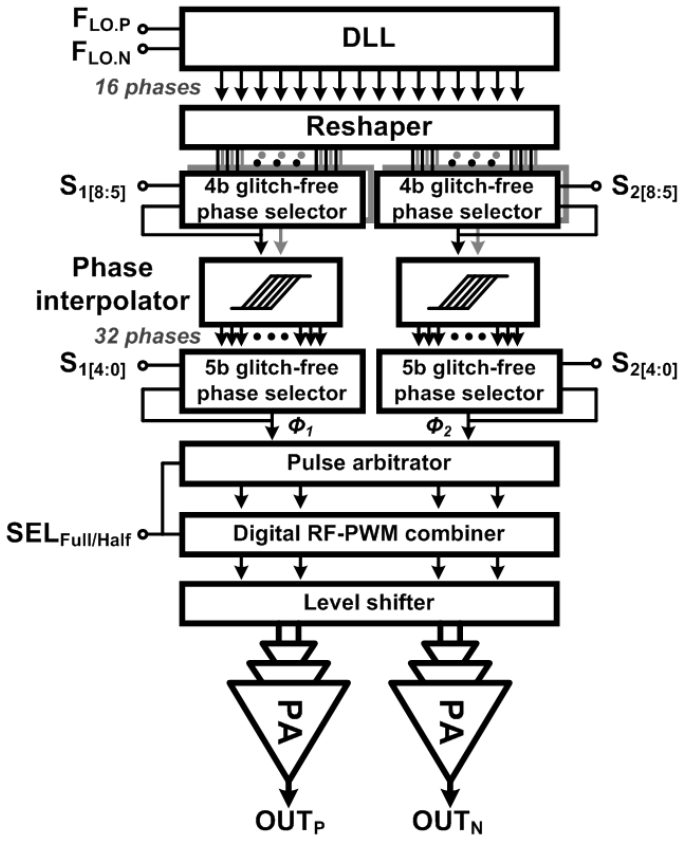


Figure 2.7: Complete transmitter architecture.

2.4 Circuit Implementation

2.4.1 Phase Modulator

In order to generate precise phase steps, a DLL with a phase interpolator is employed. Fig. 2.8 shows the circuit diagram and the timing diagram of phase modulator. The reference clock at LO frequency f_{LO} is applied to the DLL which provides distinct phases with 4 bits of precision. The voltage controlled delay cells (VCDL) employed in the DLL are carefully sized and laid-out to minimize phase offsets. Signals with 16 phases are generated by the DLL, which is followed by a pulse reshaper. The pulse reshaper, which is a simple buffer, is used to restore the pulse edges from the DLL output. Two paths are used after the DLL to generate two outphased signals. Each path chooses two neighboring phase signals of the target phase value from the DLL output, using a glitch-free phase selector. Fine phase generation is performed using the phase interpolator, which provides fine phase information between the two selected phase signals.

The phase interpolator is implemented by using an inverter chain. It receives two adjacent phase signals from the DLL output, $\Phi_{\mathrm{IN}}[\mathrm{n}]$ and $\Phi_{\mathrm{IN}}[\mathrm{n+1}]$, and is designed for a resolution of up to 5 output bits by using 5 cascaded stages. Each interpolator unit cell generates two outputs where one output is a simple delayed version of the first input $\mathrm{A_{IN}}$ and the second output is an interpolated signal derived from two inputs $\mathrm{A_{IN}}$ and $\mathrm{B_{IN}}$ (Fig. 2.8b). Asymmetric inverters are used in each interpolator unit to provide precise phase information. The loading on all interpolator units is made equal by employing

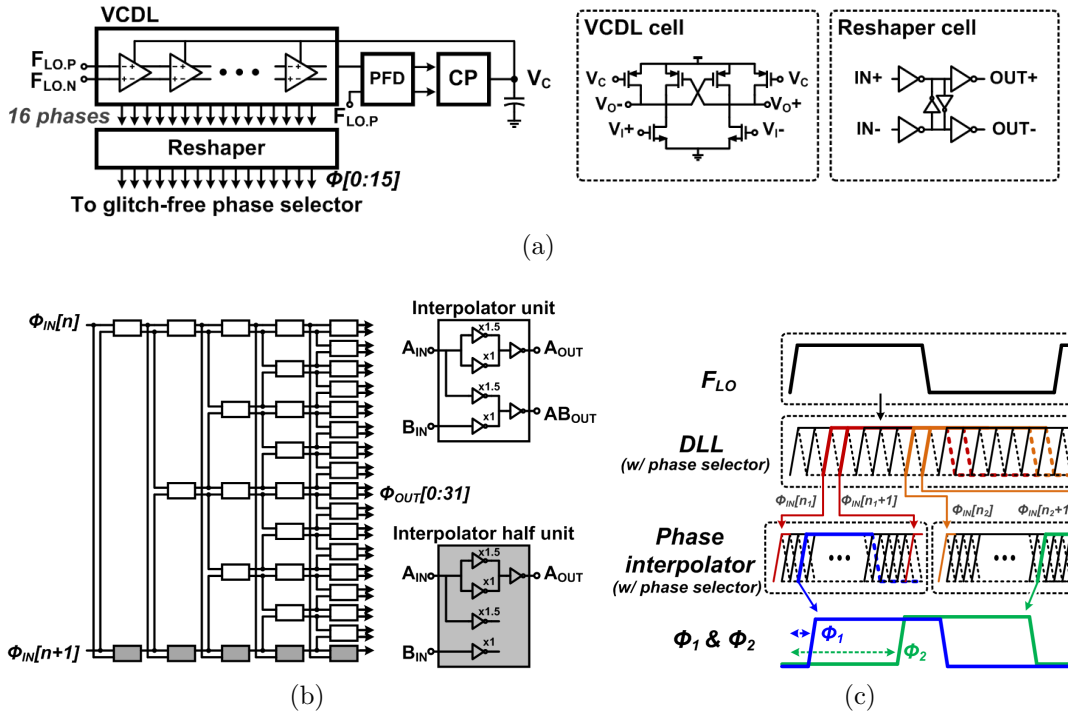


Figure 2.8: Phase modulator. (a) DLL and Reshaper. (b) Phase interpolator. (c) Timing diagram.

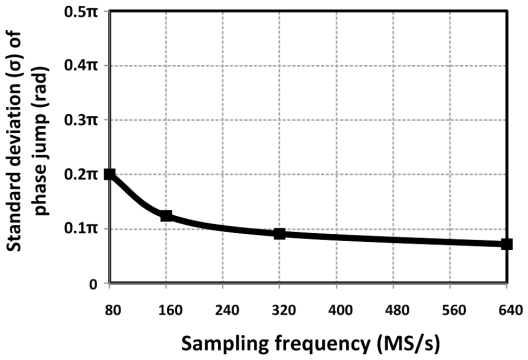
interpolator half-units, which equalizes the delay [20].

In practice, the monotonicity of the interpolator was found to degrade at carrier frequencies over 2 GHz[4]. For the 20 MHz WLAN signal, however, the phase modulator required 7-bits of precision, or in excess of 8 levels from the phase interpolator. For this purpose, 10 levels were selected from the phase interpolator, which guaranteed monotonicity. Since this architecture has no phase-jump boundary and can achieve phase unwrapping, wideband operation with 20 MHz WLAN was easily implemented. It should be noted however, that the degradation in the interpolator places a limit on the maximum signal bandwidth. For achieving even greater bandwidth, such as 40 MHz or 80 MHz wide signal, higher resolution is required in the phase modulator.

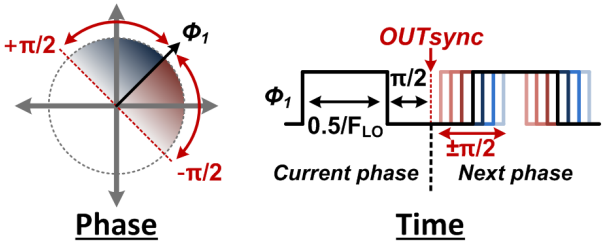
2.4.2 Glitch-Free Phase Selector

As shown in Fig. 2.7, two pairs of glitch-free phase-selectors are employed in the architecture, one pair after the DLLs and the other after the phase-interpolators. The phase selectors are essentially multiplexers (MUX), that pick one out of 2^n clocks of period F_{LO}, with respective phases of $\Phi[0] : \Phi[2^n - 1]$, as indicated in Fig. 2.10a. The MUX control is provided by n-bits that represent part of the digital input signal, S_1 and S_2, as shown in Fig. 2.7.

[4]A calibration unit could potentially be employed for this purpose, but was not included in the design. Alternatively, a faster technology node can be employed to improve high-frequency performance.

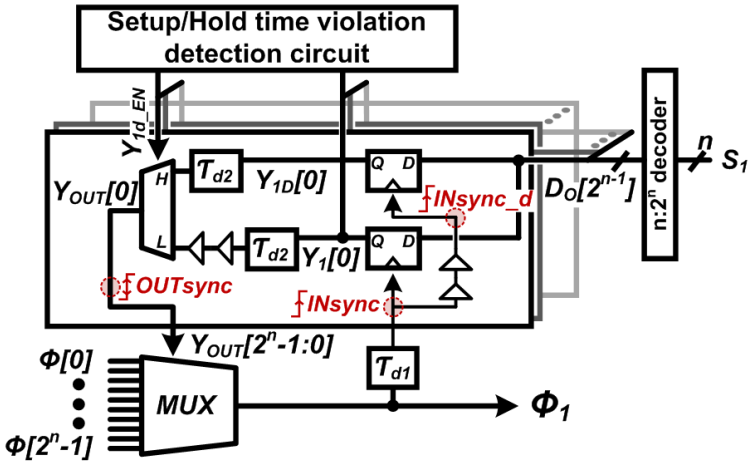


(a)

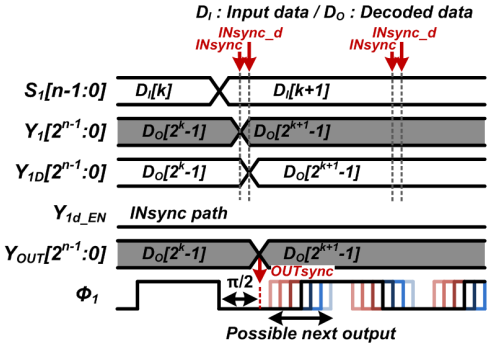


(b)

Figure 2.9: Phase transtions in outphasing system. (a) Standard deviation of instantaneous phase jump at different sampling frequency with 20-MHz 64-QAM 802.11g module signal. (b) Possible next output after OUTsync.



(a)



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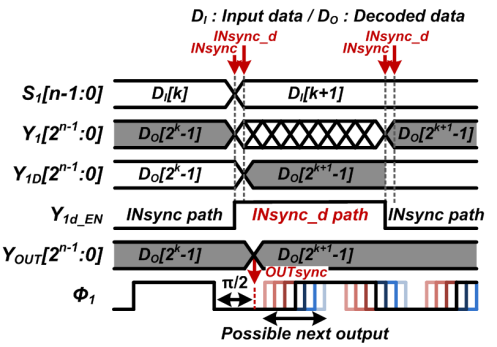


(c)

Figure 2.10: Proposed glitch-free phase selector. (a) Circuit diagram. (b) Timing diagram in normal operation. (c) Timing diagram when the violation detected.

It is critical that the desired phase output be chosen with appropriate timing, in order to avoid glitches due to instantaneous phase jumps. These glitches are usually unpredictable and can increase the spectral noise floor. This problem becomes more severe at higher signal bandwidths.

Since the DLL operates at the LO frequency, the sampling frequency can be made as high as the LO frequency, which significantly limits the magnitude of the instantaneous phase-jumps. Fig. 2.9a shows the standard deviation of instantaneous phase jumps with different sampling frequencies for a 20-MHz 64-QAM 802.11g modulated signal, including the carrier switching concept. When the sampling frequency is larger than 100 MS/s, 99.7% (3σ) of phase jumps are seen to be limited to $\pm\pi/2$. The phase-selector architecture (Fig. 2.10) is designed to provide glitch-free operation for a phase-jump up to $\pm\pi/2$. For this purpose, the output conversion point (OUTsync) is located at $\pi/2$ from the falling edge of the output of Φ_1, which is achieved by using an appropriate delay of τ_{d1}, after the falling edge is sensed. For any given selection, the phase Φ_1 stays high for a duration of $1/(2F_{LO})$. For a subsequent phase step in the range $\pm\pi/2$, the next rising edge of the phase signal can go high after a time of $1/(4F_{LO})$ to $3/(4F_{LO})$ from the current falling edge (Fig. 2.9b).

A potentially severe problem can arise from setup and hold-time violation of the D flip-flops (D-FF) used to sense the falling edge of the output. This can lead to an unknown output when the synchronization signal (INsync) is detected at the transition point of the bit selection signals S_1 and S_2 (Fig.

2.7). To address this issue, a duplicate synchronization circuit with a delayed synchronization signal (INsync_d) is employed in the phase selector. The bit selection signals are detected by both INsync and INsync_d. In normal operation, the original path that is synchronized by INsync is used. When a violation is detected in the INsync path, the delayed synchronization path is chosen which does not suffer from the violation. Once the violation has been removed in the original path, the INsync path is selected again. Delays τ_{d2} are added to signal paths Y_1 and Y_{1D} in order to provide adequate time for the violation detection circuit to make a decision regarding which paths needs to be chosen. OUTsync can be controlled by adjusting τ_{d1} and τ_{d2}.

The setup/hold time violation detection circuit indicates a violation, if the number of high bits among the synchronized input bits ($Y[2^n - 1 : 0]$) is different from 1. If a violation has occurred, the selected bits will show multiple high bits or no high bits. Although the violation detection circuit cannot detect an error when a single wrong high bit is present, the probability of this case is extremely low. Moreover, if such a case were to occur, the correct output will be selected again after one clock cycle.

2.4.3 Digital Combiner for Generating RF-PWM with Carrier-Switching

Fig. 2.11a and Fig. 2.11b show the architecture of the digital combiner for generating RF-PWM with carrier switching, and its timing diagram, respectively. The conversion between the full-carrier switching mode and half-

carrier switching mode is implemented using a pulse arbitrator. The pulse arbitrator receives the two outphased phase-modulated signals from the phase modulator. In the full-carrier switching mode, the pulse arbitrator works as a buffer. In the half-carrier switching mode, the pulse arbitrator distributes the switching pulses into two paths and generates an output at $f_{LO}/2$. In the full-carrier mode, AND and NAND logic is employed using the outphased signals Φ_1 and Φ_2 to remove even harmonics at the differential output. In the half-carrier mode, OR and NOR logic is utilized with the distributed phase signals (Φ_{H11},Φ_{H12},Φ_{H21},Φ_{H22}), that are generated by the pulse arbitrator, to remove the fundamental at $f_{LO}/2$ and odd-harmonics of this frequency in the differential output, regardless of LO frequency. The primary spectral content at the output in either mode is thus localized around f_{LO}. Consequently, the bandpass filtering requirement is significantly reduced.

A delay mismatch between OUT_P and OUT_N can lead to spectral noise around $f_{LO}/2$ and $3f_{LO}/2$. However this mismatch is expected to be very small because both outputs receive signals from Φ_1 and Φ_2 identically. Fig. 2.11c shows the simulated results of relative harmonic power at $f_{LO}/2$ and $3f_{LO}/2$ with different delay mismatches with the output filter employed in the current design. The relative power is given by the difference between the harmonic tone and the maximum output power. The output power starts from -6 dB due to half-carrier mode operation. The harmonic at $3f_{LO}/2$ shows a deep null around -7.2 dB back-off because the 3^{rd} harmonic component is 0 for a duty-cycle of 33.3%. The harmonics are seen to decrease as the mismatch becomes

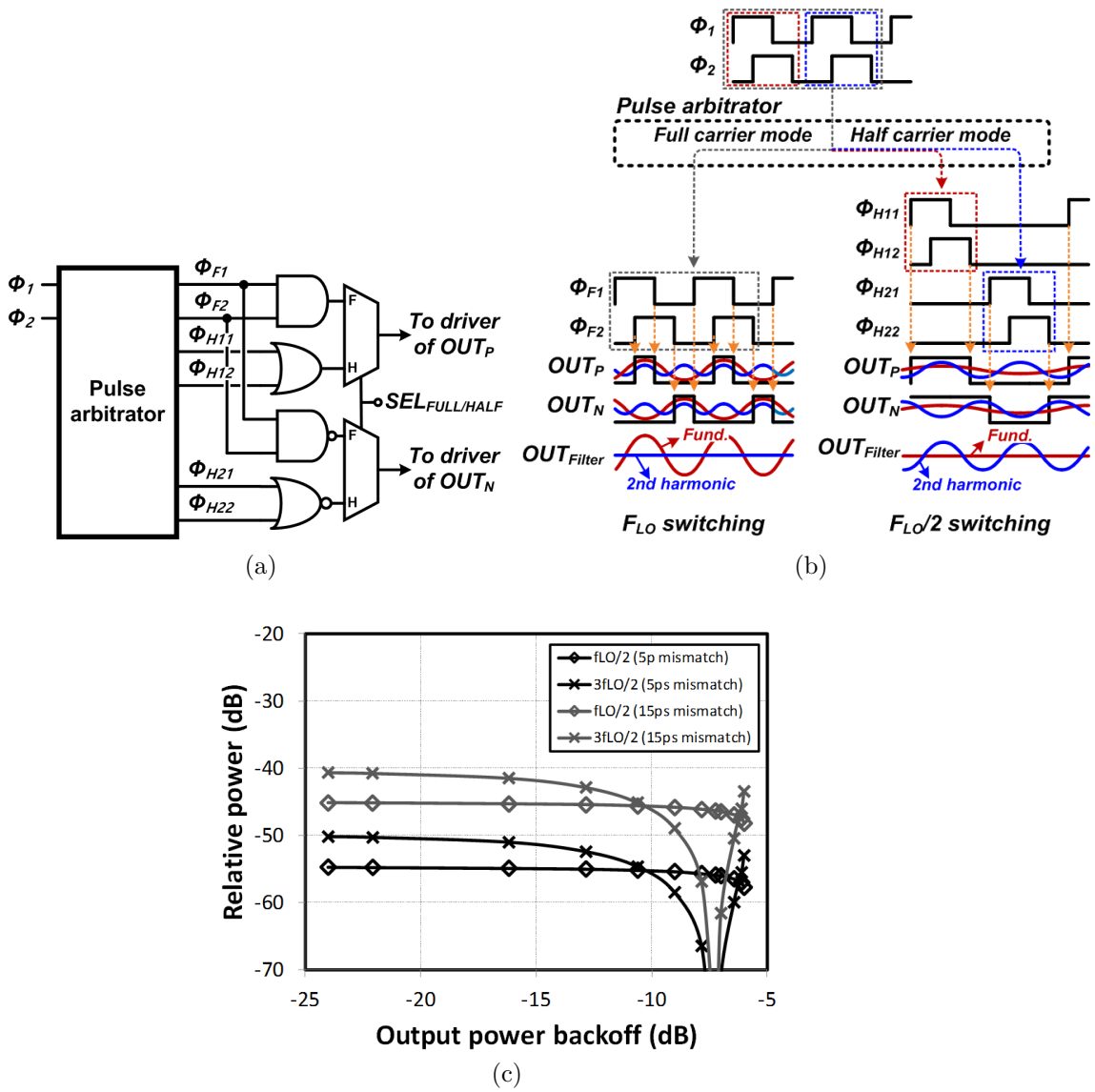


Figure 2.11: Digital combiner for generating RF-PWM with carrier-switching (a) Block diagram. (b) Timing diagram. (c) Simulated relative fundamental and 3rd harmonic power in half-carrier switching mode with delay mismatch.

smaller.

2.4.4 Power Amplifier and Driver

A class-D PA is found to be the most suitable PA design for carrier switching, compared to class-E or class-F PAs, because the class-D topology maintains high efficiency regardless of input frequency transition, duty-cycle variation or phase modulation. Fig. 2.12 shows the driver stage and class-D PA design. A critical consideration in class-D stages is the potential for shoot-through currents, which can occur during switching transitions, when both PMOS and NMOS transistors in the class-D stage turn on simultaneously. Shoot-through currents increase DC power dissipation, and degrade the efficiency of the design. To avoid these currents, the PMOS and NMOS device sizes in the two drivers preceding the class-D output stage (I1, I2, I3 and I4) are made asymmetric. This ensures that the NMOS and PMOS stages receive the transition signals with a small relative time-delay, which is sufficient to suppress shoot-through currents. The NMOS and PMOS stages are turned off rapidly and turned on relatively slowly, by employing gate signals with different slopes in the output stage (N_{IN} and P_{IN} in Fig. 2.12). The simulated non-overlap time is 30 ps, based on 50% of rising/falling transition point. The PMOS/NMOS size ratio for other drivers is set to 2/1. A large fan-out of 4 is employed in order to enhance efficiency. This is possible here, since the transmitter does not need to drive narrow-pulses at the carrier frequency, and hence is less sensitive to load capacitance. A cascode Class-D PA is employed

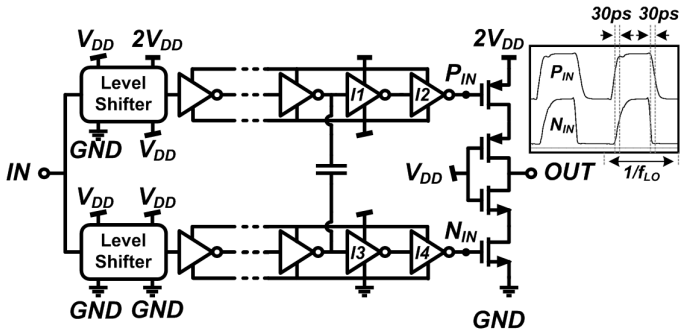


Figure 2.12: Driver stage and class-D PA.

to support high output voltage.

2.5 Measurement Results

The design has been implemented in a 130-nm CMOS process. The die-photograph of the chip is shown in Fig. 2.13. The total die area is 1.5 mm x 1.5 mm. The core area including the phase modulator, drivers, and class-D PAs is 0.46 mm^2. The phase modulator circuits and class-D PA use supply voltages of 1.4-V and 2.8-V respectively. An external impedance matching network filter and a transformer-based combiner are used. The losses of the matching network filter have been deembedded. The two outphased digital baseband signals are generated using an FPGA, which provides arcsin-predistorted amplitude and phase signals. These signals are fed directly from the FPGA to the IC at 160 MS/s using single-ended stub series terminated logic (SSTL).

Fig. 2.14 shows the measured linearity of the phase modulator. The phase information is obtained by capturing the output waveform in response

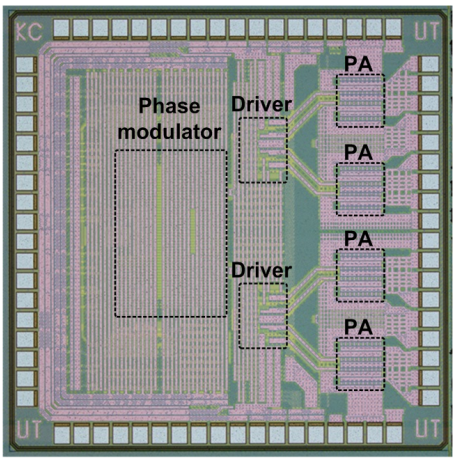
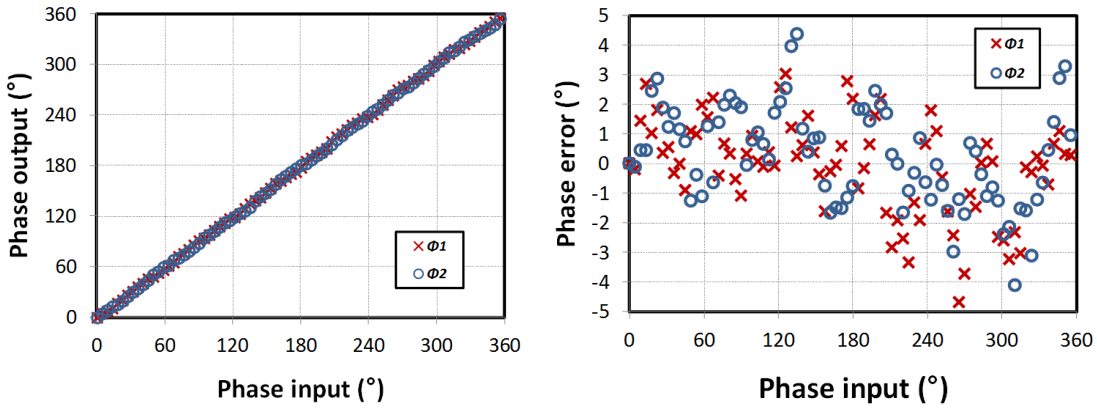


Figure 2.13: Chip photograph.

to modulated amplitude and phase inputs. Although the effective resolution of the phase modulator is reduced in the phase interpolator at the carrier frequency owing to speed limitation of the process, it is found to be sufficient to drive the 20 MHz WLAN signal.

Fig. 2.15 shows the measured peak output power and PAE at different LO frequencies. The -3 dB bandwidth from the peak output power is around 500 MHz and is determined by the matching network. Fig. 2.16 shows the output power versus the duty-cycle at an operating frequency of 2.1 GHz. The peak output power levels are 25.6 dBm and 20.2 dBm at full-carrier frequency operation and half-carrier frequency operation, respectively. The minimum measurable output power at full-carrier frequency operation is 17 dBm. The conversion point between the full-carrier switching and the half-carrier switching slightly moves to a higher duty-cycle instead of the theoretical value of 16.7% because of finite transition time. The finite transition time reduces the



(a) (b)

Figure 2.14: Measured phase modulator linearity. (a) Transfer function. (b) Phase error.

output power significantly at the low power range of the full-carrier switching mode. It is observed that a duty-cycle under 20% cannot be measured accurately. The duty-cycle here is calculated based on phase information from the DLL and the phase interpolator.

Fig. 2.17 shows the power-added efficiency (PAE) versus output power. The PAE includes the power of all drivers and PAs after the phase modulator. In full-carrier operation, the peak PAE is 34% at the maximum output power of 25.6 dBm. The low output power range can be covered by the half-carrier mode. The peak efficiency in the half-carrier mode is 23% at 25% duty-cycle. PAE is enhanced by up to 9% in the half-carrier mode compared to the full-carrier mode for the same output power level since the switching loss at output drivers and PAs is halved. The dynamic range of the architecture is 23 dB. The ideal minimum output power is zero in the half-carrier switching mode. The

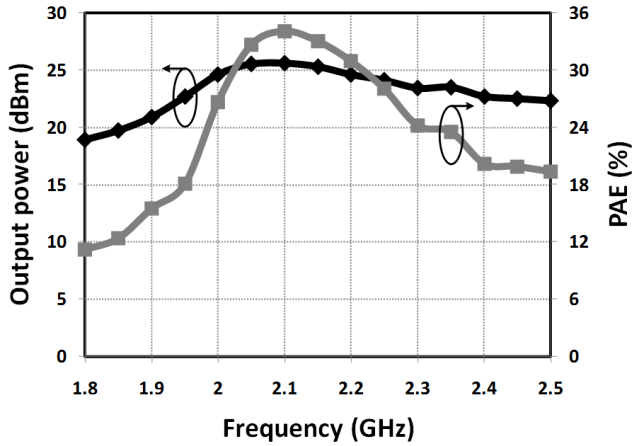


Figure 2.15: Measured peak output power and PAE at different LO frequencies.

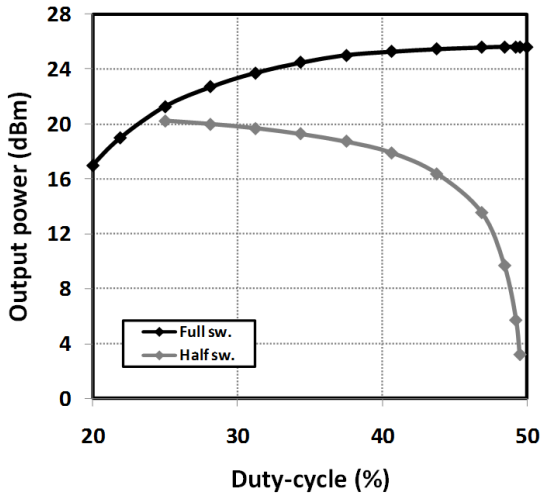


Figure 2.16: Measured output power versus duty-cycle.

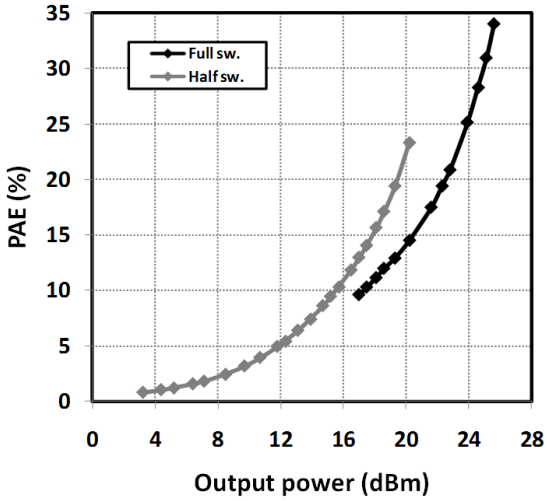


Figure 2.17: Measured PAE versus output power.

minimum output power is however greater than zero, because the duty-cycles of OUT_P and OUT_N are not exactly 50% in the practical implementation.

Fig. 2.18 shows the measured AM-AM and AM-PM characteristics. From maximum input amplitude to half of the maximum amplitude, the design is operated in the full-carrier switching mode, while for the rest of the amplitude range it is operated in the half-carrier switching mode. The AM-PM distortion abruptly changes at the transition point of the switching mode due to the reconfiguration of the digital outphasing circuit.

The transmitter has been tested with 20-MHz 54-Mb/s 64-QAM 802.11g packet WLAN signal and the sampling frequency is set to 160 MS/s. Fig. 2.19 shows the measured spectrum and EVM with average power of 18.3 dBm (7.3 dB PAPR). The PAE is 16% for an EVM of -25.5dB. The noise floor of the spectrum is determined by the non-linearity of the phase modula-

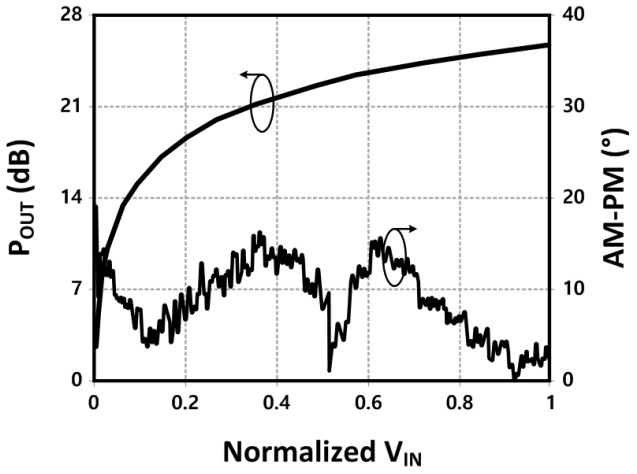


Figure 2.18: Measured AM-AM and AM-PM characteristics.

tor, especially the phase interpolator, and can be enhanced by calibrating the interpolator linearity. The total power consumption in the phase modulator including the DLL, phase interpolator, bias circuit and glitch-free phase selector is 98 mW, and the overall system efficiency is 13% for this WLAN signal.

The measured far-out-of-band spectrum is shown in Fig. 2.20. The aliased spectrum arises from the sampling of the amplitude signal with 160 MS/s ratio. Higher sampling rates can reduce the spectral aliasing significantly [21]. Due to the design of the outphasing circuit, no significant power is observed at the even harmonics of the carrier frequency, or at odd harmonics of the half-carrier frequency. A relatively high harmonic is observed at 4.2 GHz which arises from the 4^{th} harmonic of the half-carrier frequency. However, as can be observed, this level is still low.

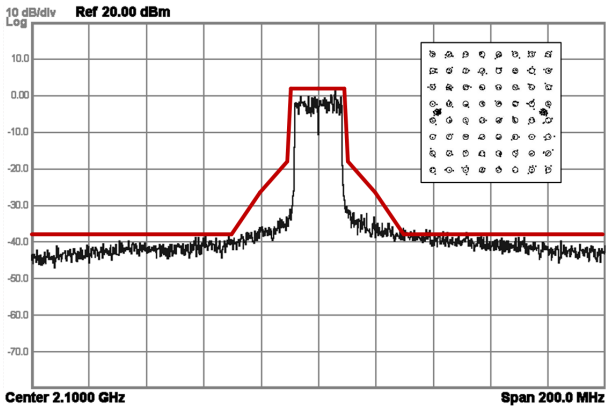


Figure 2.19: Measured spectrum and EVM with 20-MHz 64QAM 802.11g modulated signal.

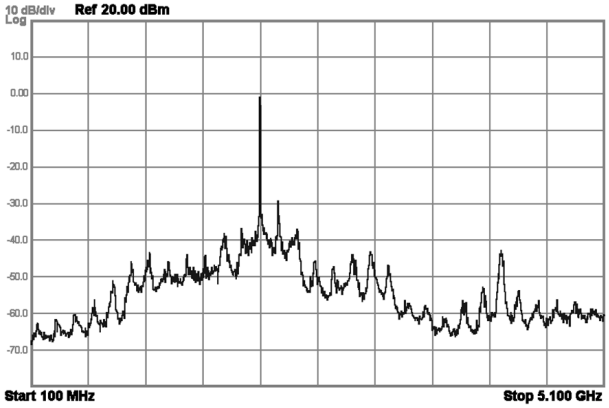


Figure 2.20: Measured far-out spectrum.

Table 2.2 summarizes the performance and provides a comparison with prior work. Although the design has been implemented in 130-nm process, the performance is comparable to the prior work that is implemented in relatively advanced processes.

2.6 Conclusion

A digitally-intensive transmitter/PA using RF-PWM with carrier switching is proposed. The carrier-switching concept overcomes the dynamic range limitation of PWM at RF that can be observed in classical RF-PWM by utilizing carrier-switching between full-carrier and half of full-carrier frequencies. This allows the transmitter to drive modulated signals with large PAPR. Efficiency is also improved in the power back-off region due to reduced switching losses in the half-carrier mode. In addition, a glitch-free phase selector is demonstrated that not only removes the deleterious glitches at the input data transitions but also prevents D-FF setup-and-hold time violations. The proposed transmitter is demonstrated using a 20-MHz 64-QAM 802.11g modulated signal. Owing to the digitally-intensive approach, the design can further benefit in performance and area through the use of more advanced technologies.

Ref.	**Archi -tecture**	**Process (nm)**	**Peak power (dBm)**	**Peak η (%)**	**Modu -lation**	**Avg. power (dBm)**	**Avg. η (%)**	**PAPR (dB)**	**Matching network / Balun**
[8]	Digital Polar	180	N/A	N/A	64-QAM OFDM	13.6	6.7†	N/A	Off-chip
[9]	Digital Polar	65	21.8	44*		14	18*	7.8	On-chip
[13]	Digital Outphas-ing	32	26	N/A		20	22†	6	Off-chip
[14]	Digital Outphas-ing	32	25.3	35†		19.6	21.8†	5.7	On-chip MN / Off-chip balun
[15]	Digital Outphas-ing	45	31.5	27†		24.8	16†	6.7	On-chip
[22]	Quadrature	45	24.7	37*		18.8	17*	5.9	On-chip
[1]	RF-PWM	65	28.6	28.5†	$\pi/4$ DQPSK	26.7	21†	1.9	On-chip MN / Off-chip balun
This work	RF-PWM	130	25.6	34†	64-QAM OFDM	18.3	16†	7.3	Off-chip
*: Drain efficiency, †: Power Added Efficiency									

Table 2.2: Performance summary.

Chapter 3

A High Speed PWM Driver using Multi-Level Class-D Architecture[1]

3.1 Introduction

An amplifier that employs a PLL-based multi-level PWM generator, with duty-cycle folding is described in this chapter [4]. PWM is generated by comparing the local average of the output of a phase-detector in a PLL to an externally applied analog signal. Through signal comparison in the phase-domain, instead of the amplitude domain the architecture allows for high-speed PWM generation.

3.1.1 System Requirements

While the architecture described here can find use in multiple applications where AC-signal amplification is required, the reported implementation is well-suited for power-line communications (PLC) applications. PLC is an integral part of the smart-grid concept [23, 24], that employs existing power lines

[1]This chapter is based on reference [4] (K. Cho and R. Gharpurey, "A 40-170 MHz PLL-based PWM driver using 2-/3-/5-Level class-D PA in 130 nm CMOS," IEEE J. Solid-State Circuits, vol. 51, pp. 2639-2650, Nov. 2016, ©2016 IEEE). Kunhee Cho was responsible for the design, implementation and measurement of the high-speed driver IC described in this publication.

for bi-directional communications [25]. The design described here addresses applications with bandwidth up to 500 kHz, [26, 27, 28], and is aligned with spectrum plans defined by CENELEC, FCC, and ARIB. Differential modulation schemes such as DBPSK, DQPSK, and D8PSK have to be supported with OFDM, for robust communication over power lines.

In systems such as PLC, the design of the AFE driver should take into consideration the following aspects: (a) good efficiency at peak power and at back-off, to support the use of modulations with high peak-to-average power ratio, (b) excellent distortion performance, with THD better than 60 dB at peak power, in order to satisfy electromagnetic compatibility, (c) low-distortion in the presence of a time-varying load, and (d) bandwidth up to 500 kHz.

3.1.2 Multi-level PLL-PWM with Class-D Output Stage

In the reported design, high efficiency in both peak and back-off regions, is achieved through the use of class-D switching output stages. Since a class-D stage is essentially a switch that connects the load to either the supply, or to the ground, the design is inherently highly efficient, and in fact leverages CMOS technology. By contrast, linear class-A and class-B stages, suffer from a significant decline in efficiency at lower power levels, in addition to significantly lower peak efficiency levels, as noted in prior chapters. Excellent distortion performance is achieved in the PLL-PWM generator, since it is based on the use of negative feedback. The use of a feedback-based system also reduces

the output impedance of the driver within the signal bandwidth, making it immune to noise and transients caused by switching of loads on the power lines. Finally, the use of PLL-based PWM generation makes it possible to replace a linear, high-frequency ramp with a reference switching clock, which allows for high-frequency operation. A switching frequency in the range from several 10s of MHz to 170 MHz is demonstrated. This aspect simplifies the design of the external low-pass filter that is placed between the driver and the power-line for spurious noise reduction.

The PLL-PWM system here is designed for wider bandwidth than the design of [29]. In addition, the work demonstrates the use of multi-level (2/3/5-level) PWM. In 3- and 5-level PWM operation, the output voltage range is divided into multiple sub-ranges. This reduces the switching voltage levels, which helps to enhance efficiency. A key design described here is a 3-level PLL-PWM driver, that uses a single voltage supply source. A novel aspect of this approach is that it has virtually no hardware overhead compared to a 2-level design and hence is an effective and low-cost approach for enhancing the efficiency. The 5-level driver enhances efficiency even further, although it requires an additional supply source/sink path compared to the 2-level and 3-level designs[2].

A critical potential challenge in switching levels in PWM is an abrupt jump in duty-cycle, as a level boundary is crossed. In a PLL-PWM, or any

[2]This aspect introduces a trade-off between hardware cost and efficiency for the 5-level driver. As such the choice to use 5-level over 3-level involves a system-level optimization.

feedback-based system, this discontinuous step in duty-cycle could cause the loop to loose lock. The second major aspect to the reported work is a technique for folding of PWM across voltage domains, that ensures that switching between levels does not cause abrupt changes in the duty-cycle.

3.1.3 Other Applications of High-Efficiency Switching Amplifiers

The above design can be contrasted with two applications that also use switching amplifiers. State-of-the-art audio amplifiers make extensive use of class-D output stages [30, 31, 32]. Typical audio architectures drive an amplitude modulated signal up to 20 kHz, and are not directly suitable for PLC applications due to limited loop bandwidth as well as low switching frequency. For the high switching-frequency operation that is required here, employing ramp-reference based (or triangular-reference based) PWM generation, that is often used in audio amplifiers, is extremely challenging due to requirements for a high-quality carrier generator and a high-speed voltage comparator [30, 31]. DC-to-DC conversion is another application where switching amplifiers are frequently used. Several high speed DC-to-DC converters have been proposed for reducing the output filter complexity and for achieving fast dynamic response with high peak efficiency [33, 34, 35]. However it is difficult to maintain high efficiency over a wide range of output signal level, as well as the load impedance. Furthermore, conventional DC-to-DC converters cannot be directly used for driving AC-signals, because these are not optimized for achieving high-linearity and wide-bandwidth simultaneously.

A technique for enhancing efficiency that is based on the use of multiple supplies is class-G amplification. Class-G operation is shown for audio amplification in [36]. A key difference between class-G and the multi-level PWM is that while class-G operation primarily targets efficiency enhancement at low-power levels through the use of multiple supplies, multi-level PWM reduces the losses at high power level as well as low output power level, since the fCV^2 losses are smaller in either case due to smaller switching levels. A DC-to-DC converter with 3-level output that merges the characteristics of a buck converter and a switched-capacitor converter is reported in [37]. By employing 3-level operation, wide range of output voltage is achieved with relaxed output filtering requirement. This design approach can be suitable for on-chip DC-to-DC conversion, however, it cannot be used for driving AC-signals due to non-linearity.

This chapter is organized as follows. Section 3.2 introduces the high switching frequency PWM driver. Section 3.3 provides a complete architecture with proposed multi-level operation. Section 3.4 describes measured results and the conclusion follows in Section 3.5.

3.2 PWM Generation

The spectrum of a PWM signal consists of a baseband component and intermodulation products located at harmonics of the switching frequency. For example, the two-level PWM output $y(t)$ for an input $x(t) = M\cos(\omega_{in}t)$ and

a switching frequency of ω_c can be shown to be given by [38]

$$\begin{aligned} y(t) &= M\cos(\omega_{in}t) + 2\sum_{m=1}^{\infty}\frac{1 - J_0(m\pi M)\cos(m\pi)}{m\pi}\sin(m\omega_c t) \\ &\quad -2\sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\infty}\frac{J_n(m\pi M)}{m\pi}\sin(m\omega_c t + n\omega_{in}t + m\pi - \frac{n\pi}{2}) \end{aligned} \quad (3.1)$$

where m is index of the harmonics of the carrier signal, n is index of the harmonics of the input signal and J_n is the n^{th}-order Bessel function. The output consists of the fundamental input frequency, the aliased spectrum localized around $m\omega_c$ and an infinite number of intermodulation products. In the time-domain, this output consists of rectangular pulses switching between two fixed levels. The desired output is derived by applying a low-pass filter to the PWM signal, to extract the first term in the spectrum of Eq. 3.1. In order to reduce the complexity of the low-pass filter, it is important to ensure that $\omega_c \gg \omega_{in}$.

Techniques for generation of PWM signals are described below.

3.2.1 Ramp-based PWM Architecture

Conventional PWM drivers typically utilize a ramp or a triangular-waveform signal as a reference, as shown in Fig. 3.1. In a ramp-based PWM architecture, the output signal of the power stage is fed back into a low-pass loop filter, and linearly subtracted from the input signal. The output of the loop filter is the compensated signal, V_{COMP}. The PWM signal (V_{PWM}) is generated by comparing the value of V_{COMP} with the ramp signal (V_{RAMP}). Consequently, the linearity of the ramp-based PWM architecture is highly

dependent on the ramp signal and the comparator performance.

For wider bandwidth applications, such as power-line communication, which requires a bandwidth of up to 500 kHz, high switching frequency operation is required. It is challenging in this case to achieve high linearity through the use of a ramp-based PWM generator, since the required ramp signal frequency can be in the range of several tens to hundreds of MHz. The requirement for high ramp frequencies arises from the need to ensure sufficient accuracy in PWM generation and for ensuring that the out-of-band spurs corresponding to the reference frequency are sufficiently far from the bandwidth corner of the desired signal (Eq. 3.1).

Generation of a precise ramp signal at this frequency can imply high power consumption, as it is a broadband signal. Furthermore, the comparator has to make instantaneous decisions based on input signals that can differ by small values, in the range of sub-mV, where the architecture is vulnerable to noise and spurs, as noted in [29]. Finite comparator gain-bandwidth product can cause distortion as well. The bandwidth limitation at the input of the comparator or within the comparator itself, can cause the ramp to deviate from its linear dependence on time. These design issues become progressively more challenging as the switching frequency is increased.

3.2.2 PLL-based PWM Architecture

In this work, a PWM architecture based on a PLL (Fig. 3.1b) is employed to allow for high switching frequency operation [29]. The PLL-based

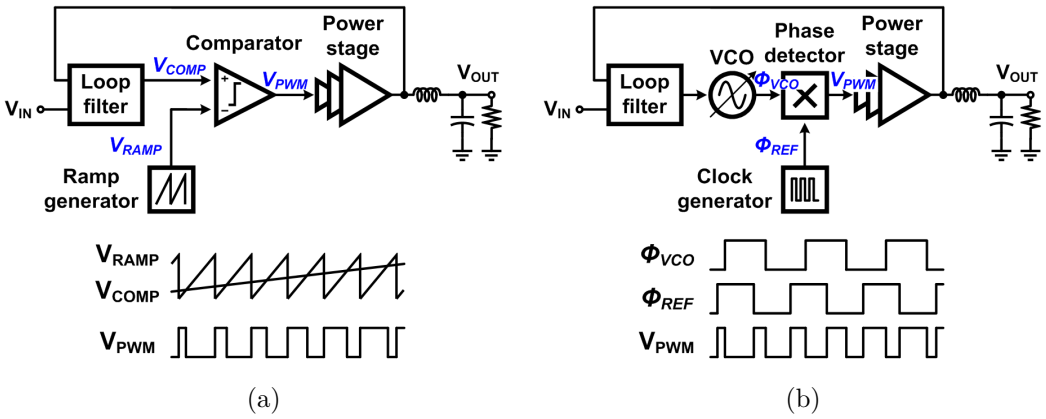


Figure 3.1: PWM generation. (a) Ramp-based architecture (b) PLL-based architecture.

approach generates PWM output by converting the difference between the input signal and the output signal into the phase of a VCO (Φ_{VCO}), and comparing the VCO phase to that of a reference clock (Φ_{REF}). A phase detector (PD) is used to provide an output that is proportional to the difference of these phases, which is used to drive the class-D output stage. The class-D output is fed back and subtracted from the input, and then applied to a low-pass loop filter. The output of the loop-filter drives the VCO control line.

When the loop is locked, the average of the VCO control line is ideally zero which implies that the difference of the inputs of the analog low-pass filter, within the bandwidth of the filter also has to have a zero average. This can be obtained only if the low-frequency content of the output stage is identical to the input signal with inverted phase. This ensures that the output of the power stage has to be PWM.

Compared to a ramp-based PWM generator, the PLL-based PWM approach eliminates the requirements for a high-speed linear ramp signal or fast voltage comparators. Implementing a precise ramp signal and high-speed comparators at frequencies as high as hundreds of MHz while meeting THD in excess of 60 dB is extremely challenging, as noted above. Moreover, the PLL-based PWM architecture can benefit from process scaling since the PWM output is generated by using a phase detector, that is essentially digital logic, and a reference clock whose shape is not critical. The speed, accuracy and power dissipation of the phase detector, and the reference clock generator improve with process scaling.

3.2.2.1 Stability

To analyze the stability of the loop, a linear model is used as shown in Fig. 3.2. An op-amp based third-order loop filter is employed to enhance the loop response. The transfer function of the loop filter is given by $T_{Filter}(s)$ and the frequency response of the operational amplifier is given by $A_{OP}(s)$. The VCO is represented by its voltage-to-phase transfer function $2\pi K_{VCO}/s$ and is modeled as an ideal integrator. Assuming that the phase detector switches between -1 and 1, the gain of the phase detector (G_{PD}) is given by $2/\pi$. The gain of the power amplifier is given by G_{PA}, which equals the ratio of the maximum PA supply to the supply of the core [29]. The attenuation of the resistive divider following the power stage is given by α. Thus, the loop gain, $A_{Loop}(s)$, can be represented by,

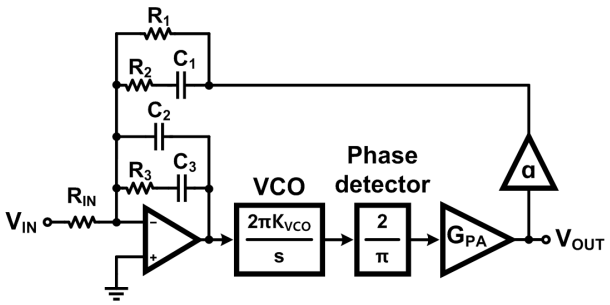


Figure 3.2: Linear model of PLL-based PWM generator.

$$A_{Loop}(s) = T_{Filter}(s) \cdot \frac{2\pi K_{VCO}}{s} G_{PD} G_{PA} \alpha = \frac{4\alpha \cdot A_{OP}(s) K_{VCO} G_{PA}}{s \cdot \left[1 + \frac{Z_{F1}}{R_{IN}} + \frac{Z_{F1}}{Z_{F2}}(1 + A_{OP})\right]} \tag{3.2}$$

where $Z_{F1} = R_1 \parallel (R_2 + 1/sC_2)$ and $Z_{F2} = (1/sC_2) \parallel (R_3 + 1/sC_3)$.

The simulated loop gain and phase response are shown in Fig. 3.3. The unity-gain loop-bandwidth product is 2.3 MHz and the phase margin is 45°. These metrics are sufficient for achieving stable operation with the required bandwidth for the PLC specification. Stability has also been verified by numerically computing the closed-loop poles of the transfer function, for nominal values of loop resistors and capacitors, and K_{VCO}, and with an assumed $\pm 20\%$ variation range. For the full-range of variations, all closed-loop poles are in the left-half plane.

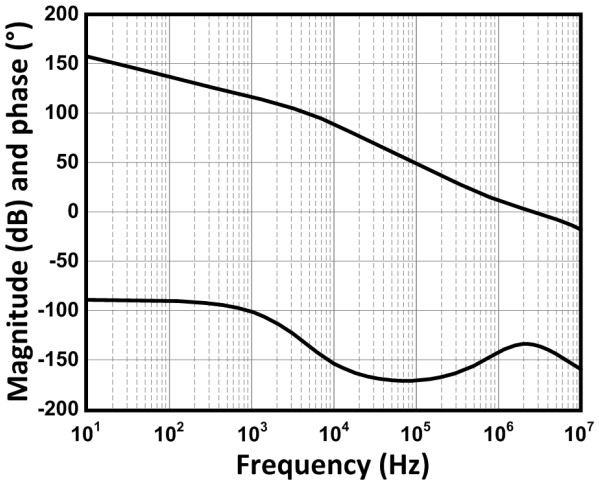


Figure 3.3: Simulated loop gain and phase.

3.2.2.2 Linearity

A key contributor to overall THD performance in the PLL-PWM is the VCO. However, the linearity of the VCO is important only in its range of operating frequency, not over a wide range of VCO operation, such as in a VCO-based ADC, for which linearization approaches such as calibration [39, 40] have been proposed. The range of VCO operating frequency can be limited by design to approximately ±10% of the PLL reference frequency, f_{REF}[3]. By exploiting the small fractional range of operation, sufficiently linear VCO operation can be achieved.

For an input signal with the frequency of f_{IN}, the PWM output contains spurs that are clustered at the harmonics of the switching frequency, f_{SW}, with

[3]In the reported design, based on simulation, the VCO output frequency is observed to vary between 28.5 MHz and 31.5 MHz with f_{REF}= 30 MHz for 2-level PA output operation when maximum input swing is applied.

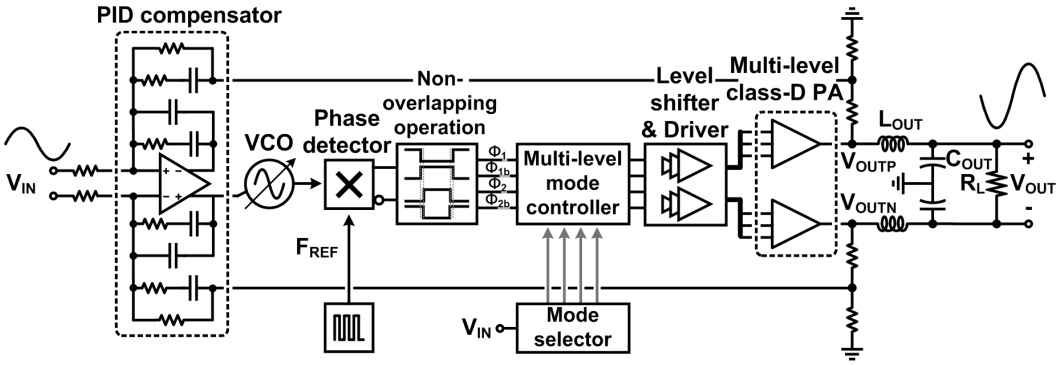


Figure 3.4: Full architecture of PLL-based PWM multi-level class-D driver.

spacing of f_{IN}. These spurs cause intermodulation distortion due to the non-linearity of VCO. For example, spurs at $f_{SW} + nf_{IN}$ and $f_{SW} + (n+2)f_{IN}$ are down-converted to base-band, and appear as a distortion at $2f_{IN}$ due to second harmonic distortion of the VCO [29]. Similarly, spurs at $f_{SW} + 2nf_{IN}$ and $2f_{SW} + nf_{IN}$ can generate third-order intermodulation distortion terms at baseband through the third-order harmonic distortion of the VCO. The even-order non-linearity of the VCO is more important than odd-order non-linearity because the spurs near $2f_{SW}$ can be rejected significantly more than those near f_{SW}, by the analog LPF.

It can also be observed that intermodulation generation can be reduced by increasing f_{SW} relative to f_{IN}, since the loop-filter attenuates f_{SW} more effectively. However, increasing the PLL reference frequency can lead to a decrease in efficiency due to higher fCV^2 switching loss in the class-D output stage. This introduces a trade-off between linearity and efficiency, which can be mitigated by migrating to a faster technology node.

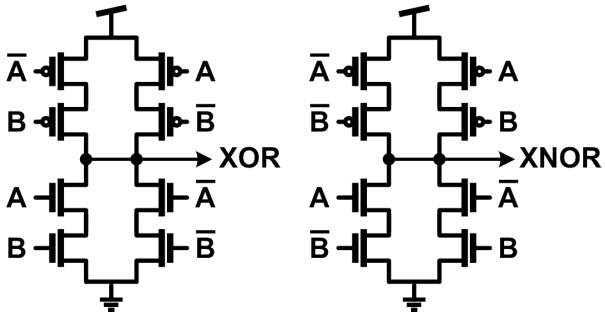
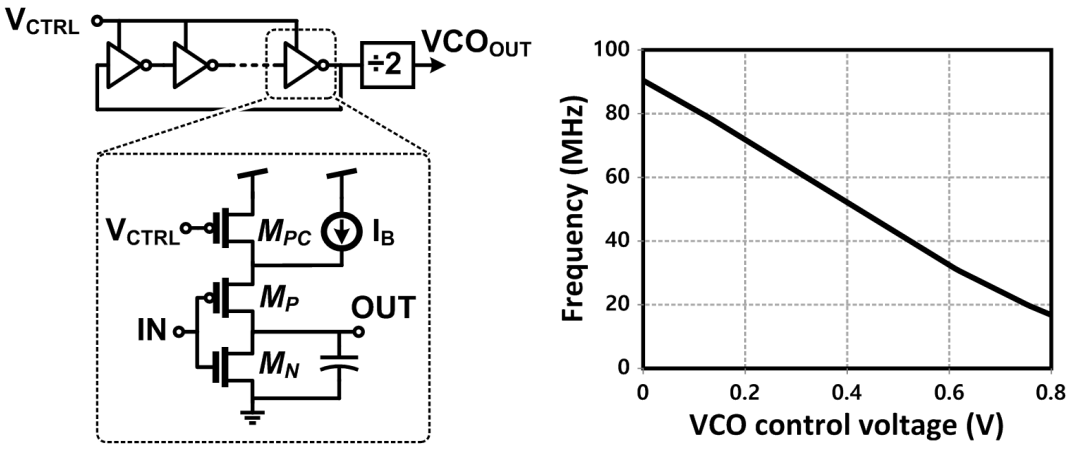


Figure 3.5: Phase detector.

3.3 Complete Architecture with Multi-level Operation

The complete architecture of the implemented PWM driver is shown in Fig. 3.4. A third-order loop filter is employed to enhance the loop response. The phase detector is implemented by static CMOS-based XOR and XNOR circuits as shown in Fig. 3.5. A current-starved inverter with a parallel current source is employed to achieve linear operation as shown in Fig. 3.6. The switching transistors, M_N and M_P are sized at W/L of 20/0.13-µm and 50/0.13-µm, respectively, in order to reduce the effect of the on-resistance of the transistors. By making the gate voltage of M_{PC} the dominant part of the VCO control mechanism, linear operation is achieved, especially within the required frequency range around the operating point which is set by f_{SW}. To enhance efficiency with high switching frequency operation, multi-level output switching is employed using the proposed reconfigurable class-D PA architecture. The PA can be configured to provide 2-level, 3-level and 5-level operation.



(a) (b)

Figure 3.6: (a) VCO structure. (b) VCO response.

3.3.1 Multi-Level Output Operation

The different output operating modes are shown in Fig. 3.7. For 2-level operation, the output switches between ground (V_{SS}) and full power-source (V_{DD4}) with duty-cycle control. For 3-level operation, the output switches from ground (V_{SS}) to mid-supply (V_{DD2}), for half of the input range, and from half to full-supply (V_{DD4}), for the second half of the input range. In 5-level operation, the output voltage range is divided into 5 levels (V_{SS}, V_{DD1}, V_{DD2}, V_{DD3}, and V_{DD4}). The input level is similarly partitioned into five regions. Similar to the 3-level design, the input level determines the switching levels at the output.

Switching loss in PWM is proportional to $fC_{PAR}V_{SW}^2$, where f is the switching frequency, C_{PAR} is the parasitic capacitance of the load and the PA, and V_{SW} is the difference in switching levels. This loss is independent

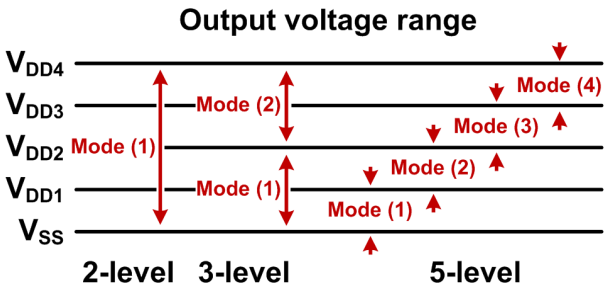


Figure 3.7: Operation range of multi-level PA.

of duty-cycle. In multi-level PWM, V_{SW} is reduced, which helps to enhance efficiency for all input levels, as well as reduce the ripple current so that the output filter can be relaxed. Fig. 3.8 shows the mode selector in the 3/5-level PA. The thresholds for mode selection are located at the normalized input of 0 and $\pm 1/2$ for 3/5-level PA. A comparator circuit is employed to compare the input to the threshold levels. The comparator which is used in the mode selector consumes 50 µA, and has a simulated propagation delay of less than 10 nsec. This delay is adequate for mode-conversions with 40-170 MHz switching frequency. A faster comparator can be employed to further reduce distortion, if required, by increasing the current dissipation. Since the output stage is differential, V_{OUTP} and V_{OUTN} operate in different modes for a given input level. In 3-level operation, when V_{OUTP} is in mode (1), V_{OUTN} is in mode (2), and vice versa. In 5-level operation, when V_{OUTP} operates in mode (1), (2), (3), or (4), V_{OUTN} operates in mode (4), (3), (2), or (1), respectively. Thus when V_{OUTP} switches between V_{SS} and V_{DD1} (mode (1)), V_{OUTN} switches between V_{DD4} and V_{DD3} (mode (4)).

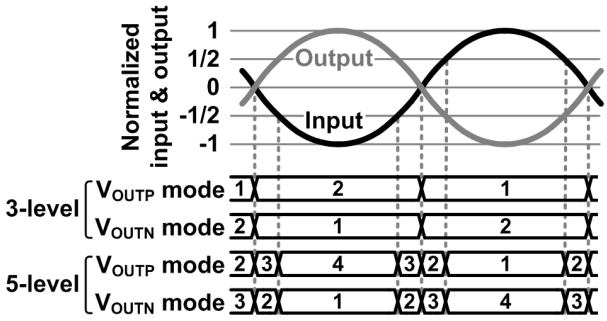


Figure 3.8: Mode selector.

3.3.2 Multi-Level PA Design

Fig. 3.9 shows the proposed PA with 2, 3 and 5 level outputs. The corresponding PA configurations consist of 4, 6, and 10 transistors respectively, and operate as a multi-level logic circuit. In the implementation, the mid-supply source level (V_{DD2}) is set to the standard power supply voltage, i. e., 1.2-V. For 2-level operation, the PA is configured as a conventional class-D PA which employs cascoded devices to support high full output voltage, V_{DD4}, (2.4-V) with 1.2-V core devices. The proposed 3-level PA adds an additional path using 2 extra transistors (M_{N5} and M_{P5}) that serve to sink, as well as source current, from half of full output voltage, V_{DD2}.

The 5-level PA is composed of 10 transistors. A pair of transistors is connected to one power-source or to ground. The V_{DD4} and V_{SS} paths are only for sourcing and sinking currents, respectively. Other paths serve as both sourcing and sinking paths. The PMOS and NMOS substrates are all connected to the highest (V_{DD4}) and lowest (V_{SS}) power-source, respectively, in order to avoid conduction through the body diodes. The proposed 5-level

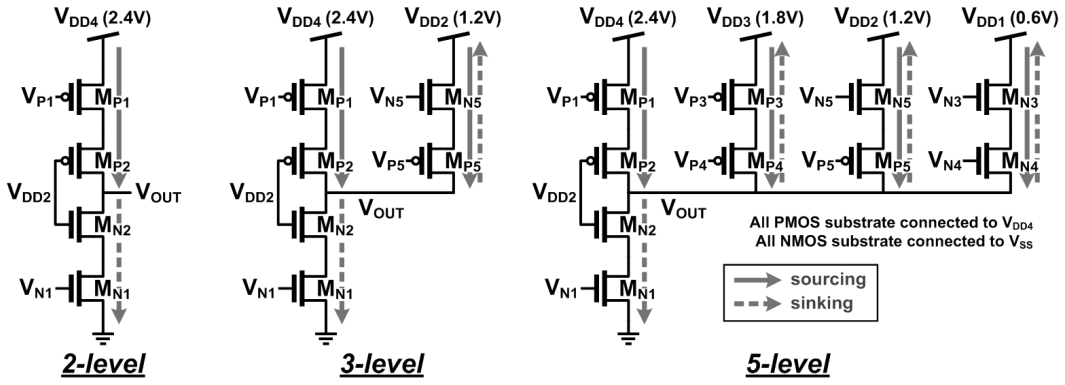


Figure 3.9: Proposed multi-level class-D power amplifier design.

PA can be reconfigured to operate as a 3-level or a 2-level PA by removing paths that are not required in a specific mode. M_{N4}/M_{P4} switches are required in both 2- and 3-level operation, to prevent the current flow between the output node and V_{DD1}/V_{DD3}, when reconfigured from the 5-level PA configuration.

Fig. 3.10 shows the topology of the differential 3-level PA. In order to achieve positive V_{OUT}, V_{OUTP} operates in mode (2) and V_{OUTN} operates in mode (1). When V_{OUTP} and V_{OUTN} are at V_{DD4} and V_{SS}, respectively, the output current flows from V_{DD4} to V_{SS}, such that V_{DD4} is the sourcing path and V_{SS} is the sinking path. When both V_{OUTP} and V_{OUTN} are at V_{DD2}, no output current flows in the V_{DD2} path and V_{DD2} serves as a virtual ground. Thus, 3-level operation is obtained without the requirement for an additional supply voltage source in the differential output stage compared to the 2-level case. A reference voltage source such as the resistive divider can be used to generate V_{DD2}.

In 5-level operation with differential output, V_{DD4}, V_{DD2}, and V_{SS} oper-

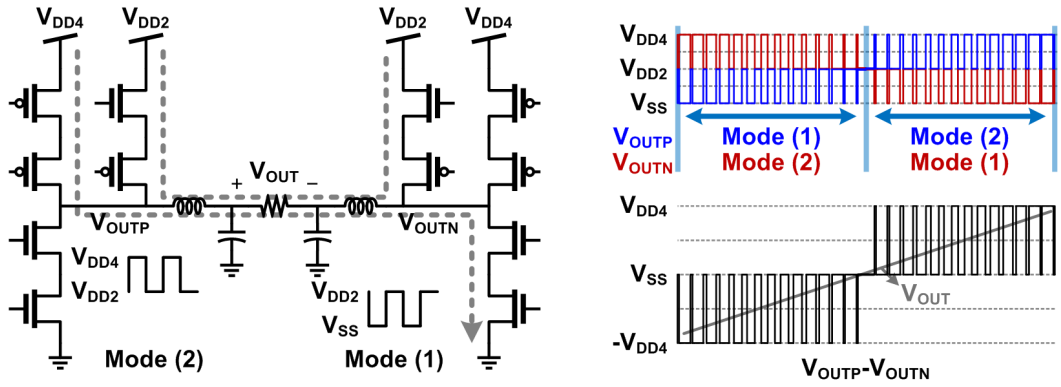


Figure 3.10: Differential output operation of 3-level PA.

Level	2-level			3-level				5-level					
V_{OUT}	V_{SS}	V_{DD4}	Φ-type	V_{SS}	V_{DD2}	V_{DD4}	Φ-type	V_{SS}	V_{DD1}	V_{DD2}	V_{DD3}	V_{DD4}	Φ-type
Mode	(1)			(1)	(2)			(1)	(2)	(3)	(4)		
V_{N1}	V_{DD2}	V_{SS}	Φ_2	V_{DD2}	V_{SS}	V_{SS}	Φ_1	V_{DD2}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Φ_1
V_{N3}					-		-	V_{DD1}	V_{DD3}	V_{DD1}	V_{DD1}	V_{DD1}	Φ_2
V_{N4}								V_{SS}	V_{DD3}	V_{DD3}	V_{DD3}	V_{DD3}	Φ_2
V_{N5}	-		-	V_{DD4}	V_{DD4}	V_{DD2}	Φ_2	V_{DD2}	V_{DD2}	V_{DD4}	V_{DD2}	V_{DD2}	Φ_1
V_{P5}				V_{DD2}	V_{SS}	V_{DD2}	Φ_{2b}	V_{DD2}	V_{DD2}	V_{SS}	V_{DD2}	V_{DD2}	Φ_{1b}
V_{P4}					-		-	V_{DD1}	V_{DD1}	V_{DD1}	V_{DD1}	V_{DD4}	Φ_{2b}
V_{P3}								V_{DD3}	V_{DD3}	V_{DD3}	V_{DD1}	V_{DD3}	Φ_{2b}
V_{P1}	V_{DD4}	V_{DD2}	Φ_{1b}	V_{DD4}	V_{DD4}	V_{DD2}	Φ_{1b}	V_{DD4}	V_{DD4}	V_{DD4}	V_{DD4}	V_{DD2}	Φ_{1b}

Table 3.1: Gate voltage of multi-level class-D PA.

ate in the same manner as in the 3-level operation. However, when V_{OUTP} and V_{OUTN} are connected to V_{DD3} and V_{DD1}, respectively, or vice versa, current flows from V_{DD3} to V_{DD1}. Thus, an additional sourcing and sinking path is required in 5-level operation. This could be implemented by using step-down converters such as synchronous PWM regulators.

3.3.3 Gate Driver

The output levels, and the corresponding gate control signals V_{N1}-V_{N5} and V_{P1}-V_{P5} that are required to achieve the corresponding output levels are shown in the Table 3.1. The output voltage (V_{OUT}) levels are shown as columns, V_{SS}, V_{DD1}, V_{DD2}, V_{DD3}, and V_{DD4}. Each mode involves switching between two levels. The gate control signal levels for each mode that provide a specific output level are shown in the Table 3.1. The shaded entries indicate the controls that need to change or switch to achieve a specific output. For instance, for mode (2) in the 5-level PA, the gate voltages V_{N3}, V_{N5}, and V_{P5}, which are the shaded part in the V_{DD1} and V_{DD2} columns, have to be controlled, when V_{OUT} switches between V_{DD1} and V_{DD2}. In order to switch V_{OUT} from V_{DD1} to V_{DD2}, [V_{N3}, V_{N5}, V_{P5}] change from [V_{DD3}, V_{DD2}, V_{DD2}] to [V_{DD1}, V_{DD4}, V_{SS}], respectively, while the other gate voltages, [V_{N1}, V_{N4}, V_{P1}, V_{P3}, V_{P4}], are held constant.

In a class-D PA design, a serious short-circuit condition called shoot-through can occur during switching transitions, when both sourcing and sinking paths turn on simultaneously. The shoot-through current increases power dissipation, and degrades the efficiency of the driver. Non-overlapping operation is employed to avoid shoot-through current. A logic block that provides non-overlapping clocks (Φ_1, Φ_{1b}, Φ_2, and Φ_{2b}) is implemented for this purpose, as shown in Fig. 3.4. This block is followed by the multi-level mode controller. Different clocks are applied to the gate driver in order to prevent the shoot-through current. The column indicated as Φ-type in Table 3.1 shows

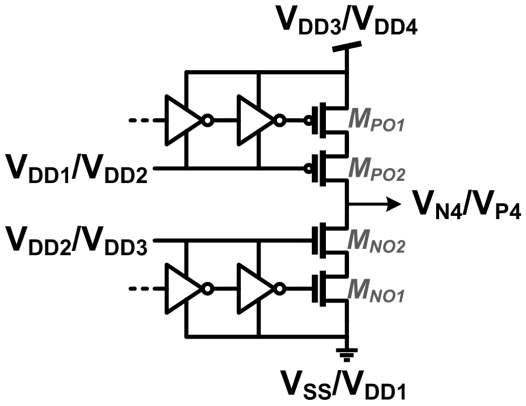


Figure 3.11: Output stage gate driver for generating V_{N4} and V_{P4} (see Fig. 3.9).

the appropriate clock type at each gate control signals. For instance, for mode (2) in the 5-level PA, the non-overlapping clocks given by Φ_2, Φ_1, and Φ_{1b}, are applied to [V_{N3}, V_{N5}, V_{P5}] which switch between [V_{DD3}, V_{DD2}, V_{DD2}] and [V_{DD1}, V_{DD4}, V_{SS}], respectively.

The gate voltage swings of the PA devices are limited to the standard power supply voltage level of 1.2 V, except for M_{N4} and M_{P4}. The gate voltages of M_{N4} and M_{P4}, V_{N4} and V_{P4}, experience a swing of up to 1.5 times the standard power supply voltage. V_{N4} switches between V_{SS} and V_{DD3} and V_{P4} switches between V_{DD1} and V_{DD4}. To avoid device breakdown with this voltage overdrive, the gate voltages of M_{N4} and M_{P4} are driven by a cascoded output stage as shown in Fig. 3.11. M_{NO1} and M_{PO1} are driven by inverters that use the standard supply voltage, and M_{NO2} and M_{PO2} prevent the drain-to-source voltage of each output transistor from exceeding the standard supply voltage. Other transistors in the PA are switched using standard voltage levels that

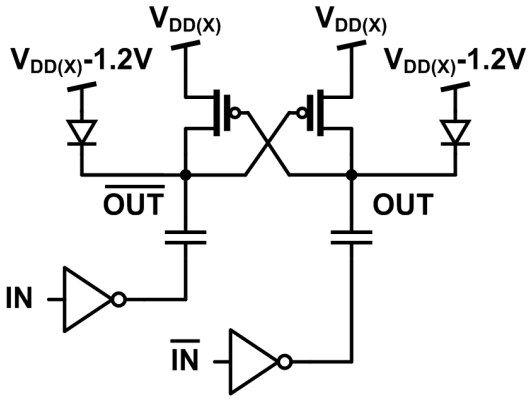


Figure 3.12: Level shifter.

can be easily applied by a simple inverter-based driver.

In order to apply the pulse-width modulated signal into the gate driver, a capacitively-coupled level-shifter is employed as shown in Fig. 3.12 [41], [42]. The pulse-width modulated input signal with 1.2 V swing is coupled to metal-oxide-metal (MOM) capacitors, and cross-coupled PMOS transistors ensure that the high logic level is at $V_{DD(X)}$ where X = 2, 3, or 4. Since both outputs change simultaneously, shoot-through currents at the switching instant are avoided. Coupling capacitors of 920 fF are used which ensures that for a switching rate in the range of tens-to-hundreds of MHz, the high logic level is $V_{DD(X)}$ and the low logic voltage level is $V_{DD(X)}$ - 1.2 V. The diodes that are connected to each of output nodes, with $V_{DD(X)}$ - 1.2 V at the anodes, are used to ensure proper start-up. These diodes also limit the lowest voltage to $V_{DD(X)}$ - 1.2 V - V_{DIODE}.

3.3.4 Folded Duty-cycle Variation

The output PWM signal is determined by the duty-cycle and the source/sink levels in the PA for the corresponding input (Fig. 3.13a). With a 5-level switching scheme, the typical duty-cycle as a function of the input signal level is shown in Fig. 3.13b. In a PLL-PWM driver, the PLL is unable to maintain lock with this duty-cycle variation if the mode changes, due to an abrupt duty-cycle jump from 100% to 0% or vice versa. This causes severe harmonic distortion. To address this issue, a folded duty-cycle variation is proposed, as shown in Fig. 3.13c.

In this approach, in any one mode, the duty cycle is either linearly increased with the input signal, or linearly decreased in response. The first state is termed the BUF state (for buffer), while the second state is termed the INV state (for inverter). In each mode, the output varies between a lower bound of V_{SINK} and an upper bound of V_{SRC}. Consider the typical operation in BUF state. Here V_{OUT} can be expressed as $D \times V_{SW} + V_{SINK}$ where V_{SW} is the switching voltage swing which equals V_{SRC}-V_{SINK}, and D is the duty-cycle. As D varies from 0 to 1, V_{OUT} varies from V_{SINK} to V_{SRC}. In the INV state, the duty-cycle is changed from D to 1-D. Thus the small signal in the INV state maps to a duty cycle of 1, while the largest signal maps to 0. V_{OUT} is then expressed as $(1\text{-}D) \times V_{SW} + V_{SINK}$. The output still switches from V_{SINK} to V_{SRC}. Since the duty cycle is continuous at the boundaries of various modes, mode changes do not lead to abrupt transitions, thereby avoiding the potential for losing lock.

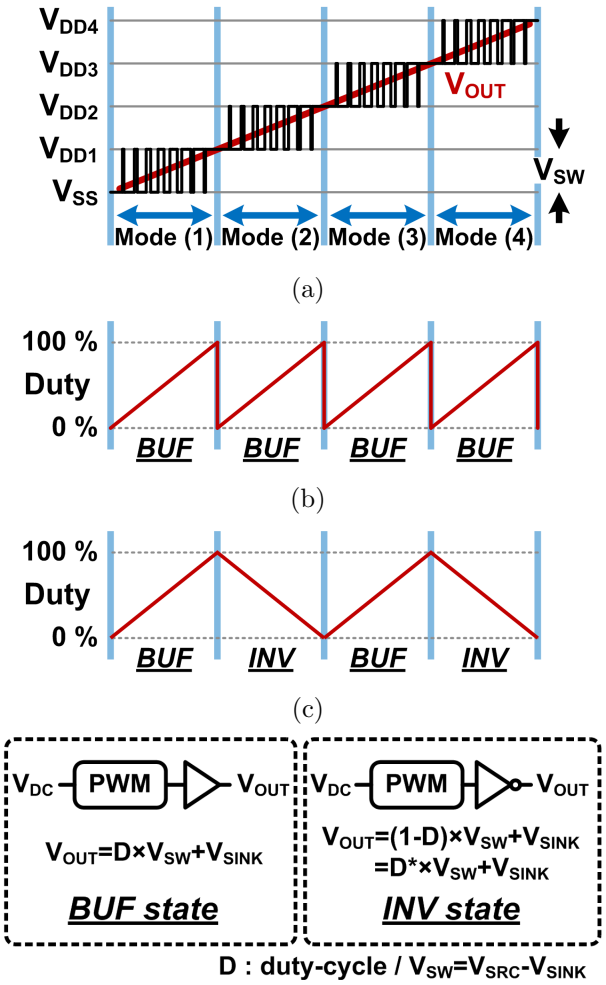


Figure 3.13: (a) 5-level PWM output. (b) Typical duty-cycle variation. (c) Folded duty-cycle variation. (d) BUF and INV state.

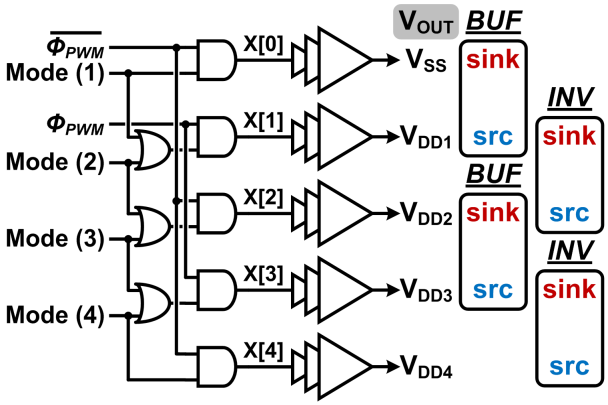


Figure 3.14: Multi-level mode controller.

The block diagram of multi-level mode controller for folded state conversion is shown in Fig. 3.14. Folded duty-cycle operation is achieved by properly multiplexing the PWM signal Φ_{PWM} and the inverted PWM signal $\overline{\Phi_{PWM}}$ to the output, based on the mode control signals. X[0:4] are signal nodes that enable the V_{SS}, V_{DD1}, V_{DD2}, V_{DD3}, and V_{DD4} paths, respectively. The operation of this block is illustrated by means of an example.

Consider the case where the mode (1) control signal is high and other mode control signals are low, which enables X[0] and X[1]. In this case, X[0] receives the inverted PWM signal ($\overline{\Phi_{PWM}}$) and X[1] receives the original PWM signal (Φ_{PWM}). Thus the driver operates in the BUF state, such that V_{OUT} is connected to V_{SS}, when Φ_{PWM} is low, and V_{OUT} is connected to V_{DD1}, when Φ_{PWM} is high. If the mode (2) control signal is high and other mode control signals are low, then X[1] receives Φ_{PWM} and X[2] receives $\overline{\Phi_{PWM}}$. Now the design operates in the INV state because V_{OUT} is connected to V_{DD1} when Φ_{PWM} is high, and to V_{DD2} when Φ_{PWM} is low. In 5-level operation,

by applying Φ_{PWM} to X[0], X[2], and X[4], and $\overline{\Phi_{PWM}}$ to X[1] and X[3], folded operation is thus automatically achieved, because V_{DD1}, V_{DD2}, and V_{DD3} operate as both sourcing and sinking paths. Mode (1) and mode (3) operation uses the BUF state, while mode (2) and mode (4) operation uses the INV state, where the BUF and INV states are shown in Fig. 3.14. The same approach can be employed for 3-level operation to achieve seamless mode-switching. In 3-level operation, mode (1) operation uses the BUF state, while mode (2) operation uses the INV state.

In 3/5-level PA operation, a dead-zone can be observed within the available operating range near 0 or 100 % duty-cycle. However, the dead-zone is narrow enough that the PLL does not lose lock, if the output does not remain in the dead-zone for a sufficiently long time, with a time-varying input. In 5-level PAs especially, it is also critical, that the noise level on the threshold lines in the mode selector be adequately small, as pointed out in the measurements sections.

3.4 Measurement Results

The design has been implemented in a 130-nm CMOS process. Fig. 3.15 shows the chip photograph. The modulator uses a 1.2-V supply voltage and the multi-level PA uses supply voltages of 0.6-V, 1.2-V, 1.8-V, and 2.4-V. The chip has been tested with variable switching frequencies from 40-170 MHz with differential load resistor of 10 Ω. An LC filter with an inductor of 88 nH and a capacitor of 10 nF is employed as the output LPF.

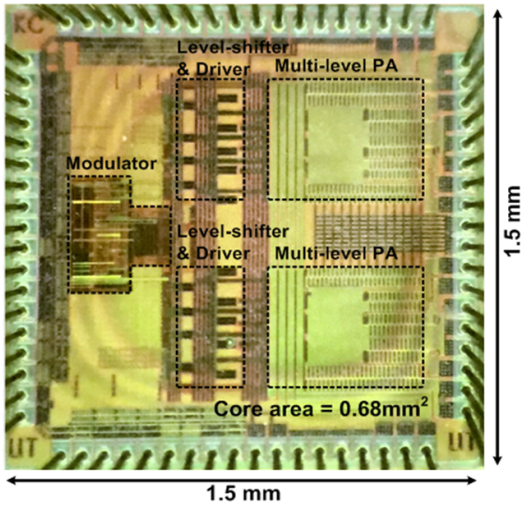


Figure 3.15: Chip photograph.

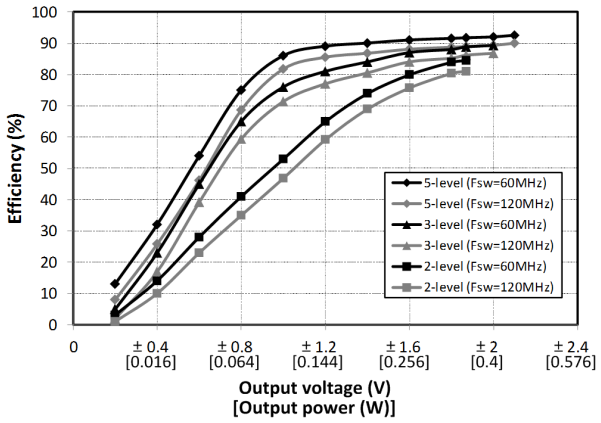


Figure 3.16: Measured power efficiency as a function of the output voltage (output power) with 2/3/5-level PA at 60/120 MHz switching frequency for $R_L = 10\ \Omega$.

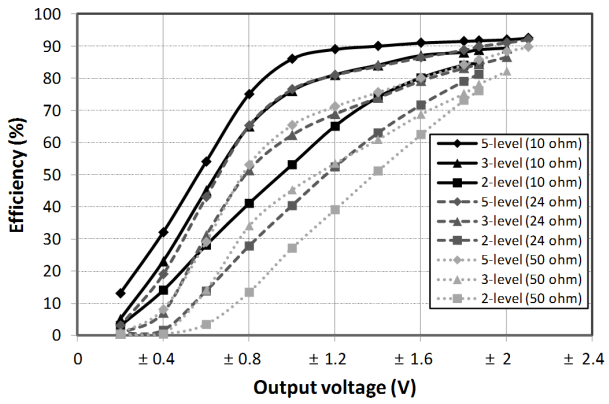
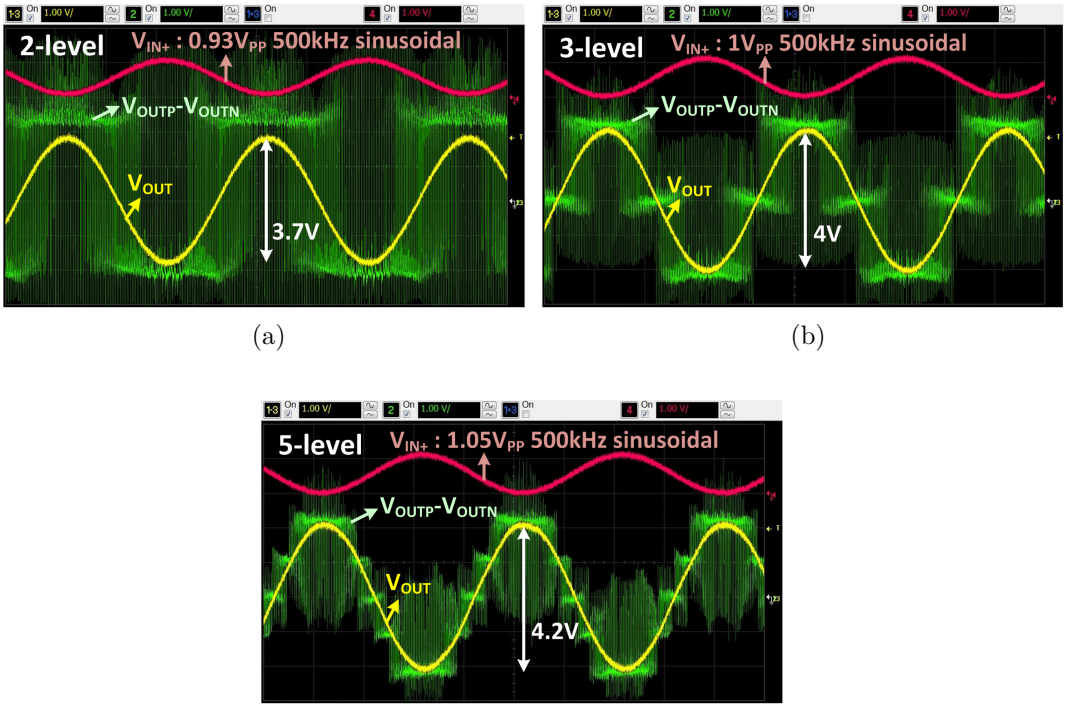


Figure 3.17: Measured power efficiency as a function of the output voltage with 2/3/5-level PA for different load resistance at $f_{SW} = 60$ MHz.

Fig. 3.16 shows the measured power efficiency of the output-stage with 2/3/5-level PA for different switching frequencies. The output-stage power efficiency includes the driver and the PAs. In the 5-level configuration, the efficiency at dead-zone around half of the peak output voltage range is interpolated in Fig. 3.16 in order to validate the performance of the output-stage in the proposed 5-level PA design[4]. Implementing 2-level and 3-level PA operation by reconfiguring the 5-level PA introduces additional parasitic capacitance, which slightly degrades the efficiency in 2/3-level operation. The reduced output voltage swing for 3/5-level PA operation makes it possible to drive a higher output power with the same duty-cycle. Increasing the PA switching levels improves back-off power efficiency as well as peak power efficiency due to reduced dynamic loss, especially at higher switching frequency.

[4]It is possible to do this here, since an ac signal is applied. Thus the output spends a very small time in the dead-zone.



(a) (b)

(c)

Figure 3.18: Measured waveform of 2/3/5-level PA operation with 500kHz sinusoidal input for f_{SW} = 60 MHz. (a) 2-level PA. (b) 3-level PA. (c) 5-level PA.

The output-stage power efficiency is also measured with different loads with f_{SW} = 60 MHz as shown in Fig. 3.17. It is important to study this behavior, since the load impedance varies in an actual power-line environment. The efficiency is decreased when the load resistance is increased as the output power is reduced. While the static loss is reduced when the load resistance is increased because the output current is reduced, the switching loss stays unchanged. The higher level PA still improves back-off as well as peak efficiency.

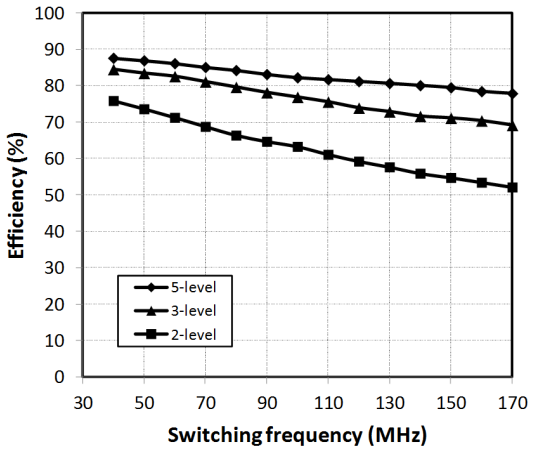


Figure 3.19: Measured full driver efficiency vs. switching frequency (f_{SW}) with the maximum available 500 kHz sinusoidal input.

Fig. 3.18 shows the measured waveform for the maximum peak-to-peak 500 kHz sinusoidal signal input (PAPR = 3 dB) at 60 MHz switching frequency. Peak-to-peak input voltage of 0.93/1.0/1.05-V is applied to the 2/3/5-level PAs respectively. This maps to the maximum available output power in each case, which is different depending on the PA configuration. The corresponding average output power is 175/200/220 mW. By employing folded duty-cycle variation, the output follows the input without losing lock at mode conversion boundaries in 3/5-level operation. Fig. 3.19 and Fig. 3.20 show the full driver efficiency including the modulator, and THD by varying the switching frequency with the maximum peak-to-peak 500 kHz sinusoidal signal input, respectively. The efficiency is decreased when the switching frequency is increased since the switching loss is larger, especially for the 2-level PA. THD under -60 dB is achieved for 2/3-level PA when the switching fre-

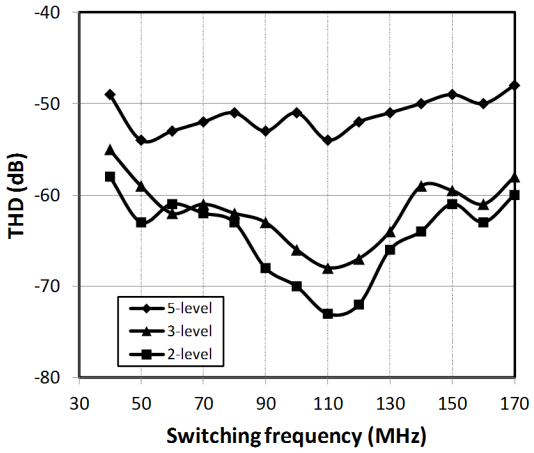


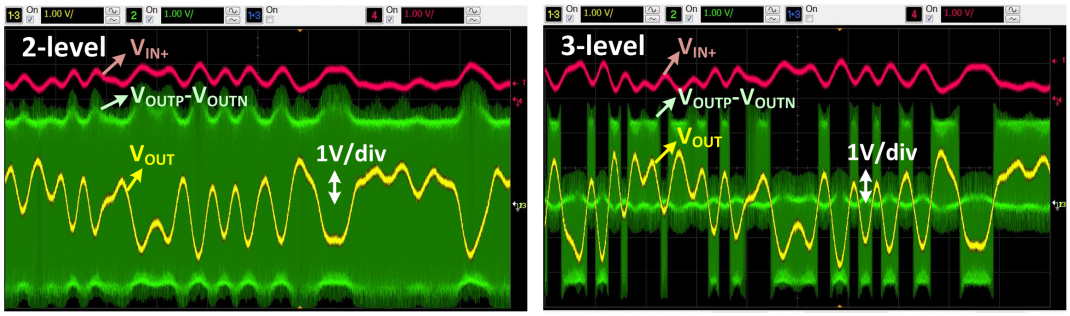
Figure 3.20: Measured full driver THD vs. switching frequency (f_{SW}) with the maximum available 500 kHz sinusoidal input.

quency is larger than 60 MHz. The lowest THD is achieved around 110 MHz of switching frequency which implies that the VCO has the best linearity performance around 55 MHz output frequency. THD of the 5-level PA is limited to about -54 dB. Although the lock of the loop in 5-level PA is never lost due to the use of the folded duty-cycle variation, the distortion caused by additional mode switching compared to 2/3-level operation increases the THD of the 5-level PA. Table 3.2 summarizes the performance and provides a comparison with prior work. The PLL-PWM design is also compared with high switching frequency buck converters, for DC operation. While this design is not a buck converter since it is intended for providing time-varying output signals, the designs are similar since they both employ synchronous PWM and PMOS/NMOS switching output stage for high-side/low-side switches, that operate at similar values of switching frequency. The DC conversion efficiency

	This work						JSSC 2013 Huang		JSSC 2014 Cheng		JSSC 2015 Kinyua	JSSC 2014 Lu
	5-level*		3-level*		2-level		2-level		2-level		2-level	2-level
Technology	0.13 µm						0.13 µm		0.13 µm		55 nm	0.13 µm
Supply voltage	0.6 / 1.8 / 2.4 V		2.4 V		2.4 V		1.2 V		3.3 V		5.5 V	4.8 V
Output filter	LC off-chip L = 88 nH / C = 10 nF						LC on-chip L ≈ 7 nH C = 9.8 nF		LC off-chip L = 330 nH C = 1 µF		Filter-less	LC off-chip L = 500 nH
Load	R_L = 10 Ω						I_L = 0.225 A		I_L = 0.25 A		R_L = 8 Ω	R_L = 6.8 Ω
DC conversion performance												
F_{SW} (MHz)	120						100		30		N/A	N/A
P_{PEAK} (W)	η	0.44	0.9	0.4	0.87	0.35	0.81	0.23	0.9	0.6	0.86	
P_{OUT1} (W)** (P_{OUT1}/P_{PEAK})	η	0.31 (0.7)	0.89	0.28 (0.7)	0.84	0.25 (0.7)	0.75	0.16 (0.7)	0.72	0.45 (0.75)	0.82	
P_{OUT2} (W)** (P_{OUT2}/P_{PEAK})	η	0.22 (0.5)	0.87	0.2 (0.5)	0.81	0.18 (0.5)	0.65	0.11 (0.5)	0.53	0.3 (0.5)	0.75	
AC amplification performance												
Frequency of sinusoidal input	500 kHz						N/A		N/A		1 kHz†	60 kHz
P_{OUT}	220 mW		200 mW		175 mW						1.35 W††	1.1 W
F_{SW} (MHz)	60	120	60	120	60	120					2.133	20
η	0.86	0.81	0.83	0.74	0.71	0.59					0.85	0.8
THD (dB)	-53	-52	-62	-67	-61	-74					-77†††	-67

* 1.2 V reference level is employed for virtual ground level.
** P_{OUT1} and P_{OUT2} are back-off power levels achieved by lowering output voltage from the peak power for maximum η condition. (For resistive load R_L, $P_{OUT} \propto V_{OUT}^2$; For fixed current load I_L, $P_{OUT} \propto V_{OUT}$)
† Signal bandwidth is up to 20 kHz.
†† 90% of peak output power (1.5W).
††† Estimated THD+N at 1.35W. THD+N at peak output power (1.5W) = 0.1%.

Table 3.2: Performance summary.



(a) (b)

Figure 3.21: Measured waveform of 2/3-level PA operation with D8PSK modulation at $f_{SW} = 60$ MHz. (a) 2-level PA. (b) 3-level PA.

at back-off as well as peak output power is compared by varying the output voltage. The proposed multi-level PA architecture improves back-off as well as peak efficiency at high switching frequency. Additionally, it achieves significantly higher signal bandwidth, and comparable or even better efficiency with sinusoidal signal amplification while operating at higher switching frequency.

The driver with 2/3-level PA has been tested with a modulated, high PAPR, 500kHz wide signal, with 60 MHz switching frequency. The measured waveform is shown in Fig. 3.21. The signal employed in this case has a PAPR of 8.2 dB, and is implemented by using the real part of a D8PSK signal. The average output power is observed to be 52 mW and 60 mW, and the efficiency is 37% and 52% for the 2/3-level PA, respectively. While the 5-level PA was verified with constant amplitude signals, it could not be verified with the D8PSK signal used for the 2/3 level PA. Based on simulation, it was observed that excessive threshold line noise in the mode selector would cause the 5-level

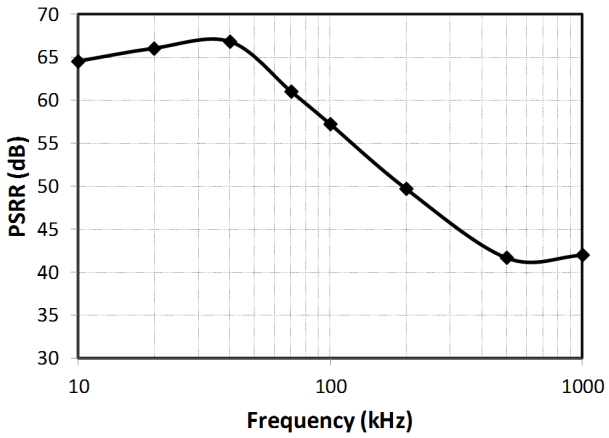


Figure 3.22: Measured PSRR.

PA to intermittently loose lock, when the input signal stayed near a threshold boundary. This is not a case for constant amplitude signals, such as FSK, PM, FM, or for AM signals, where the amplitude does not stay at the boundaries, since the input crosses the threshold boundaries rapidly.

Fig. 3.22 shows the measured power supply rejection ratio (PSRR). PSRR is measured by coupling $200mV_{p\text{-}p}$ sinusoidal signal into power supply of 2-level PA and varying its frequency. PSRR is above 60 dB when the sinusoidal frequency is below 70 kHz and it decreases to 40 dB at 500 kHz.

3.5 Conclusion

A high speed PWM driver with multi-level class-D PA is demonstrated. Employing a PLL-based PWM architecture enables high switching frequency operation with high linearity. A multi-level output stage provides high peak- as well as back-off efficiency, at high switching frequency by reducing the switch-

ing levels. Folded duty-cycle variation is proposed, which ensures seamless operation for a continuous input signal. In the differential implementation, 3-level operation can be implemented without the requirement for an additional supply source compared to 2-level operation. The proposed PWM driver operates from 40 MHz to 170 MHz and is demonstrated using a sinusoidal input as well as a modulated signal with high PAPR. Highly linear operation is achieved in 2-level as well as the 3/5-level modes, that offer higher efficiency.

Chapter 4

An Efficient Buck/Buck-Boost Reconfigurable LED Driver Employing SIN^2 Reference

4.1 Introduction

Light emitting diodes (LED) are becoming a commonly-used light source for general-purpose applications because of their long lifetime and high efficiency compared to fluorescent and incandescent lamps. Fluorescent lamps had gained popularity compared to incandescent lamps due to better efficiency before high performance LED devices became available. However, LED technology has dramatically improved the performance beyond that offered by fluorescent lamps, in both the lifetime and efficiency [43]. High-brightness and high-efficiency LEDs are now widely used in lighting solutions [44, 45, 46, 47, 48, 49, 50, 51] and LCD backlight solutions [52, 53, 54]. Owing to high-efficiency, and a wide range of options with regards to form factors and light colors, LED lighting is also a key part of emerging smart-home technologies (chapter 1.1).

A key design challenge for LED technology arises from the requirement for an efficient driver. For efficient transmission of energy from a source to a load, it is desirable to maximize the real power delivered by the AC line voltage

(V_{AC}) while minimizing RMS current. Power factor (PF), which is defined as the ratio of real power to apparent power in a load, is a metric that determines how efficiently electrical power is being transferred to the load. To achieve high PF from an AC line voltage, V_{AC}, the phase of the AC line current (I_{AC}) has to be aligned with V_{AC}. Furthermore the shape of the waveform has to follow a sinusoidal form. Total harmonic distortion (THD) of I_{AC} is another important consideration. A high THD is not acceptable since it can cause interference in the operation of other electronic systems and also shorten the life span of the equipment [55].

Inductor-based switching-type DC-to-DC converters are widely used in off-the-shelf LED lamp drivers and are shown in Fig. 4.1a and Fig. 4.1b. The DC-to-DC converter can be a buck converter, which can step-down the voltage from the input to the output, or it can be a buck-boost or flyback converter that can step-down or step-up the voltage from the input to the output. In order to design a simple and low-cost LED driver, the DC-to-DC converter can use DC supply from the rectified AC input by filtering the AC ripple with a large capacitor (Fig. 4.1a). However, this approach leads to significant reactive power due to different shapes of the supply voltage and the current flowing in the AC line, which lowers the PF. The PF can be improved by the use of a controller-based active [56, 57], or valley-fill passive [58] power factor correction (PFC) circuit, in combination with a DC-to-DC converter [44, 45, 46, 47] to drive LEDs, as shown in Fig. 4.1b. However, these approaches both increase the manufacturing cost and the power consumption.

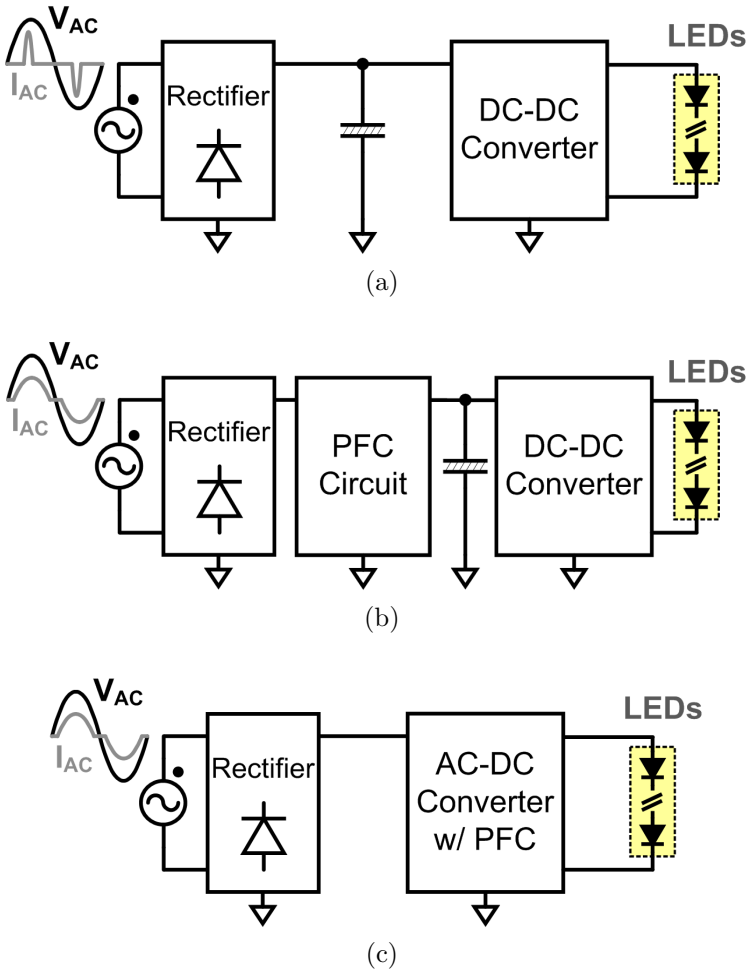


Figure 4.1: LED drivers. (a) DC-DC converter. (b) DC-DC converter with power factor correction circuit. (c) AC-DC converter with power factor correction.

Recently, LED drivers that can directly drive LEDs from an AC outlet source (Fig. 4.1c) and perform PFC have been demonstrated using AC-to-DC conversion [48, 49, 50, 51]. The AC-to-DC converters are also based on inductor-based switching regulators, and employ a basic architecture that is almost identical to a DC-to-DC converter. However, unlike a DC-to-DC converter, the rectified AC signal, instead of a DC supply, is applied to the load, and the time-varying signal is used as the reference signal for the regulator control loop. AC-to-DC converters have been implemented by using a non-isolated single-stage buck converter [48, 49] and an isolated transformer-based flyback converter [50, 51]. A non-isolated driver offers benefits of efficiency and low cost, while the isolated type is also attractive due to better safety. These designs perform PF correction and exhibit low total harmonic distortion by directly driving the load from the rectified AC source.

Conventional AC-to-DC LED drivers [48, 49, 50, 51] employ a rectified sine-wave reference ($|\sin(\phi)|$) to control the inductor current. The shape and the phase of the AC input current is determined primarily by the inductor current. By comparing the sensed inductor current to the reference, the inductor current is forced to follow the shape of the reference, which has a rectified sine-wave form. The rectified sine-wave reference helps to improve the PF.

In this chapter, an efficient LED driver based on peak current control is described that uses a $|\sin(\phi)|$ as well as a $\sin^2(\phi)$ term in I_L for both buck and buck-boost converters. The proposed reference control can improve the PF as well as the THD compared to a design that uses a rectified sinusoidal

reference. In addition, the design ensures that the peak of the inductor current maintains a constant level that is invariant for different AC line voltages.

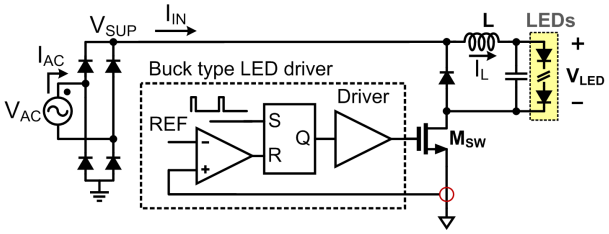
This chapter is organized as follows. Section 4.2 describes efficient PF correction methods using a $|\sin(\phi)|$ as well as a $\sin^2(\phi)$ reference for buck and buck-boost converters. Section 4.3 describes a complete architecture with the proposed reference generation circuits. Section 4.4 describes measurement results, and the conclusion follows in Section 4.5.

4.2 Power Factor Correction for Buck/Buck-Boost Converters

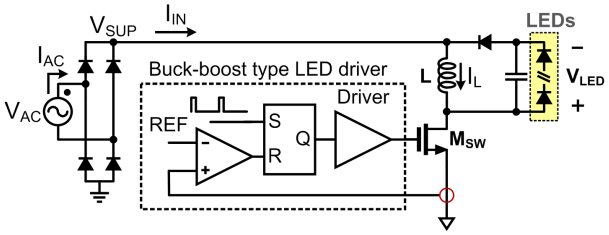
In order to transmit energy efficiently from an AC power source to a load, and minimize losses, the average power needs to be maximized while the RMS current and voltage need to be minimized. PF is a metric that determines how efficiently electrical power is transferred to a load and it is expressed as,

$$PF = \frac{P_{LOAD}}{V_{RMS} \cdot I_{RMS}}, \tag{4.1}$$

where V_{RMS} is RMS voltage of the source, I_{RMS} is RMS current of the source, and P_{LOAD} is the average power in the load. To achieve a high PF, the phase of the AC input current needs be aligned with that of the AC input voltage, and the shape of the AC input current has to follow the sinusoidal shape of AC input voltage. Hence, the maximum PF that can be obtained for resistive loads is unity.



(a)



(b)

Figure 4.2: AC-DC converter for LED drivers. (a) Buck type. (b) Buck-boost type.

Step-down converters such as buck converters, and step-down-and-step-up converters such as buck-boost converters or flyback converters, are typically used to implement LED drivers which directly drive the LEDs from an AC outlet.

Unlike a conventional rectified sinusoidal reference, an optimized reference signal that contains a $\sin^2$ factor is proposed here, to maximize the PF and minimize THD in buck and buck-boost converters for AC-to-DC conversion. Buck and buck-boost type LED drivers that employ direct AC-to-DC conversion are shown in Fig. 4.2. The driver controls the active switch (M_{SW}) by comparing the sensed inductor current (I_L) to the reference signal and forces the shape of the inductor current to follow that of the reference signal.

4.2.1 Buck Converter

Fig. 4.2a shows a buck type LED driver using AC-to-DC conversion. The buck converter is a switching topology that lowers the input supply voltage, V_{SUP}, to the output LED voltage, V_{LED}. The duty-cycle (D) determines the ratio between the input voltage and the output voltage, which can be expressed as below,

$$V_{LED.B} = D \times V_{SUP} \tag{4.2}$$

where $V_{LED.B}$ is the output LED voltage of the buck converter.

In a buck converter, the output current flows continuously when the converter is operating in continuous conduction mode (CCM) because the inductor is always connected to the output voltage. Thus, a relatively small capacitor can be used at the output voltage, for reducing the voltage ripple across the LEDs.

The input current (I_{IN}) of a buck converter only flows when the switch is in the ON-state. Thus I_{IN} is given by product of the duty-cycle (D) and the inductor current (I_L). The duty-cycle is determined by V_{LED}/V_{SUP}, where V_{LED} is the forward voltage of LED output string and V_{SUP} is the rectified AC input voltage. V_{SUP} can be represent as $V_{AC.PEAK} \times |\sin(\phi)|$. $V_{AC.PEAK}$ is the peak voltage of V_{SUP}, that is $\sqrt{2} \times V_{SUP}$. Thus, I_{IN} can be represented as below,

$$I_{IN.B} = D \times I_L = \frac{V_{LED}}{V_{SUP}} \times I_L = \frac{V_{LED}}{V_{AC.PEAK} \cdot |\sin(\phi)|} \times I_L \qquad (4.3)$$

where $I_{IN.B}$ is the input current of the buck converter.

In order to achieve a high PF and low THD, it can be observed from the above equation that I_{IN} needs to have a rectified sinusoidal form, $|\sin(\phi)|$. However, if V_{LED} is assumed to be a DC voltage, and I_L follows the rectified sine-wave shape of the reference, then I_{IN} will be a DC level. The DC form of I_{IN} will degrade the PF and also increase the THD. Therefore, if I_L has a $\sin^2(\phi)$ shape, instead of the rectified sine-wave shape, a rectified sinusoidal form of I_{IN} can be achieved.

In a practical design, I_L has to have a shape that is a combination of $|\sin(\phi)|$ and $\sin^2(\phi)$, because V_{LED} is not an ideal DC level. V_{LED} is determined by the I-V characteristic of the LED, which typically follows an exponential relationship. Since the LED current is varying in response to the shape of I_L, V_{LED} holds a relatively constant DC value when it is fully turned-on by a sufficiently high I_L, however, V_{LED} decreases when I_L is low. Thus V_{LED} has a small $|\sin(\phi)|$ component, in addition to the DC value. Consequently, the optimal shape of I_L has to be between $|\sin(\phi)|$ and $\sin^2(\phi)$.

4.2.2 Buck-Boost Converter

Fig. 4.2b shows a buck-boost type LED driver. Unlike a buck converter, the output voltage of the buck-boost converter can step-up as well as step-down

the output voltage relative to the input. The relationship between the input voltage and output voltage can be expressed as below,

$$V_{LED.BB} = \frac{D}{1-D} \times V_{SUP} \tag{4.4}$$

where $V_{LED.BB}$ is the output LED voltage of the buck-boost converter and D is the duty-cycle of the waveform applied to the switch M_{SW}.

In a buck-boost converter, the inductor is connected to the input when the switch is in the ON-state and it is connected to the output when the switch is in the OFF-state. Therefore, the current only flows into the LED when the switch is OFF. A large capacitor is thus required at the output, across the LED, to filter the discontinuous output current.

The input current $I_{IN.BB}$ in a buck-boost converter is also given by the product of the duty-cycle (D) and inductor current (I_L), where the duty-cycle is $V_{LED}/(V_{LED} + V_{SUP})$. Thus, $I_{IN,BB}$ can be represented as below,

$$I_{IN.BB} = D \times I_L = \frac{V_{LED}}{V_{LED} + V_{SUP}} \times I_L = \frac{V_{LED}}{V_{LED} + V_{AC.PEAK} \cdot |\sin(\phi)|} \times I_L \tag{4.5}$$

In this case, if V_{LED} is assumed to be a DC voltage, I_L has to be of the form of $|\sin(\phi)| + V_{AC.PEAK}/V_{LED} \times \sin^2(\phi)$ in order to obtain a rectified sinusoidal I_{IN}. If V_{LED} is low due to the use of a small number of LEDs, the desired form of I_L is close to $\sin^2(\phi)$. Increasing the number of LEDs will increase the $|\sin(\phi)|$ factor in the form of I_L. In a practical design, since V_{LED} will contain

Buck	Input current (I_{IN})
	$I_{IN} = Duty \cdot I_L = \frac{V_{LED}}{V_{SUP}} \cdot I_L = \frac{V_{LED}}{V_{AC.PEAK} \cdot \lvert\sin(\Phi)\rvert} \cdot I_L$
	Desired inductor current (I_L)
	$I_L = I_{PEAK} \cdot \sin^2(\Phi)$
Buck -boost	Input current (I_{IN})
	$I_{IN} = Duty \cdot I_L = \frac{V_{LED}}{V_{LED}+V_{SUP}} \cdot I_L = \frac{V_{LED}}{V_{LED}+V_{AC.PEAK} \cdot \lvert\sin(\Phi)\rvert} \cdot I_L$
	Desired inductor current (I_L)
	$I_L = I_{PEAK} \cdot \lvert\sin(\Phi)\rvert + \frac{V_{AC.PEAK}}{V_{LED}} \cdot I_{PEAK} \cdot \sin^2(\Phi)$

Table 4.1: Input current and desired inductor current for buck converter and buck-boost converter.

a $|\sin(\phi)|$ component due to the V-I characteristic of the LEDs, I_L needs an additional $|\sin(\phi)|$ term.

Thus for both Buck and Buck-boost converters, the desired inductor current has to be form of $\alpha \times |\sin(\phi)| + (1-\alpha) \times \sin^2(\phi)$ $(0 \leq \alpha \leq 1)$. The coefficient α will be a fixed value in the case of buck converters, while in buck-boost converters, α will vary based on the number of LEDs. The input current and desired inductor current are summarized in Table 4.1.

4.3 Complete LED Driver Architecture

Fig. 4.3 shows the architecture of proposed LED driver. The driver is designed to provide pulse-width-modulation (PWM) and pulse-frequency-modulation (PFM) operation. Table 4.2 describes the operating modes of the proposed driver. In the PWM mode, the output of the driver switches at a fixed switching frequency of 43 kHz and the maximum duty-cycle is limited

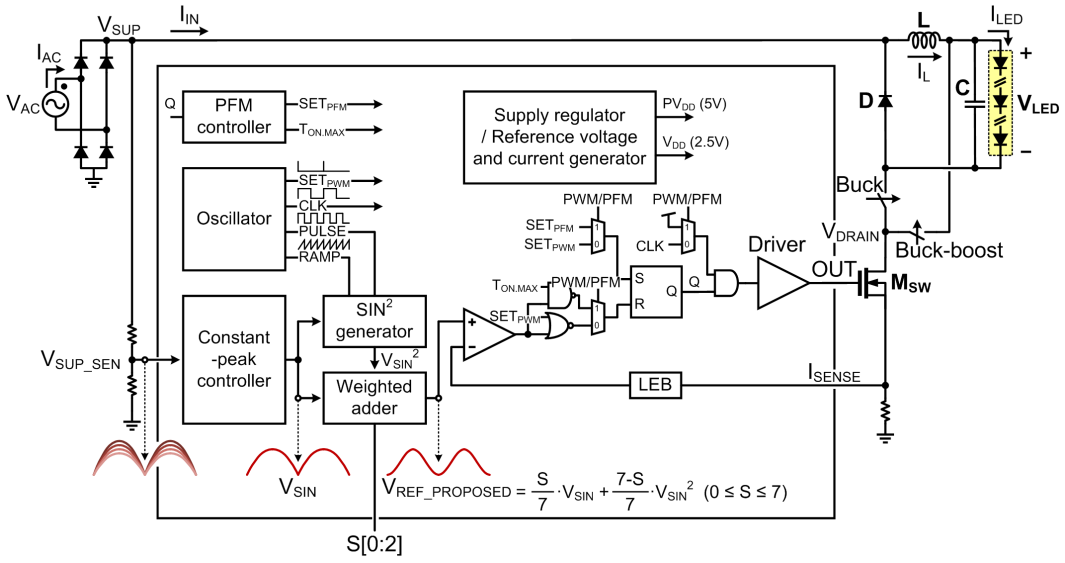


Figure 4.3: Architecture of proposed LED driver.

to 50%. In the PFM mode, the driver operates with constant OFF-time control. Once the sensed inductor current, I_{SENSE}, exceeds the reference level, $V_{REF\_PROPOSED}$, the output maintains a low level with a set OFF-time of 13 µs. The maximum duty-cycle is limited to 80%, such that the high-state of the output cannot be longer than 52 µs. The PWM mode is used for the buck converter and the PFM mode is used for buck and buck-boost converters. To generate the desired reference voltage of the form $\alpha \times |\sin(\phi)| + (1-\alpha) \times \sin^2(\phi)$ $(0 \leq \alpha \leq 1)$, for both buck and buck-boost converter, V_{SIN} and $V_{SIN}{}^2$ signals that have a constant peak, and provide $|\sin(\phi)|$ and $\sin^2(\phi)$, respectively, are generated from the sensed voltage (V_{SUP_SEN}), while the ratio α is adjusted by a weighted adder.

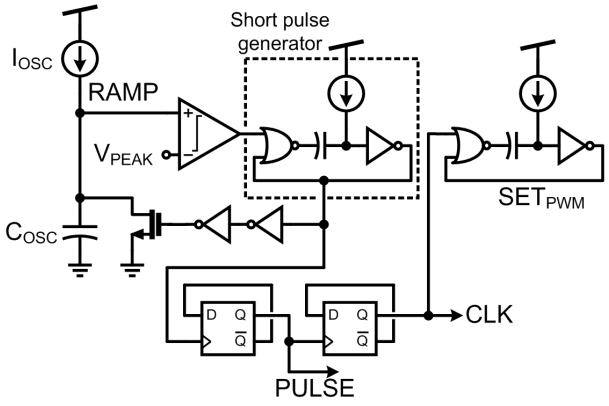
Mode	Operation	Max. duty-cycle
PWM	43 kHz fixed switching frequency	50%
PFM	Constant OFF-time (~13μs)	80%

Table 4.2: Operation modes of proposed driver.

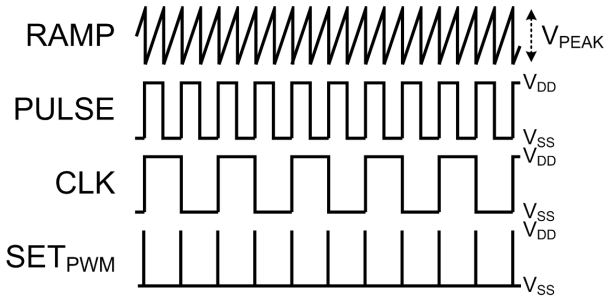
4.3.1 Oscillator

Fig. 4.4 shows the block diagram and timing diagram of the oscillator. A relaxation-mode oscillator is employed and it generates the necessary timing and control signals for the architecture. The capacitor, C_{OSC}, is charged by the current source, I_{OSC}, and generates a RAMP signal. When the RAMP signal exceeds V_{PEAK} (0.5 V), a short pulse is generated at the rising edge of the output of the comparator. This short pulse resets the capacitor and is also applied to a frequency divider to generate the PULSE signal, which has a 50% duty-cycle. The signal PULSE is divided by 2 again and generates the CLK signal which has a frequency of approximately 43 kHz.

In the PWM mode, the CLK signal functions as the main operating clock and the output is set to high at every cycle of the CLK signal by using SET_{PWM}. The PULSE and the RAMP signals are used in the SIN^2 generator to generate the ${V_{SIN}}^2$ reference by using a switching multiplier.



(a)



(b)

Figure 4.4: Oscillator. (a) Block diagram. (b) Timing diagram.

4.3.2 Constant Peak Controller

If the rectified sinusoidal reference is derived from the rectified AC input voltage, V_{SUP}, then the reference can vary in response to AC line voltage variation and in turn vary the inductor current. This will cause the output power of the LEDs to vary. Thus, a constant reference level is essential to maintain a constant output power regardless of the AC line voltage.

A rectified sinusoidal reference with a constant peak level can be implemented by using a current DAC and an up-down counter [50]. In this approach, the peak level of the reference continuously tracks a given threshold level to maintain a constant peak amplitude. However, when the peak amplitude reaches the given threshold and approaches steady state, it still toggles around the threshold level.

A constant peak level without toggling in the steady state is proposed here, by employing a hysteresis range for safe operation, as shown in Fig. 4.5. V_{SUP_SEN}, which is an attenuated version of the supply voltage V_{SUP}, is applied to the generator. The amplitude of V_{SIN} starts from 1/5 of V_{SUP_SEN}. Two comparators compare V_{SIN} with 0.5 V and 0.53 V to determine the peak of V_{SIN}. Until the peak of V_{SIN} reaches 0.5 V, the amplitude of V_{SIN} is increased gradually in every cycle of V_{SUP_SEN}. When V_{SIN} exceeds 0.5 V, the current DAC maintains its amplitude by holding the output of the counter. If the peak of V_{SIN} decreases below 0.5 V due to V_{AC} variation, the DAC starts to increase the amplitude again until the peak of V_{SIN} reaches 0.5 V. If the peak of V_{SIN} exceeds 0.53 V due to V_{AC} variation, the DAC starts to decrease the

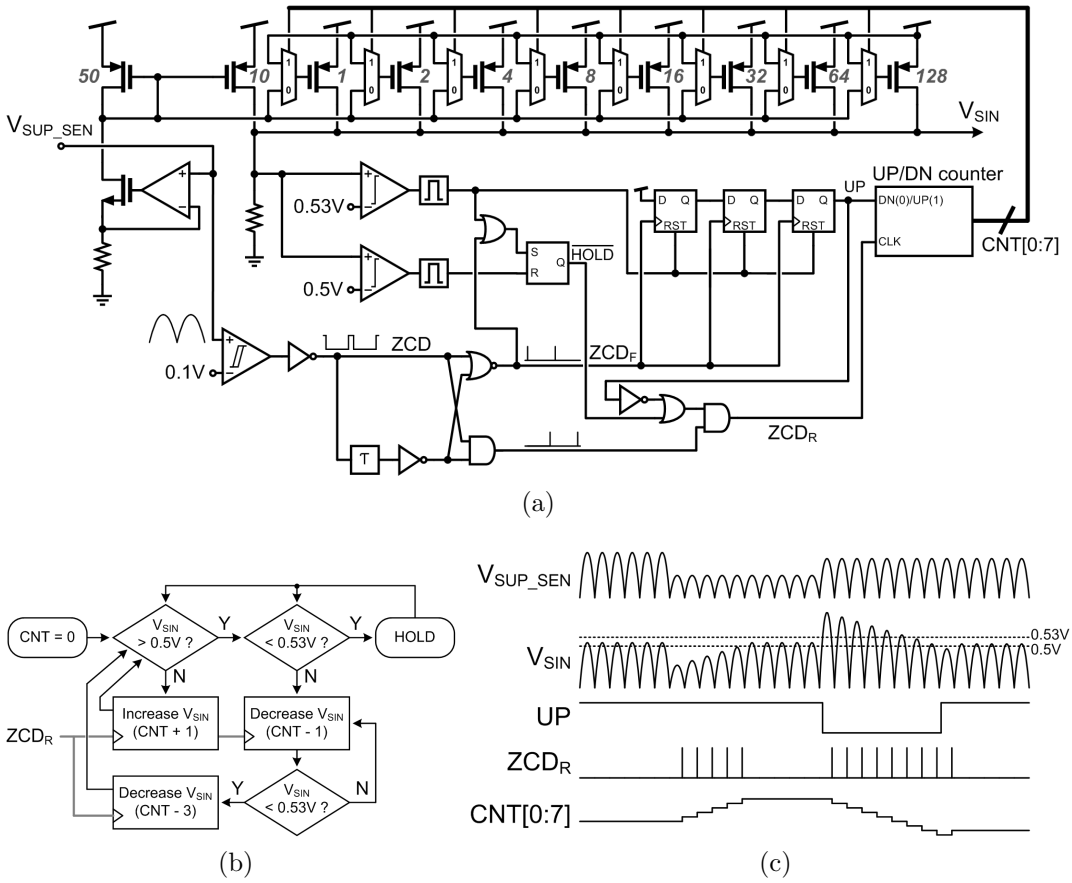


Figure 4.5: Constant-peak controller. (a) Block diagram. (b) Flow chart. (c) Timing diagram.

amplitude of V_{SIN}. Once V_{SIN} crosses 0.53 V, the DAC decreases the level by three additional bits, which ensures that the peak of V_{SIN} is located around 0.5 V. Therefore, V_{SIN} can be expressed as $V_{PEAK}\times|\sin(\phi)|$ where V_{PEAK} is set to 0.5 V by the design.

4.3.3 Reference Generator

To obtain the desired reference signal that has to be form of $\alpha \times |\sin(\phi)| + (1-\alpha) \times \sin^2(\phi)$ $(0 \leq \alpha \leq 1)$, a SIN^2 generator and a weighted adder based on a current mirror are proposed. The ${V_{SIN}}^2$ reference that has a constant peak of V_{PEAK} and provides a $\sin^2(\phi)$ shape is obtained by using a switching multiplier as depicted in Fig. 4.6. The reference V_{SIN} ($=V_{PEAK}\times|\sin(\phi)|$), which has a constant peak amplitude (V_{PEAK}) set by the constant peak controller, is applied to the SIN^2 generator. V_{SIN} is switched using a PWM signal which has a duty-cycle that is controlled by comparing V_{SIN} and a RAMP signal. The RAMP signal has the same peak amplitude, V_{PEAK}, that is generated by the oscillator. Therefore, the duty-cycle can be represented V_{SIN}/V_{PEAK}. After low-pass filtering, the PWM output of switching multiplier, is thus given by $V_{SIN}\times V_{SIN}/V_{PEAK}$, that is $V_{PEAK}\times\sin^2(\phi)$. The ripple voltage on the output is removed by employing a sample-and-hold circuit.

A weighted adder is used to combine V_{SIN} and ${V_{SIN}}^2$ terms that have same peak amplitude but provide $\sin(\phi)$ and $\sin^2(\phi)$, respectively, by using a 3-bit reference control signal (S) as shown in Fig. 4.7. The V_{SIN} and ${V_{SIN}}^2$

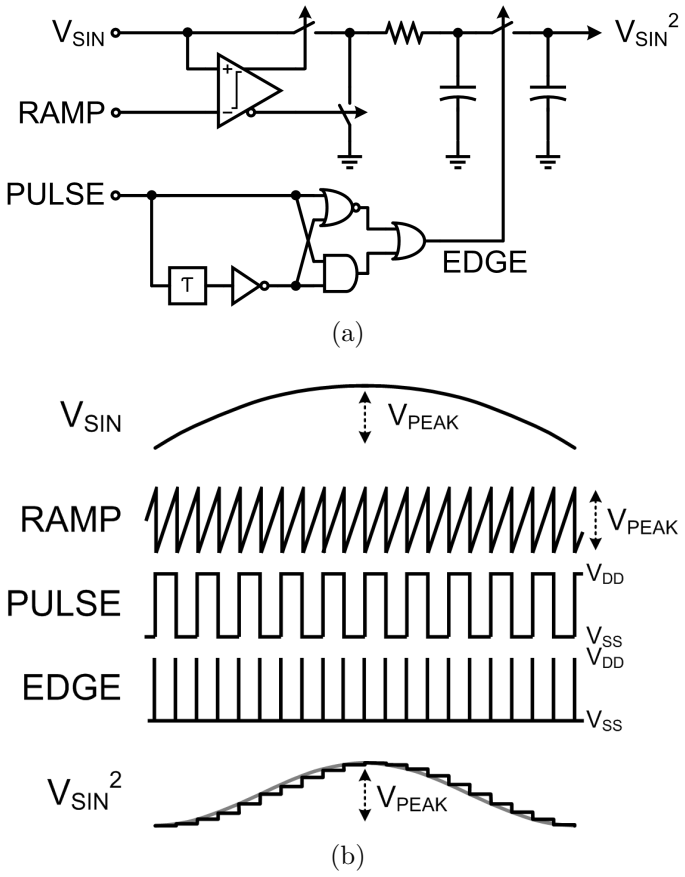


Figure 4.6: SIN^2 generator. (a) Block diagram. (b) Timing diagram.

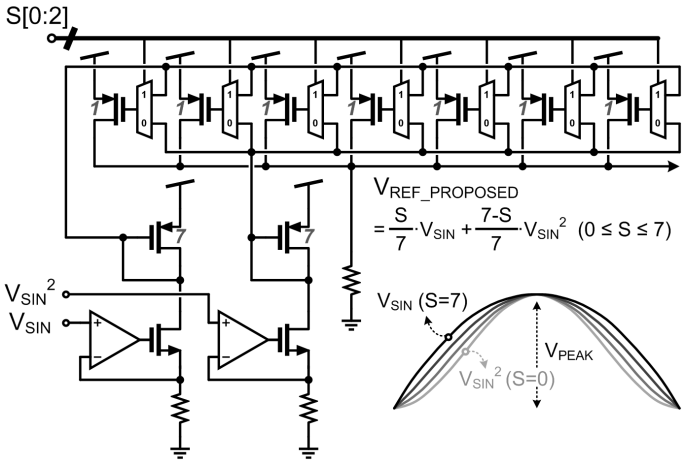


Figure 4.7: Weighted adder.

references are converted to current information and applied to the current weighted adder. The reference control signal, S, can be controlled externally. By changing the current mirror ratio of V_{SIN} and ${V_{SIN}}^2$ through S, the proposed reference signal ($V_{REF\_PROPOSED}$) can be represented as,

$$V_{REF\_PROPOSED} = \frac{S}{7} \times V_{SIN} + \frac{(7-S)}{7} \times {V_{SIN}}^2 \tag{4.6}$$

where, S can vary from 0 to 7. For S=7, $V_{REF\_PROPOSED}$ equals V_{SIN}, which is same as the reference signal used in prior implementations [48, 49, 50].

4.4 Measurement Results

The above design has been implemented in a 130-nm CMOS process (Fig. 4.8). A 400-V N-channel power MOSFET and a 400-V diode are used for the switches. A supply voltage of 5.5 V is applied to the driver externally. A

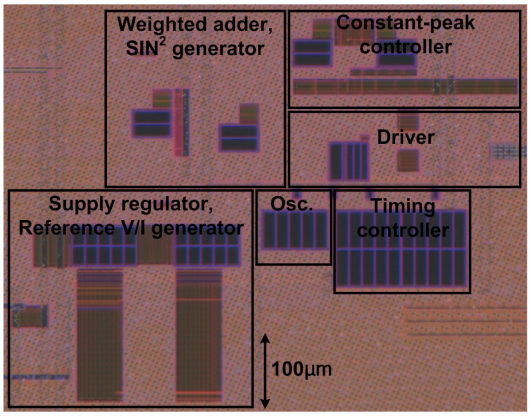
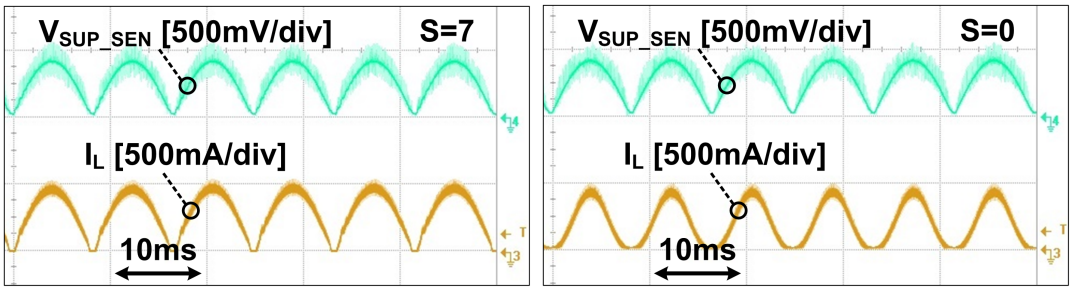


Figure 4.8: Chip photograph.

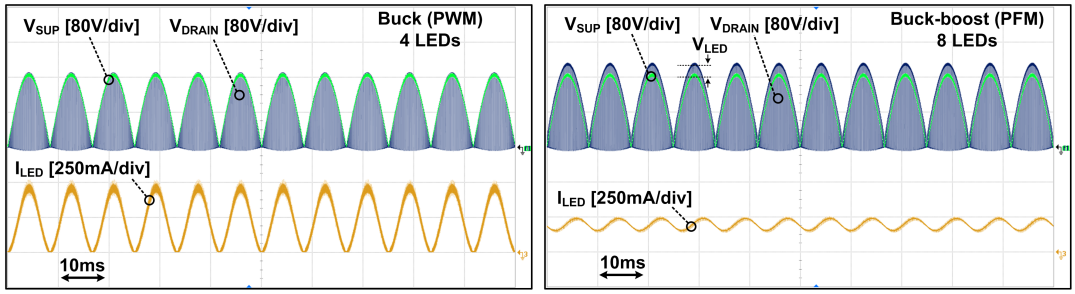
4.7 mH inductor is employed in the converter. The reference control signal (S) can be controlled externally. The driver can be configured as a buck converter as well as a buck-boost converter. A 22 nF ceramic capacitor and a 330 µF aluminum capacitor are used across the LED output in the buck converter and the buck-boost converter, respectively. The buck-boost converter requires a large output capacitor since the output of the buck-boost converter switches in every cycle, while the output of the buck converter does not. The operating mode can be changed between PWM and PFM (Table 4.2). The PWM mode is used in the buck converter and the PFM mode is used in the buck and buck-boost converters.

To verify the operation of the proposed reference signal, the inductor current is measured, since it is proportional to the shape of the reference signal. Fig. 4.9 shows the measured V_{SUP_SEN} and the inductor current. V_{SUP_SEN} follows the shape of rectified sinusoidal because it is directly sensed from the



(a) (b)

Figure 4.9: Measured waveform of V_{SUP_SEN} and inductor current I_L. (a) S=7. (b) S=0.

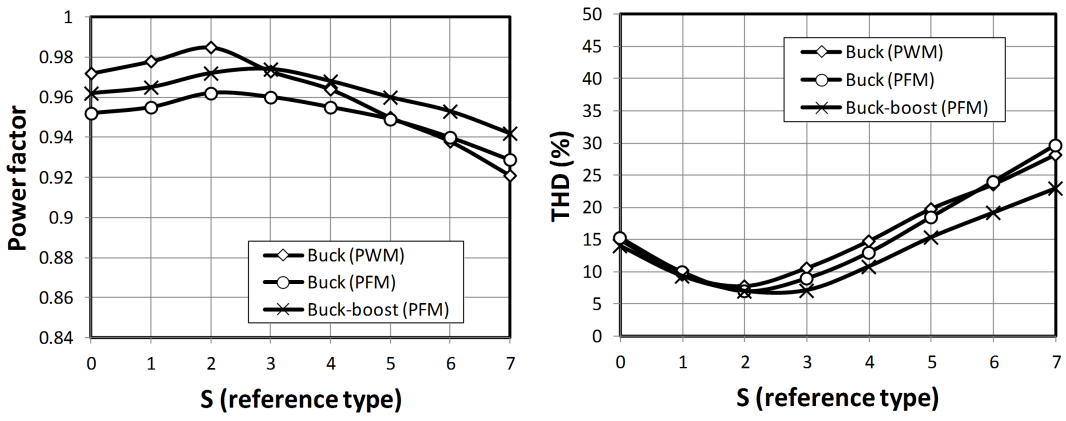


(a) (b)

Figure 4.10: Measured waveforms. (a) Buck converter (PWM). (b) Buck-boost converter (PFM).

rectified AC input. I_L follows the $|\sin(\phi)|$ form when S=7 and follows the $\sin^2(\phi)$ form for S=0. The shape of I_L can be varied between $|\sin(\phi)|$ and $\sin^2(\phi)$ by changing S.

Fig. 4.10 shows the measured waveform of the buck converter in the PWM mode, and the buck-boost converter in the PFM mode. The drain voltage switches between $V_{SUP} + V_D$ and GND in the buck converter while it switches between $V_{SUP} + V_{LED} + V_D$ and GND in the buck-boost converter. V_D



(a) (b)

Figure 4.11: Measured PF and THD vs. different types of reference signal with 4 LEDs.

is the forward-bias voltage of the power diode switch. The LED current (I_{LED}) is averaged in the buck-boost converter because a large output capacitor is used to low-pass filter the switching output voltage in this mode.

Fig. 4.11 shows the measured PF and THD for various settings of S. The measurement employs 4 LEDs. In a buck converter (PWM and PFM), the highest PF and lowest THD are achieved when S=2 rather than S=0, because, as stated above, V_{LED} is not purely a DC level, but instead depends on the current flow through the LED. Thus V_{LED} has a small $|\sin(\phi)|$ component, which causes the best performance to be observed for S=2. In a buck-boost converter, S=3 shows the best performance because the desired I_L of the buck-boost design already contains the $|\sin(\phi)|$ term.

To verify the operation of the constant peak reference controller, the

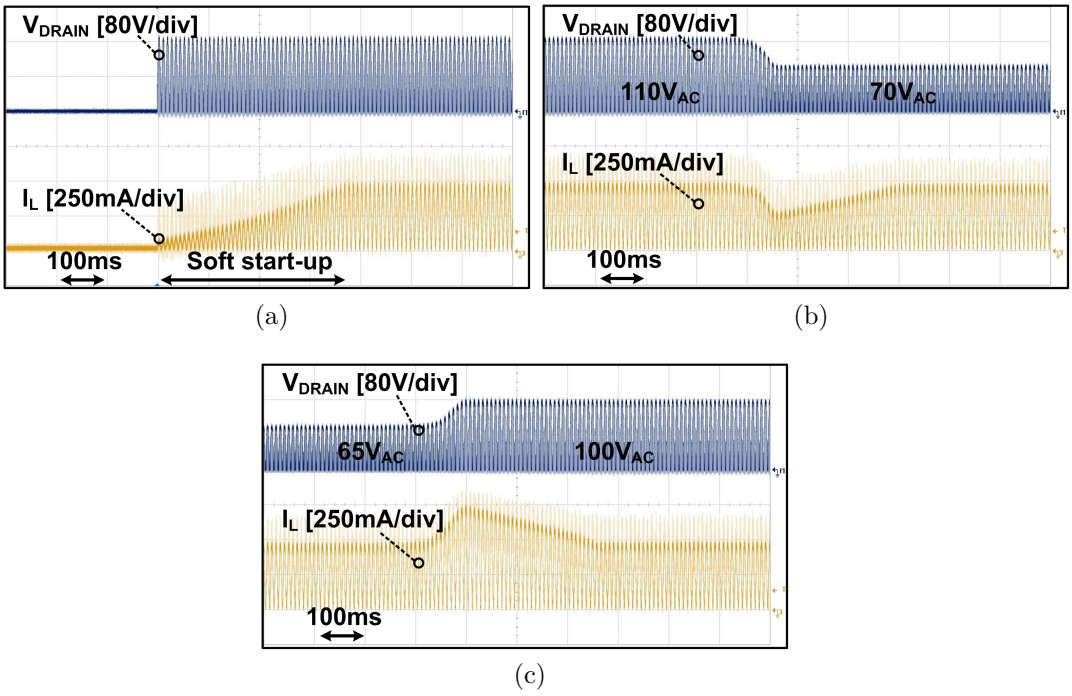


Figure 4.12: Measured waveform of drain voltage (V_{DRAIN}) and inductor current (I_L) in the buck converter (PWM). (a) Soft start-up. (b) AC line voltage transition from $110V_{AC}$ to $70V_{AC}$. (c) AC line voltage transition from $65V_{AC}$ to $100V_{AC}$.

drain voltage of M_{SW}, and I_L are measured (Fig. 4.12). When V_{AC} is applied, I_L starts to increase gradually through a soft start-up function, and maintains a constant peak current of 0.5 A. I_L is observed with an abruptly varying V_{AC}. Even if V_{AC} varies, I_L is observed to maintain a constant peak current level, due to the use of the proposed constant-peak controller.

Fig. 4.13 shows the LED current (I_{LED}) as V_{AC} is varied from 80 V_{RMS} to 140 V_{RMS}. I_{LED} of the buck converter (PWM, PFM) deviates by ±5% due to V_{AC} variation regardless of number of LEDs, except for the case of 16 LEDs at low V_{AC} in the buck converter (PWM). A large number of LEDs cannot be driven properly with low V_{AC}, because the duty-cycle is limited to 50% in the buck converter (PWM). I_{LED} of the buck-boost converter increases almost linearly with V_{AC}, because the output load current of the buck-boost design is (1-D)×I_L, where the duty-cycle (D) decreases as V_{AC} is increased.

PF and THD are measured by varying the number of LEDs from 2 to 16. Two different types of references are used to compare the performance with the proposed reference and the conventional reference (S=7; V_{SIN}) (Fig. 4.14). S=2 is used in the buck converter regardless of the number of LEDs, while S=3/4/5 are used for the buck-boost converter for 2-8/10-14/16 LEDs because the desired form of the inductor current has to be changed as a function of the the number of LEDs as explained in Section 4.2.2. PF and THD are both observed to improve when the proposed reference is employed. The peak PF and lowest THD are 0.995/0.983/0.996 and 7.8/6.2/3.5% for buck (PWM), buck (PFM), buck-boost (PFM) cases, respectively. Since the buck converter

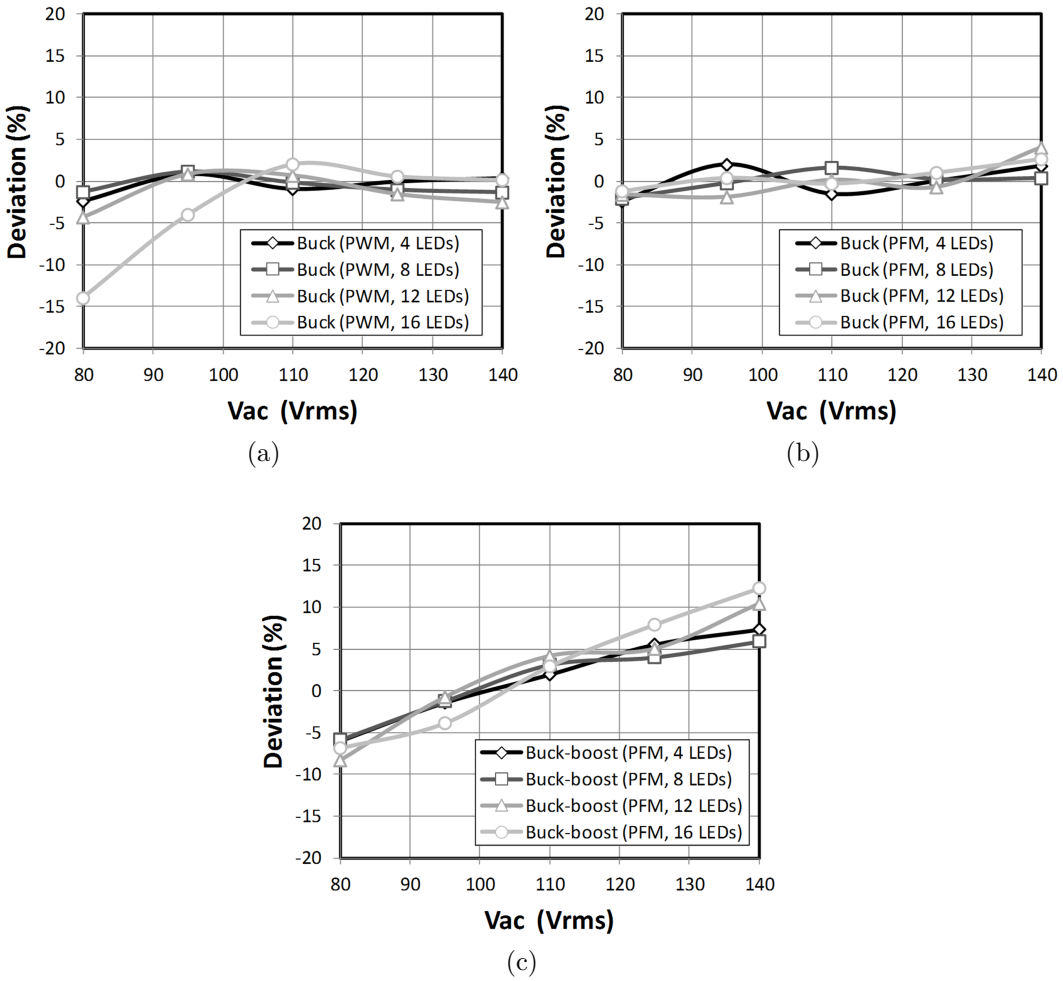
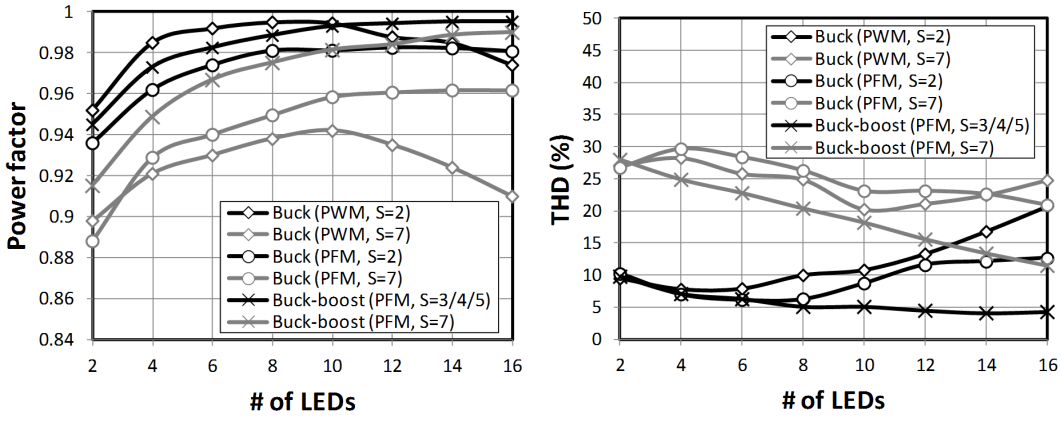


Figure 4.13: Measured LED current vs. AC voltage variation. (a) Buck converter (PWM). (b) Buck converter (PFM). (c) Buck-boost converter (PFM).

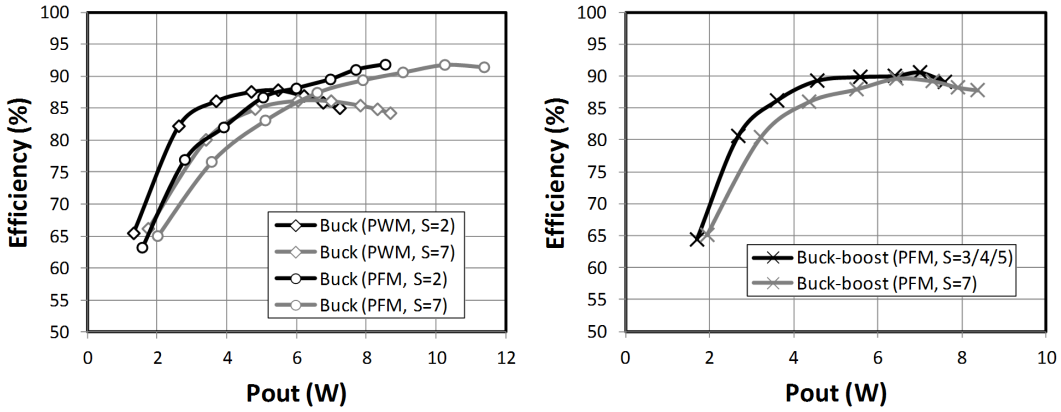


(a) (b)

Figure 4.14: Measurement results for different number of LEDs. (a) Power factor. (b) THD.

only allows step-down conversion, the PF and THD are degraded when the number of LEDs is increased, especially in the PWM mode, due to the limited maximum duty-cycle. In the buck-boost converter, PF and THD are improved significantly when the number of LEDs is small because the shape of the desired inductor current is close to ${V_{SIN}}^2$.

Fig. 4.15 shows the measured efficiency for different numbers of LEDs. The efficiency is improved for a given P_{OUT} with the proposed reference by using a larger V_{LED} with more LEDs. I_L in the proposed reference has a narrower shape, which leads to lower I_{LED} than the conventional case. P_{OUT} in the proposed case can also be made higher by using a higher reference peak level for a given number of LEDs. The PWM mode has a higher efficiency than the PFM mode at the same P_{OUT} due to reduced switching. The peak efficiency is 88/92/91% for the buck with PWM, buck with PFM and buck-boost (PFM)



(a) (b)

Figure 4.15: Measured efficiency for different number of LEDs. (a) Buck converter. (b) Buck-boost converter.

cases, respectively, which includes the driver current consumption of 280 µA with PWM and 330 µA with PFM. Table 4.3 summarizes the performance using conventional as well as proposed references and provides a comparison with prior work.

4.5 Conclusion

An efficient buck/buck-boost reconfigurable LED driver that supports PWM and PFM operation is demonstrated. Rectified sin as well as $\sin^2$ functions are employed in the reference signal to improve the PF and THD of the buck and buck-boost converters. The design ensures that the peak of the inductor current maintains a constant level that is invariant for different AC line voltages. The peak PF and lowest THD are 0.995/0.983/0.996 and 7.8/6.2/3.5% for buck (PWM), buck (PFM), buck-boost (PFM) cases, respec-

	ISSCC 2011 Hwang	ISSCC 2013 Bandyopadhyay	JSSC 2012* Hwang	This Work					
Topology	Non-isolated Buck	Quasi-resonant Non-isolated Buck	Flyback	Non-isolated Buck				Non-isolated Buck-boost	
Control	PWM	Burst mode	CRM	PWM		PFM		PFM	
				S=7 **Conventional**	S=2 **Proposed**	S=7 **Conventional**	S=2 **Proposed**	S=7 **Conventional**	S=3/4/5 **Proposed**
# of LEDs	5-16	20	5-11	2-16					
Output power	2.5-7 W	7-22 W	6-10.5W	1.8-8.7 W	1.3-7.3 W	2-11.4 W	1.6-8.6 W	1.9-8.4W	1.7-7.6 W
PF	0.96-0.98 ($110V_{AC}$) 0.82-0.95 ($220V_{AC}$)	0.78-0.95 ($110V_{AC}$)	0.895-0.935 ($220V_{AC}$)	0.9-0.94 ($110V_{AC}$)	0.95-0.995 ($110V_{AC}$)	0.94-0.962 ($110V_{AC}$)	0.89-0.983 ($110V_{AC}$)	0.95-0.992 ($110V_{AC}$)	0.92-0.996 ($110V_{AC}$)
Lowest THD	19 % ($110V_{AC}$) 14 % ($220V_{AC}$)	N/A	N/A	20.2 % ($110V_{AC}$)	7.8% ($110V_{AC}$)	21 % ($110V_{AC}$)	6.2 % ($110V_{AC}$)	8.2 % ($110V_{AC}$)	3.5% ($110V_{AC}$)
Peak efficiency	88 %	89.4 %	85 %	86.2 %	87.8 %	91.8 %	91.8 %	89.6 %	90.6 %
* The performance is shown the case of TYPE 1 in their paper that achieved the maximum efficiency condition.									

Table 4.3: Performance comparison.

tively. In addition, the peak efficiency is 88/92/91% for buck (PWM), buck (PFM), buck-boost (PFM) cases, respectively.

Chapter 5

Conclusion and Future Work

Energy efficient ICs for power delivery based on the use of PWM are investigated as part of this research, with switching frequencies in the range from several kHz to GHz. PWM architectures that enhance efficiency and avoid limitations of previously demonstrated techniques are described. The design in each frequency range is motivated by a suitable application.

A RF-PWM architecture that employs carrier switching is proposed for wireless transmitter applications. The transmitter is designed to switch between the carrier frequency and half of the carrier frequency, based on the signal amplitude, in order to alleviate the dynamic range limitation of PWM at RF that can be observed in classical RF-PWM implementations. In addition, a glitch-free phase selector is demonstrated that not only removes deleterious glitches at the input data transitions but also prevents D-FF setup-and-hold time violations. The proposed transmitter is demonstrated using a 20-MHz 64-QAM 802.11g modulated signal. Owing to the digitally-intensive approach, the design can further benefit in performance and area through the use of more advanced technologies.

As part of future work on this topic, the linearity can be further im-

proved by combining the approach with RF-DAC architectures. A hybrid design using RF-PWM with an RF-DAC can also be used for wide bandwidth transmitter applications. An RF-DAC with 11-14 bits is commonly used for wide bandwidth designs. However the effective resolution is typically lowered because of non-linearity of the DAC. By combining the RF-PWM concept in an RF-DAC architecture, the effective resolution can be improved and the transmitter can drive a wider bandwidth or reduce the output noise. The approach can also be combined with a class-G output to enhance efficiency. In the proposed architecture, back-off efficiency is improved by the half-carrier switching frequency operation. By adopting a class-G PA approach in the half carrier mode, the back-off efficiency can be enhanced even more. Further, linearity can also be improved by reducing the switching level at the lowest output power mode.

A high speed PWM driver with a multi-level class-D PA has been demonstrated for signals up to MHz bandwidth. Employing a PLL-based PWM architecture enables high switching frequency operation with high linearity. A multi-level output stage provides high peak- as well as back-off efficiency at high switching frequency by reducing the switching levels. Folded duty-cycle variation is proposed, which ensures seamless operation for a continuous input signal. In the differential implementation, 3-level operation can be implemented without the requirement for an additional supply source compared to 2-level operation. The proposed PWM driver operates from 40 MHz to 170 MHz and is demonstrated using a sinusoidal input as well as a high

PAPR modulation signal. Highly linear operation is achieved in 2-level as well as 3/5-level modes, that offer higher efficiency.

As part of future work, an autonomous mode control can be used to enhance the noise immunity at mode transitions. In the proposed architecture, the mode control between multiple levels is achieved by using a comparator for sensing the input voltage. However, sensing the duty-cycle to change the mode, if the duty-cycle is 0 or 100%, can eliminate noise sensitive mode control and achieve autonomous mode control. Further, noise performance can be improved by using an LC oscillator instead of a ring oscillator. Oscillator phase-noise is the dominant part of the total output noise, and determines the dynamic range of the output. Since an LC oscillator has better phase noise than a ring oscillator for a given power dissipation, it can be expected to improve the dynamic range of the design.

An efficient buck/buck-boost reconfigurable LED driver that supports PWM and PFM operation is demonstrated that switches at several kHz. Rectified sin as well as $\sin^2$ functions are employed in the reference signal to improve the PF and THD of buck and buck-boost converters. The design ensures that the peak of the inductor current maintains a constant level that is invariant for different AC line voltages. The proposed driver is demonstrated in buck converter (PWM, PFM) and buck-boost converter (PFM) configurations. The design operates with 80-140 Vac and can drive 2 to 16 LEDs.

As part of future work on the LED driver, the proposed reference can be employed not just in buck/buck-boost converters, but also in most step-down

or step-down-and-up converters for AC-to-DC conversion, with PF correction. For example, the proposed reference can be used in any flyback converter for AC-to-DC conversion. The architecture proposed here does not provide dimming control. This functionality can be included through the use of a TRIAC or by controlling the peak of the reference.

Appendix

Appendix A

Averaged Switch Model of Power Converters

In order to verify the architecture of a power converter topology, such as a buck or a buck-boost converter, and reduce the design time, a behaviorial simulation based on averaged switch model can be used. Different conditions such as the input voltage, the output load condition, the size of passive components and the shape of reference can be easily applied to prove the idea. This chapter presents an averaged switch model for power converters that are based on peak current control.

A.1 Buck Converter

Fig. A.1 shows the circuit, and the inductor current of an LED driver that employs a buck converter. The buck converter is based on peak current-controlled PWM which controls the inductor current (i_L) by employing a current reference control (i_C) signal. The sensed inductor current is compared to the peak level of the current reference signal and controls the duty-cycle (D) of the converter. The inductor current follows the shape of the current reference with certain amount of ripple.

The averaged switch model of the buck converter can be described by

the equations below,

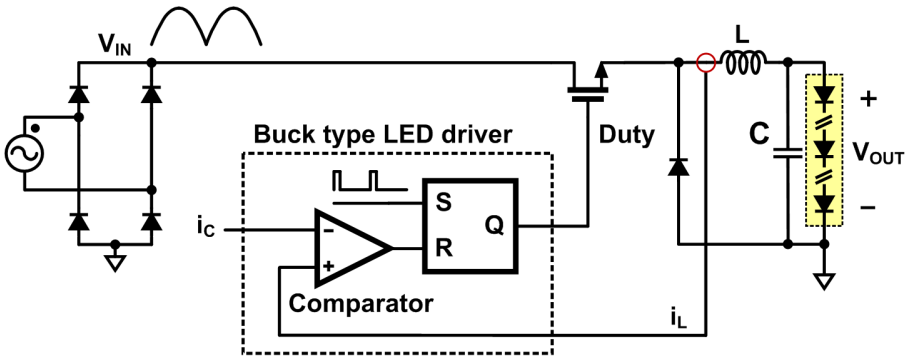
$$L\frac{di_L}{dt} = D \cdot V_{IN} - V_{OUT} \tag{A.1}$$
$$C\frac{dV_{OUT}}{dt} = i_L - I_{OUT}$$

where V_{IN} is the input voltage, V_{OUT} is the output voltage which is the forward voltage of LEDs, C is the output capacitor, and I_{OUT} is the output LED current.

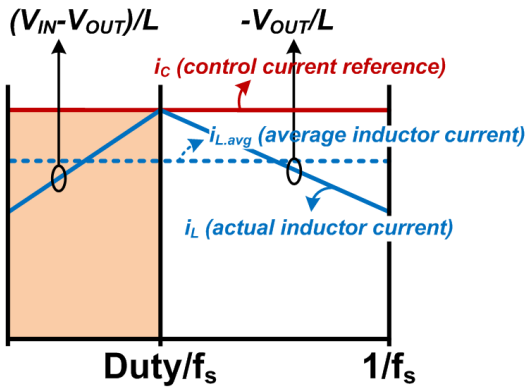
In the averaged switch model, the duty-cycle for the peak current-controlled PWM method is calculated based on the current reference, the average inductor current, the input voltage, and the output voltage as shown in Fig. A.1b, and can be shown to be given by

$$D = \frac{(i_C - i_L) \cdot L \cdot 2f_S}{V_{IN} - V_{OUT}} \tag{A.2}$$

where f_S is the switching frequency. The input current (I_{IN}) flows only when the switch is in the ON-state, and hence depends on the duty-cycle. The output LED current (I_{OUT}) is equal to the inductor current in a buck converter. Therefore, the input current and the output current can be expressed as,



(a)



(b)

Figure A.1: LED driver using a buck converter. (a) Circuit. (b) Average model of duty-cycle.

$$I_{IN} = D \cdot i_L \tag{A.3}$$

$$I_{OUT} = i_L$$

A.2 Buck-Boost Converter

Fig. A.2 shows the circuit and the inductor current of a LED driver that uses a buck-boost converter. Tha averaged switch model of a buck-boost converter can be described by the equations below,

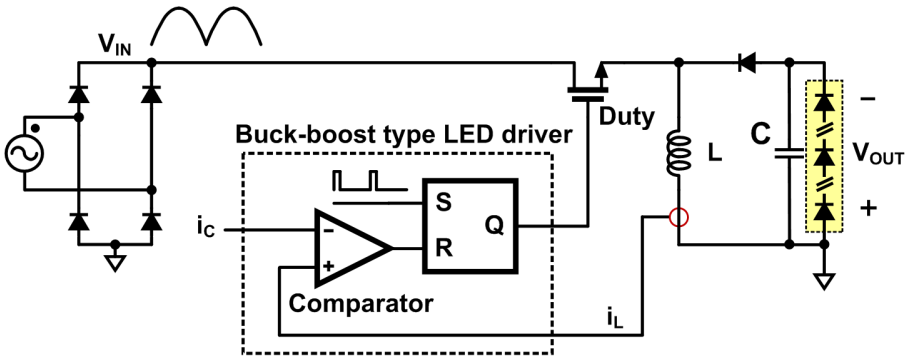
$$L\frac{di_L}{dt} = D \cdot V_{IN} - D' \cdot V_{OUT} \tag{A.4}$$

$$C\frac{dV_{OUT}}{dt} = D' \cdot i_L - I_{OUT}$$

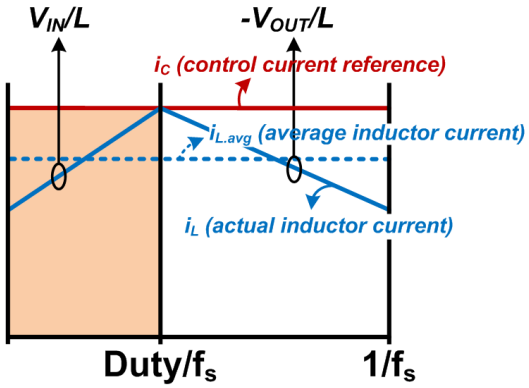
where D' = 1-D. The duty-cycle equation that describes the peak current control is modified compared to a buck converter because the rising slope of the inductor current in the buck-boost converter is $\frac{V_{IN}}{L}$ instead of $\frac{V_{IN} - V_{OUT}}{L}$. It can be calculated as shown below,

$$D = \frac{(i_C - i_L) \cdot L \cdot 2f_S}{V_{IN}} \tag{A.5}$$

In a buck-boost converter, when the switch is ON, the inductor is connected to the input and when it is OFF, the inductor is connected to the



(a)



(b)

Figure A.2: LED driver using a buck-boost converter. (a) Circuit. (b) Average model of duty-cycle.

output. Therefore, both the input and the output currents depend on the duty-cycle and can be expressed as

$$I_{IN} = D \cdot i_L \tag{A.6}$$
$$I_{OUT} = (1 - D) \cdot i_L$$

A.3 Boost Converter

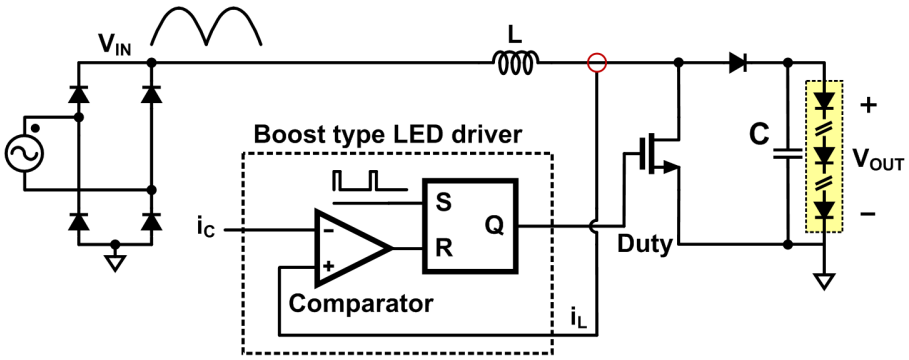
Fig. A.3 shows the circuit and inductor current of a LED driver that uses a boost converter. The averaged switch model of a buck-boost converter can be described by the equations below,

$$L\frac{di_L}{dt} = V - D' \cdot V_{OUT} \tag{A.7}$$
$$C\frac{dV_{OUT}}{dt} = D' \cdot i_L - I_{OUT}$$

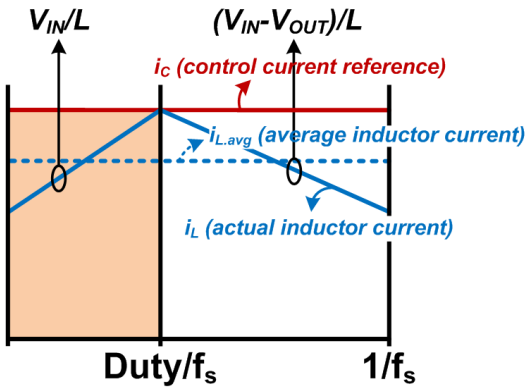
The equation for determining the duty-cycle is the same as a buck-boost converter since the rising slope of the inductor current is identical in the two cases. It can be shown to be given by,

$$D = \frac{(i_C - i_L) \cdot L \cdot 2f_S}{V_{IN}} \tag{A.8}$$

In a boost converter, the input current is the same as the inductor



(a)



(b)

Figure A.3: LED driver using boost converter. (a) Circuit. (b) Average model of duty-cycle.

current since the inductor is always connected to the input. The output current depends on the duty-cycle because the inductor is connected to the output when the switch is OFF. Therefore, the input current and the output current can be expressed as,

$$I_{IN} = i_L \tag{A.9}$$

$$I_{OUT} = (1 - D) \cdot i_L$$

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Vita

Kunhee Cho received the B.S. and the M.S. degree from Yonsei university, Seoul, South Korea, in 2007 and 2009, respectively. He joined the graduate program in electrical and computer engineering at the University of Texas at Austin in 2012. Since then he has been working towards his Ph.D., specializing in the field of analog and mixed-signal integrated circuit design.

From 2009 to 2012, he was with Fairchild Semiconductor, Bucheon, South Korea, where he designed power management ICs. He held research intern position at Texas Instruments, Dallas, TX, USA, in 2015, and 2016. He was the recipient of the Texas Instruments Outstanding Student Design Award in 2013.

Email address: khcho128@gmail.com

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