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Noise Shaping Asynchronous SAR ADC based Time to Digital Converter

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Noise Shaping Asynchronous SAR ADC based Time to Digital Converter

by

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by

Sowmya Katragadda, MSE

The University of Texas at Austin, 2016

SUPERVISOR: Nan Sun

Time-to-digital converters (TDCs) are key elements for the digitization of timing information in modern mixed-signal circuits such as digital PLLs, DLLs, ADCs**,** and on-chip jitter-monitoring circuits. Especially, high-resolution TDCs are increasingly employed in on-chip timing tests, such as jitter and clock skew measurements, as advanced fabrication technologies allow fine on-chip time resolutions. Its main purpose is to quantize the time interval of a pulse signal or the time interval between the rising edges of two clock signals. Similarly to ADCs, the performance of TDCs are also primarily characterized by Resolution, Sampling Rate, FOM, SNDR, Dynamic Range and DNL/INL.

This work proposes and demonstrates 2nd order noise shaping Asynchronous SAR ADC based TDC architecture with highest resolution of 0.25 ps among current state of art designs with respect to post-layout simulation results. This circuit is a combination of low power/High Resolution 2nd Order Noise Shaped Asynchronous SAR ADC backend with simple Time to Amplitude converter (TAC) front-end and is implemented in 40nm CMOS technology. Additionally, special emphasis is given on the discussion on various current state of art TDC architectures.

Table of Contents

List of Tables

List of Figures

Chapter 1: Time to Digital Converters

1.1 Introduction

Traditionally, time-to-digital converters (TDCs) have mostly been used in digital storage oscilloscopes, logic analyzers, high-energy particle physics and positron emission tomography (PET) [1,2] applications as a time interval measurement device which converts input time interval into a digital output code. Recently however, TDCs have become increasingly more important with the advent of digitally assisted analog and mixed-signal circuits such as Digital PLL/DLLs [3–11] and time-domain Analog-to-Digital Converters (ADCs) [12–16]. In these applications, TDCs are used as a phase detector or a quantizer with respect to time, and serves as a core block that determines the overall performance. Therefore, in order to achieve high performance mixed-signal circuits, a high-resolution and high-speed TDC is required.

1.2 Background & Motivation

Recently, high-resolution TDCs have gained in popularity due to their increasing implementation in digital PLLs, ADCs, jitter measurement, oscilloscopes and time-of-flight measurement units. In this report, a low resolution TDC is designed in the context of digital PLLs which are briefly discussed in this section.

A phase-locked loop (PLL) is widely used in communication systems. It can be used for clock generation, clock recovery from data signals, clock distribution and also as a frequency synthesizer. PLLs can be broadly classified into three types – Analog PLL, Digital PLL and All Digital PLL (ADPLL).

Traditionally, majority of analog PLLs are based on the charge-pump PLL topology. As shown in Fig. 1.1, the output clock of the voltage controlled oscillator (VCO) is divided by integer N or fractional N. The divided clock is compared with reference clock. The phase error (the time difference) between the edges of the two clocks will be detected by the Phase/Frequency Detector (PFD) and it will generate either an UP or a Down (DN) pulse proportional to the detected time difference. That UP or DN pulse will control the on/off of current source I_1 and I_2. In the loop filter, current flow will be converted to a VCO tuning voltage which will control the frequency of F_{out} and thus closing the loop. The frequency of F_{out} shall be Multiplication Factor (MF) times the frequency of F_{ref} when the loop is stable and settled. Since decades of research, different types and orders of analog PLLs have been analyzed and procedures for their design have been developed [17]. Second-order analog PLLs have also been analyzed and implemented by Hein and Scott [18] and Gardner [19]. But all analog PLLs suffer from limitations of analog loop filter such as large output resistance & mismatch (between up –down current sources) of charge pump, leaky and large area capacitors and additionally complexity of VCO design.

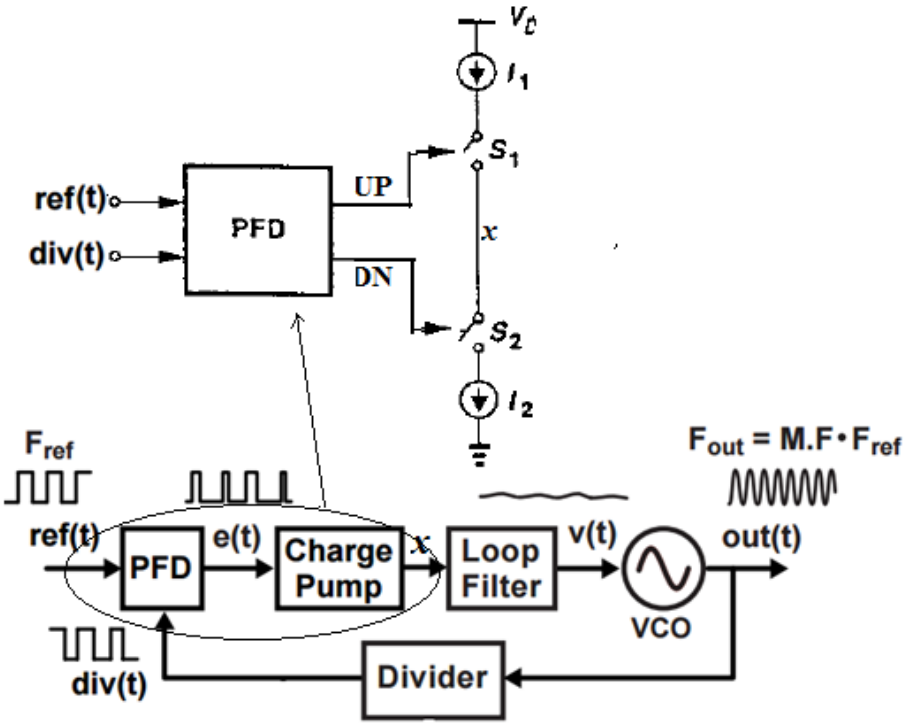


Figure 1.1: Architecture of Analog PLLs [47]

Past several years has seen proliferation of digital phase-locked loops (DPLL) for RF and high-performance frequency synthesis due to their clear benefits of flexibility, reconfigurability, transfer function precision, settling speed, frequency modulation capability, eliminating the noise-susceptible analog control for a VCO, the inherent noise immunity of digital circuits and amenability to integration with digital baseband and application processors [20-22]. When implemented in nanoscale CMOS, the DPLL also exhibits advantages of better performance, lower power consumption, lower area and cost over the traditional analog intensive charge-pump PLL.

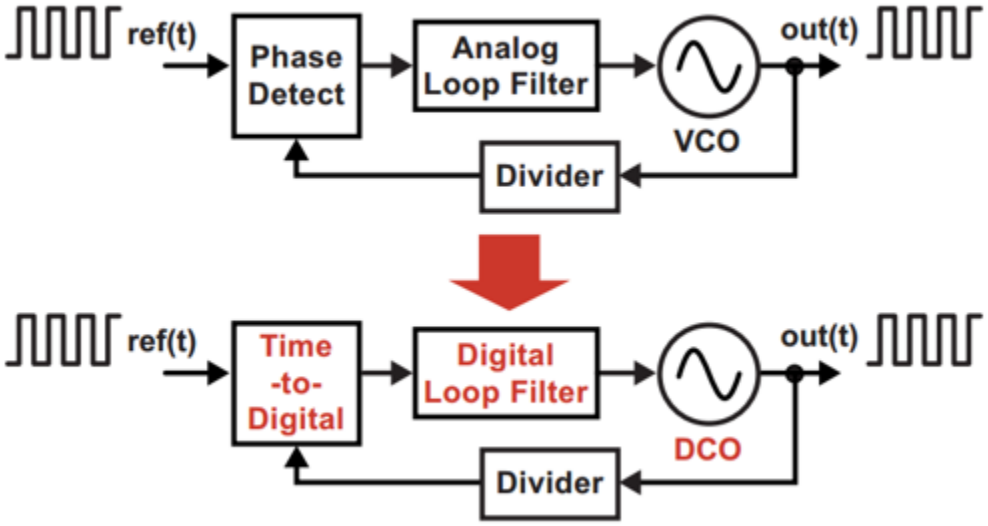


Figure 1.2: Architecture of Digital PLLs [23,47]

As shown in the Fig. 1.2, a digital filter is used in place of a traditional RC loop analog filter, which has the benefits of removing the need for large loop filter capacitance and analog components such as charge pumps. However, there is now a need of TDC to achieve digital encoding of the phase error between reference and divider output, and a digitally-controlled oscillator (DCO) to allow interfacing to the digital loop filter. While there has been much progress on achieving high performance DCO circuits, the development of high performance TDC circuits is currently an active research topic in the mixed-signal circuit community. Resolution, linearity, and conversion range of TDC have been major factors limiting the performance of fractional-N synthesizer DPLL.

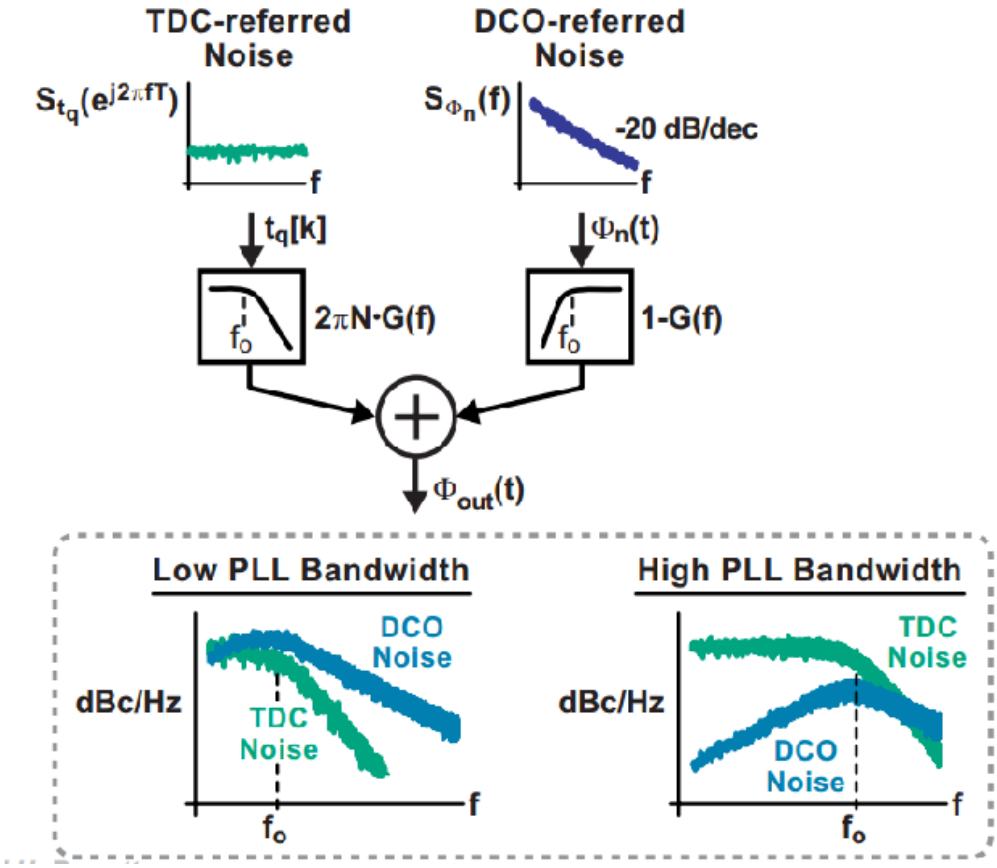
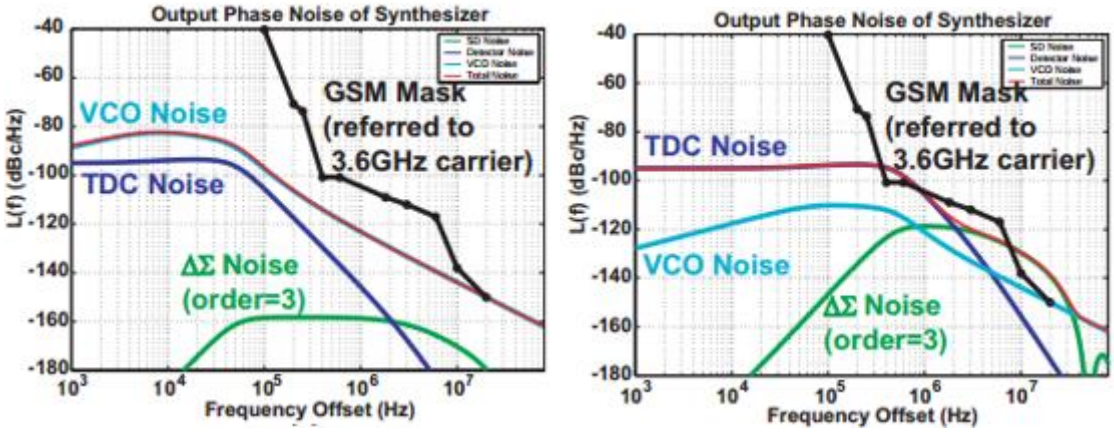


Figure 1.3: Analysis of Nosie Sources – DPLL [23]

The three noise sources for digital PLLs are contributed from TDC $t_q[k]$ (Quantization noise) which is low pass filtered with a DC gain of 2πn and cutoff frequency f_o- PLL Bandwidth in Fig. 1.3, DCO's phase noise which is high-pass filtered with a DC gain of 1 and lastly Δ–Σ noise from Fractional N (Δ–Σ modulators of fractional N divider or integer N dividers) [23]. The dominating noise sources that affect the performance are from DCO and TDC based on the bandwidth of the PLL as in Fig. 1.3. As shown in Fig. 1.4(a), when the PLL bandwidth is narrow, the noise associated with the third-order ΔΣ modulator and TDC is so low that its impact on the performance of synthesizer is insignificant. For high performance applications like GSM which necessitates high bandwidth PLL at system level, TDC quantization noise is dominating evident from the phase noise of frequency synthesizer. As illustrated in Fig. 1.4(b), both the TDC and divider quantization noises

cannot meet the GSM-level requirement. The GSM level requirement can be met by high resolution TDCs.



(a) (b)

Figure 1.4: Output Phase noise of Synthesizer (a) Low Bandwidth (b) High bandwidth [23]

At the DPLL output, the power spectral density contributed by the TDC quantization noise within the PLL bandwidth can be expressed as

$$S_{TDC} = \frac{(2\pi)^2}{12}\left(\frac{\Delta t_{del}}{T_{DCO}}\right)^2 \frac{1}{f_{REF}}$$

Where Δt_{del} denotes the quantization time error of the TDC, T_{DCO} is the period of the DCO oscillation, and f_{REF} is the frequency of the reference clock [24]. Obviously, a higher resolution TDC results in a lower in-band PLL noise and thus low jitter DPLLs. This defines one of the prime motivations for pushing towards low resolution and high linearity TDCs.

1.3 Performance Characterization of TDC

Functionally, TDCs are very similar to ADCs except that instead of quantizing continuous voltages, these designs are used to quantize continuous time intervals. Hence, all performance metrics characterizing the step function of ADCs (e.g., offset and gain error, differential and integral nonlinearity (DNL, INL)) can also be applied for TDC. The

smallest time interval that can be digitized in a TDC is the resolution of the TDC. The dynamic range of a TDC is the maximum time interval that can be measured without any saturation effects. The conversion time or the latency, respectively, describes how long it takes after a start or stop signal before the measurement result is available. The dead time is the minimum time between two successive time digitization operations before a new operation can be started.

The noise performance of a TDC is usually described by the single shot precision: If a constant time interval is measured repeatedly, the digital output values vary with a standard deviation that is called single shot precision. The area and power consumption of several TDCs can be compared by adopting the established ADC figures of merit, namely $FOM_P = \frac{P}{f_{conv}} 2^{ENOB}$ for the power and for the area $FOM_A = \frac{A}{f_{conv}} 2^{ENOB}$, P where is the power consumption, f_{conv} the conversion rate of TDC, A the area, and ENOB the effective number of bits. Further, the process of time digitization should be linear across the dynamic range of the operation. In RF frequency synthesizers, a high resolution, wide range TDC with zero dead-time is desired.

In the following sections, a comparative discussion among various TDC architectures is made with respect to these performance parameters. It can be observed from the following discussion that most of the TDC architectures resemble ADC architectures.

1.3.1 Modelling of TDC

The mathematical model of TDC [23] is shown in Fig. 1.5. Phase error is converted to time error by scale factor of T/2π. TDC introduces quantization error - $t_q[k]$ and its gain is set by average delay per step - Δt_{del}.

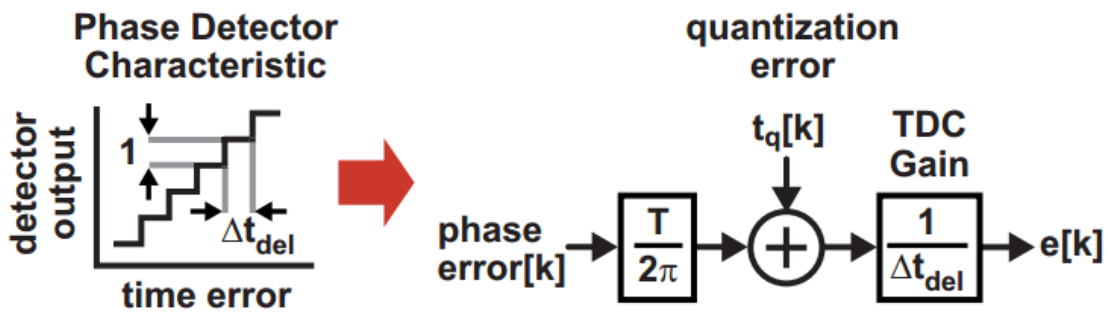


Figure 1.5: Mathematical modelling of TDC [23]

1.4 Comparative study of TDC architectures

Similar to ADCs, existing architectures of TDCs can be divided into several categories as discussed in detail below: Flash, Pipeline, Interpolation, Oversampling, Stochastic and Successive approximation Register (SAR) TDCs.

1.4.1 Vernier delay line based TDCs

TDCs research began with delay line based TDCs which counterparts to Flash ADCs. They use inverters or buffers to generate quantization level, as shown in Fig. 1.6(a). Although a delay-line TDC achieves the highest conversion rate among other TDCs, its time resolution is limited by the CMOS gate-delay. In order to achieve finer time resolution, Vernier structure [25] can be adopted which is shown in Fig. 1.6(b). The converter is realized starting from two delay lines formed by stages with a delay of τ_1 and τ_2 so that τ_1- τ_2 = Δ, where Δ is the TDC resolution. The two lines are connected to a series of flip-flops which stores a 1 or a 0 depending if the rising edge of the reference arrives before or after that of the signal in Fig. 1.6(b). Actually, the signal edge, which lags a reference edge by nΔ at the input of TDC, will be lined up with it after n stages producing a thermometric code at the flip-flop outputs in Fig. 1.6(b). In practice, such kind of TDC works as traditional flash ADC where the delay lines creates a set of time references like resistor/capacitive DAC and the flip-flops are used as time comparators.

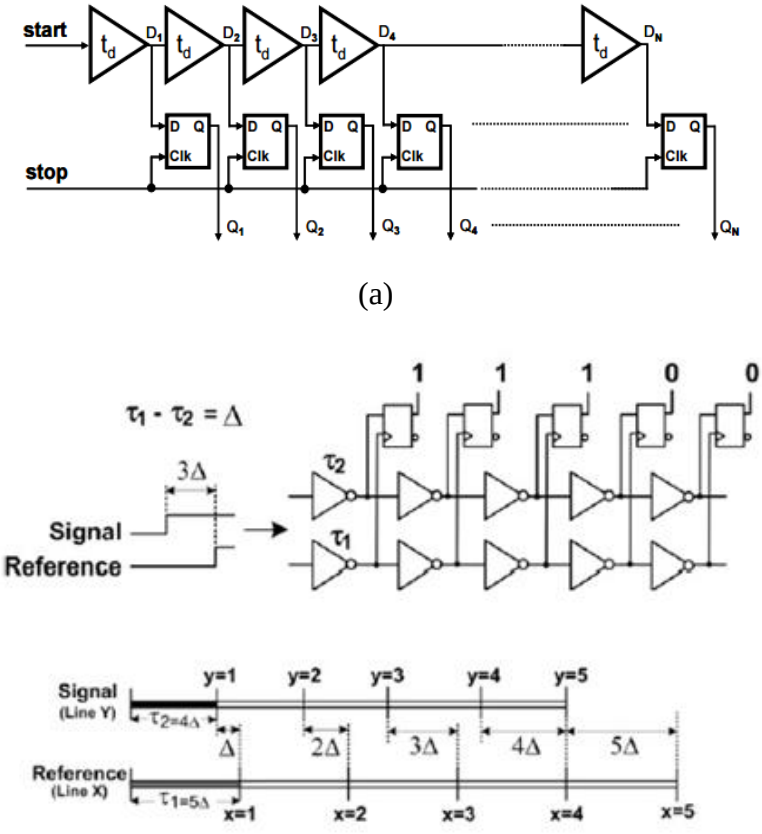


Figure 1.6: (a) Delay line based TDC (b) Classic Vernier Based TDC [25]

It can be observed that, the dynamic range ($t_{DR} = n(\tau_1 - \tau_2)$) is dependent on no of stages which results in large power and long conversion time. This can be resolved by architectures such as cyclic Vernier delay line [26] because the dynamic range was simply expanded by the extra counter bits. The resolution has been most limiting factor of this architecture, as it directly depends on the delay of the device which is in turn prone to mismatch and process variations. Hence, this architecture necessitates intensive calibration techniques and there by increases power and area.

Also the random variations of the delay elements, caused by the device mismatch, due to the process parameter variation, are a source of DNL. This is accumulative as the signal

propagates along the delay line. Additionally, the setup time and metastability rate of the sampling D flip-flops can cause errors in the time measurement in the same way comparator metastability limits least significant bit (LSB) resolution of a typical flash ADC architecture.

Several modified linear Vernier architectures proposed in literature try to increase resolution and/or reduce power consumption by interpolation techniques [27] or by exploiting the periodicity of the input signals. The high resolution of Vernier TDCs was also achieved by variants like 2D, 3D plane/cyclic vernier architectures [28- 30]. However in all cases, the number of stages grows exponentially with the number of bits which increases design/ calibration complexity and with it, the jitter noise and the sensitivity to mismatches increase, thereby limiting the linearity.

1.4.2 Pipeline TDCs

Resolution is improved by two-step coarse-fine TDCs. Initially, Pipeline TDC began with two-step TDCs as shown below with coarse stage implemented by single delay chain followed by Fine stage using Vernier delay chain [31]. This is followed by the two-step architecture in which, the input time signal is quantized by a coarse TDC and the residue which is amplified by a Time Amplifier (TA), is again quantized by a coarse TDC, as shown in Fig. 1.7 [32]. Due to the gain of the TA, the overall time resolution of TDC is increased. Also, as the coarse TDCs are usually made by delay-line TDCs, it achieves high conversion rate. The time-amplification scheme is implemented by metastability of D-Flip flop as shown in the Fig. 1.8. Metastability leads to progressively slower output transitions as setup time on latch is encroached upon. However, the downside of this scheme is that it suffers from uncertainties of gain due to nonlinearity and PVT variations.

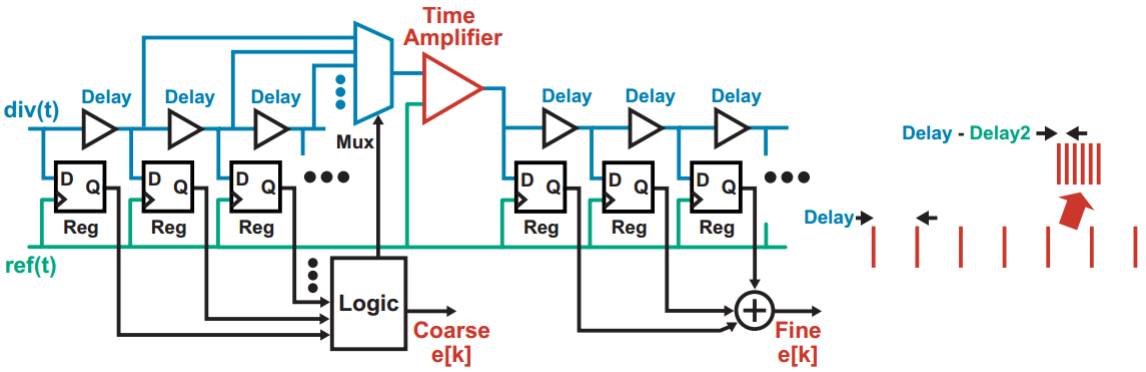


Figure 1.7: Two step TDC using time-amplification [23]

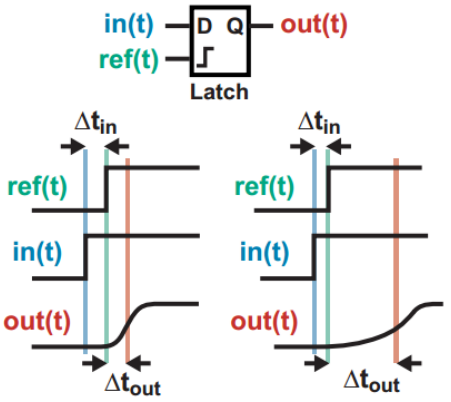


Figure 1.8: Implementation of Time amplification [23]

Although the range for these architectures is larger than what would be achieved for a single-step TDC using the same resolution improvement techniques, the fundamental range versus size tradeoff does not improve compared with the simple delay chain TDC discussed earlier. Pipeline TDCs are demonstrated with relatively high throughput of above 100 MS/s, but their resolutions exceed only few ps. Hence there has been a lot of progress in Pipeline TDCs pushing resolution, Dynamic range and linearity by implementing synchronous and asynchronous multi-step architectures using 1.5 – 2.5 bit MDACs (Multiplying Digital-to-Analog Converters) [33-34] as shown in the Fig. 1.9. In Fig. 1.9(a), synchronous pipeline TDC consists of three 2.5 bit MDAC stages, Time register for

storage, time amplifier and calibration circuits. In Fig. 1.9(b), Asynchronous pipelined TDC consists of ten 1.5-bit time-domain MDAC stages, a time amplifier, gain calibration block, a pseudo random bits generator (PRBG), and a backend digital background calibration block for residue error correction in seven MSB stages.

These circuits necessitate time amplifiers and time registers for storage which also increase overall design complexity. Though these architectures can achieve low resolution, they tend to be very power-hungry, area intensive and require additional calibration circuitries due to the inaccuracy and PVT vulnerability of the time amplifier or time register.

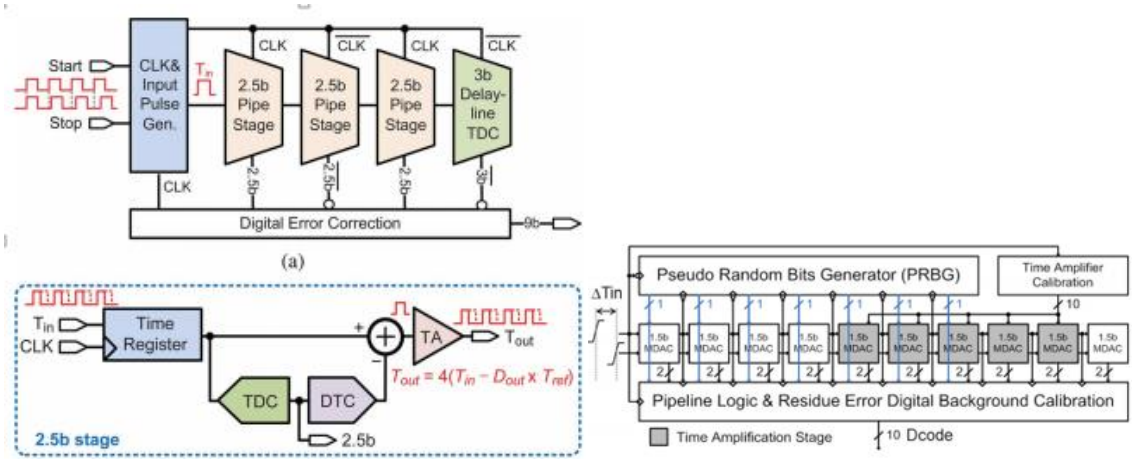


Figure 1.9: (a) Synchronous pipelined ADC – 2.5 bit/stage [33] (b) Architecture of the proposed 10-b asynchronous pipelined TDC [34]

1.4.3 Interpolation TDCs

Another technique to enhance TDC resolution beyond gate-delay is to interpolate between the input and output signals of a digital gate. Fig. 1.10 illustrates this concept using a resistive divider, where the undriven nodes are taken to be the average of the delay element input and output signals and in Fig. 1.11, digital -gates acts as sub-delay elements to produce averaging effect [37]. The operation of averaging creates a new intermediate signal with a transition that effectively divides the gate-delay into two smaller intervals. All of the new signals must be registered appropriately, which increases the TDC size, but a cyclic architecture can be utilized to mitigate this issue [36]. However, achieving a significant

improvement in resolution requires more than two delay elements to be connected in parallel, which significantly increases the complexity of the multiplexer. It can be observed that the improvement in resolution is practically limited by the non-linear impedances of the delay elements during the switching transients.

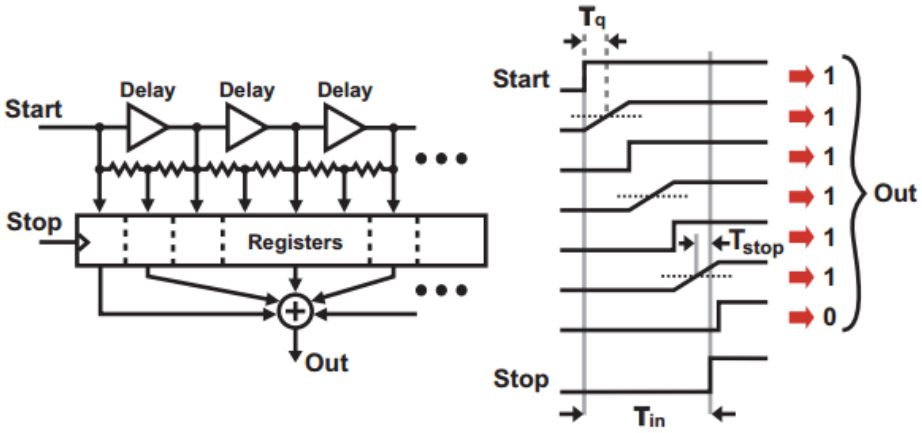


Figure 1.10: Analog interpolating TDC for creating transitions with sub-gate-delay spacing [36]

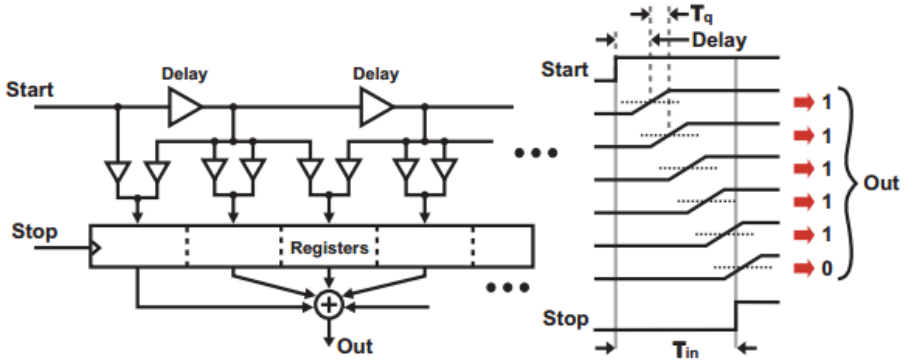


Figure 1.11: Digital technique for creating transitions with sub-gate-delay spacing [37]

The local passive time interpolation technique [36] with minimum latency and minimum dead-time with a resolution of 4.7ps proves to be the attractive design but still its resolution is highly limited by PVT variations and necessitates calibration intensive design. Also the area and power proportionally increases with range.

1.4.4 Oversampling TDCs

Noise shaping is another method for reducing the in-band TDC quantization noise contribution in a DPLL. This type of TDC uses a gated ring-oscillator (GRO) [37] instead of a delay line which results in accumulation of the quantization errors across successive measurements. The relatively large quantization error is therefore shaped in frequency as in a first order modulator, assessed from the equation below.

e[k] = Phase Error[k] + q[k] – q[k-1]

This quantization noise is largely pushed towards higher frequencies, where it is suppressed by the low-pass filter in the DPLL. In Fig. 1.12 a simple GRO based noise shaping TDC is demonstrated by enabling ring oscillator only during measurement intervals and the states of oscillator are holded between measurements. Averaging these errors results in first order noise shaping and thus improves resolution.

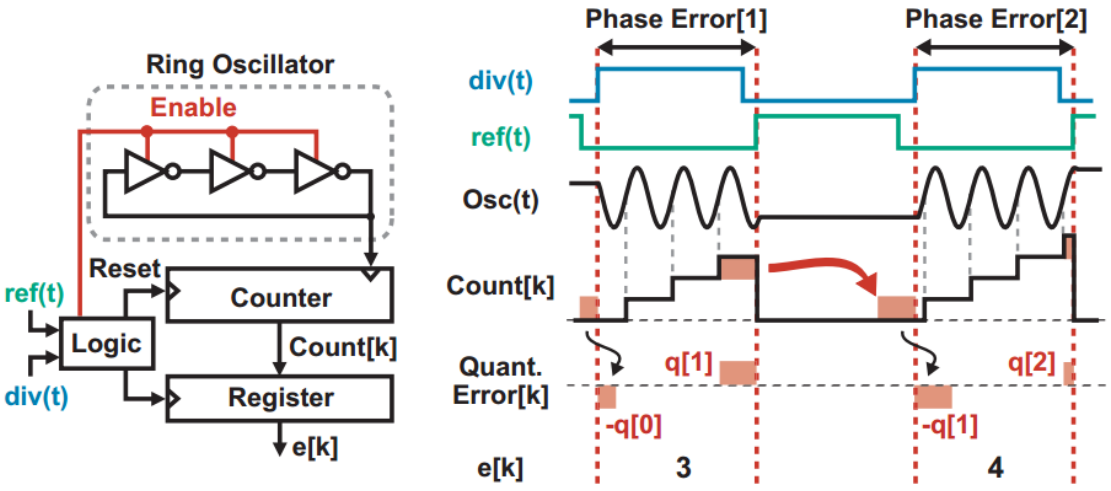


Figure 1.12: Demonstration of 1st order Noise Shaping using GRO [38]

Based on the premises above, several variants of noise shaping TDCs like multipath GRO, 2D GRO, 1-1-1 MASH (Multistage noise shaping) and 1-1 MASH 2D GRO [38-41] are implemented to achieve high resolution and performance. However the limitations of this architecture are low signal bandwidth, resolution limited by Over Sampling Ratio (OSR),

degradation of noise shaping performance due to mismatch among the stages and higher power-area consumption.

1.4.5 Stochastic TDCs

Besides the aforementioned architectures, other popular TDCs are such as stochastic TDCs, SAR TDCs and Cyclic TDCs. Stochastic TDCs [42-43] are based on stochastic properties of the arbiters. Each arbiter from the set, given the same input signals, f_{REF} and f_{DIV}, will react differently because they exhibit finite random mismatches resulting from Gaussian distribution of process variations and this results in accumulation of transfer function. Hence, the statistical variation becomes the effective time resolution of TDC. Even though resolution would be high, the linear region of the transfer function is inherently short. Due to this the detectable range is limited and the performance is heavily dependent on the technology used.

1.5 Current State of Art

After the brief discussion of various architectures, a Table 1.1 summarizes the comparison of current state of art TDC architectures based on the lowest resolution. Based on this, the target specifications are framed.

Table 1.1: Comparison of state-of-the-art TDC architectures

	[28]	[44]	[45]	[35]	[38]	[43]	[46]
Technology	65nm CMOS	65nm CMOS	35nm CMOS	130nm CMOS	130nm CMOS	Fin FET 14nm	65nm CMOS
Supply	1.2 V	0.9 V	3.3 V	1.3 V	1.5 V	0.6 V	1.0 V
Bits	7	12	12	11	11	10	10
Resolution	4.8 ps	0.63 ps	1.22	0.63 ps	1 ps	1.17 ps	0.83 ps
Sampling Rate (Ms/s)	50	10	100	65	50	100	40
FOM (pJ/conv)	1.14	0.1	0.65	1.26	0.2	0.025	0.72
Area (mm^2)	0.067	0.011	4.45	0.32	1	0.036	0.06
Type	Vernier	Cyclic	Interpolation (hybrid – Cyclic-SAR)	Pipeline	Oversampling	Stochastic	SAR

1.5.1 Target Specifications

The key performance metrics that we will pursue for this design are high resolution and high linearity in the TDC time-to-digital mapping characteristic, and low power and low area in its implementation. Based on the comparative study of current state of art architectures the following performance metrics are targeted which concludes the highest resolution of TDC ever achieved.

Resolution: 0.25 ps

Sampling rate: 100Ms/s

Linearity – (SNDR): 80dB

ENOB > 12 bits

The design is implemented in 40nm CMOS technology with a supply voltage of 1.1V.

Chapter 2: 2nd order Noise Shaped Asynchronous SAR TDC

2.1 Background

Before describing architecture/design details, an initial discussion of a SAR based TDC [46] architecture from which the current design is inspired is discussed briefly in this section. This design is based on TAC (Time to Amplitude Converter) followed by an ADC.

The conceptual block diagram is shown in Fig. 2.1 where time interval is translated to charges on a capacitor using a charge pump and then the charges are quantized by an ADC. From a simplified equation: $t_{res} = CV_{LSB}/I$, the time resolution can be boosted by increasing the current, reducing the capacitance, or enhancing the ADC's resolution. The capacitance C is total capacitance of one differential side of the Digital-to-Analog (DAC) array of SAR ADC. The performance achieved from this topology is listed in Table - 1.

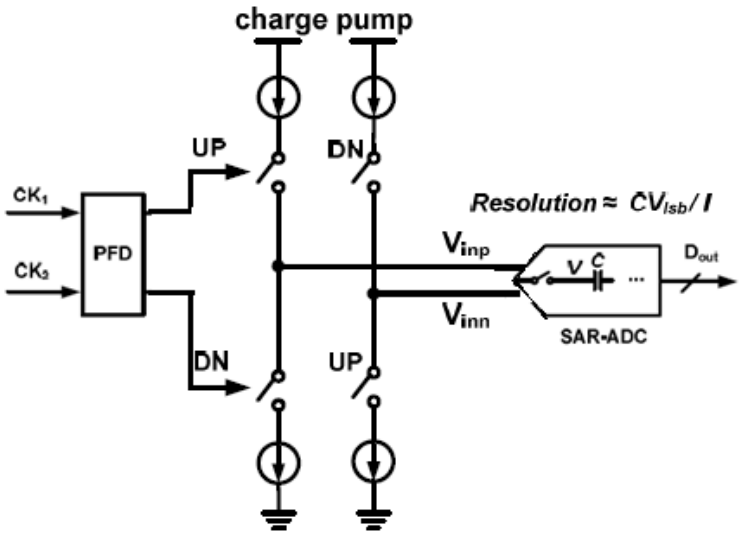


Figure 2.1: Charge pump based SAR TDC Architecture [46]

The following are the downsides of this architecture:

- The use of charge pump as main element for TAC results in nonlinearity of TAC, the static power consumption due to the constantly turned on current sources and lastly the thermal noise and mismatches from the current source causes undesired harmonics.
- Also the resolution is dependent on increasing the current I, which is not viable solution considering already higher power consumption of 2.47mW from 1 V supply.
- An important thing to observe is, the down scaling of C (decreasing C for improving resolution) is contrary with the up scaling of SAR ADC (increasing Capacitance for enhancing V_{lsb}).
- Additionally, this design involves charge-pump whose elimination was one of the motives behind Digital PLLs.

Hence, from the above discussion it's clear that, in this architecture there's no further room for improvement of resolution besides the aforementioned limitations.

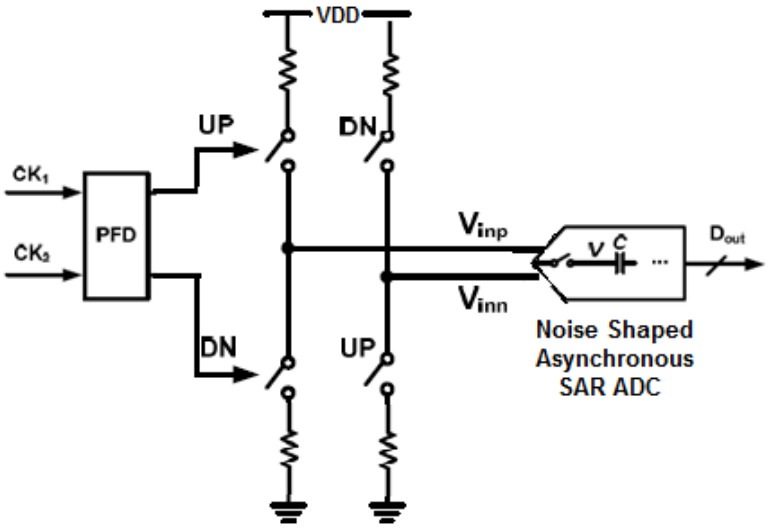


Figure 2.2: Proposed TDC Architecture

In the proposed architecture in Fig. 2.2, the TAC is implemented using simple RC charging /discharging circuit which eliminates charge pump and thus its issues. Since the maximum

phase that needs to be detected will be only few hundreds of pico seconds, from the Taylor series expansion, the RC time to voltage conversion will be quite linear. The TAC circuit implementation and analysis is described in detail in the further sections. As the resistances are made of poly, the area is also comparatively less. The mismatch due to process variations will result in static offset and doesn't affect the linearity, unlike the mismatch in current-sources of charge pump that result in nonlinearity.

2.2 Motivation – Noise Shaping Asynchronous SAR ADC

The choice of ADC plays a crucial role in the design. A flash ADC is capable of extremely high speed with low resolution. To increase its dynamic range, the comparators increase exponentially and hence significant power, area and calibration are involved. A pipeline ADC features high resolution and high speed. However, the amplifiers consume much power, and designing a high gain op-amp becomes tough with recent technologies. A delta-sigma ADC faces the similar situation due to its integrators, although it achieves extremely high resolution [47]. And also the conversion speed will be low. Asynchronous SAR ADC is chosen due to its several advantages for the proposed TDC. First, unlike other types of ADCs, it only contains one Capacitive DAC shared between both TAC RC circuit, sampling and quantization, as well as one comparator. Thus, a compact structure is available. Since, its asynchronous in nature, there is no directional tradeoff between power and speed in this topology and a need of external clock/source unlike Synchronous architecture. By using metal-oxide-metal (MOM) capacitors and a dynamic comparator, it squeezes power and area consumptions to be low with enough sampling rate for DPLLs.

However, for the extension of resolution beyond 10 bit, capacitance of binary DAC array increases exponentially by two and since majority of power and area consumption in any SAR ADC is attributed to DAC array, this increases power consumption and also chip area. Moreover, as capacitance is increased the conversion from time to analog voltage is also affected. Hence, the resolution is increased further by around 3 bits by 2^{nd} order noise shaping and oversampling. The passive noise shaping is achieved by charge transfer

mechanism, eliminates the need for power-consuming OTAs for integration. This 2nd order noise shaped asynchronous SAR hybrid architecture is discussed in detail in further sections. ADC architecture is implemented in fully-differential configuration that benefits from improved common-mode noise rejection, doubling of the signal voltage range, reduction of even order harmonic distortion and thus improves ENOB.

2.2.1 Design Calculations

The circuit is implemented in 40nm CMOS technology and with supply voltage of 1.1V. For simplicity, calculations are evaluated for the targeted range of 200 ps. The maximum OSR for 2nd order noise shaping is 8. The 13 bit ADC is achieved by the combination of 10 bit Asynchronous SAR ADC and 3 bits Noise shaping.

Target SNDR from entire ADC = 6N + 1.76 = 80 dB

SNDR from 10 bit SAR ADC > 61.76 dB

$V_{LSB} = \frac{V_{FS}}{2^N} = \frac{2.2}{2^{13}} = 0.26$ mV

Noise associated with the switch is sampled by the capacitor and this contribution is known as $\frac{kT}{C}$ noise. This thermal noise from the capacitive DAC array should not limit the SNDR of the 12 bit ADC. Hence from the calculations below, the lower limit of total capacitance is evaluated which is 0.84 pF.

$\frac{KT}{C} < \frac{\Delta^2}{12} \Rightarrow C > 12KT \left(\frac{2^N}{V_{FS}}\right)^2 \approx 0.84$ pF

For an 10-bit SAR ADC, the total DAC array capacitance of one differential side is assumed to be 1 pF for simplicity based on DAC switching technique, No of Bits, SNDR required (KT/C noise calculations mentioned above), power consumption, speed and smallest available CRT – MOM unit capacitance (1.515 fF).

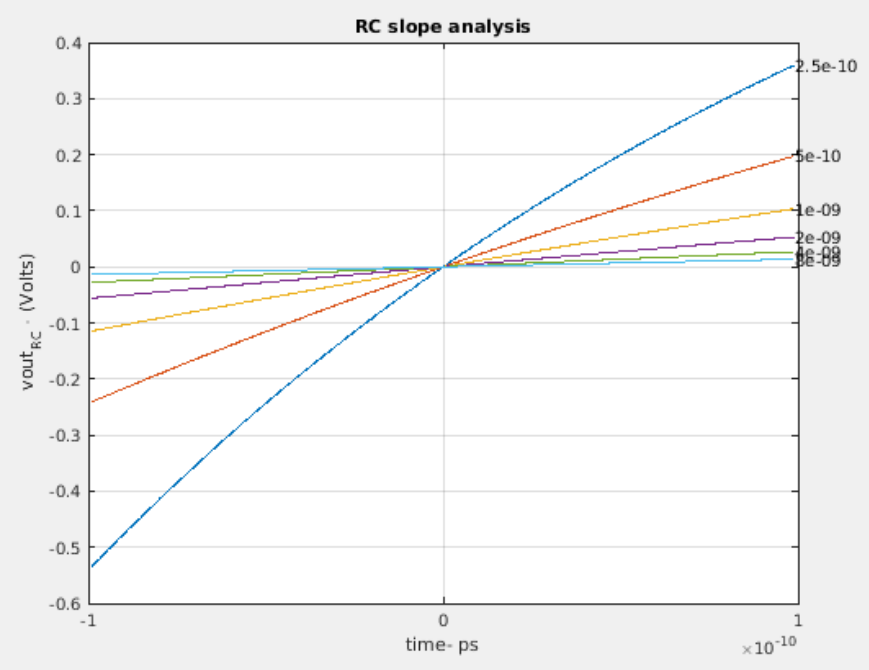


Figure 2.3: RC charging - $Vout_{RC}$ vs time

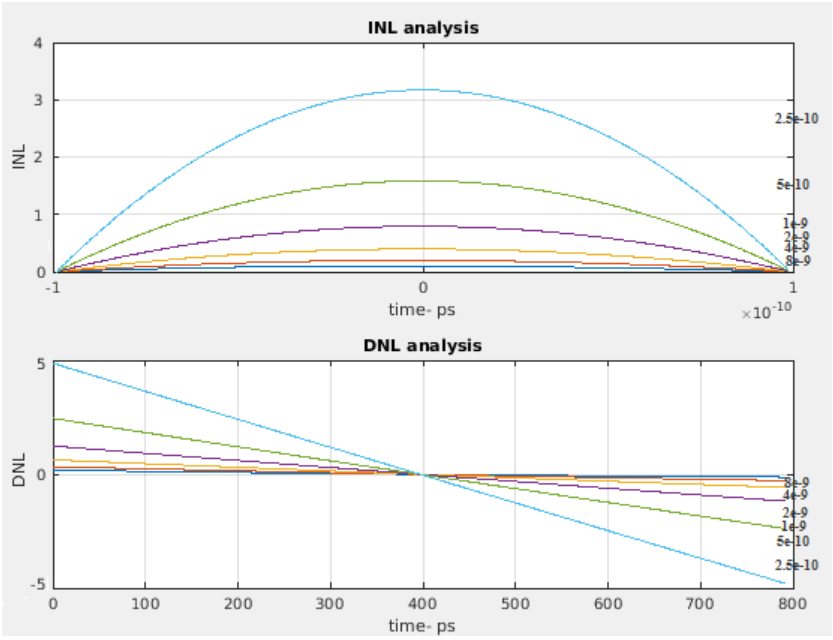


Figure 2.4: $Vout_{RC}$ vs time – INL/DNL analysis

The choice of RC decides the range, linearity and resolution of TAC. Hence a brief mathematical analysis is done in Matlab. The RC values are swept from $2.5\text{x}10^{-10}$ to $8\text{x}10^{-9}$ by a multiplicative ratio of 2. The voltage and DNL-INL plots for Taylor expansions of uncompensated values are shown in the Fig. 2.4. It can observed that, as RC value decrease the quantization step scaling becomes non-uniform which increases non-linearity though it provides sufficient voltage to be detected is illustrated in Fig. 2.3. But as RC value increases, the corresponding voltage for resolution - 0.25ps will be too small to detect by 13 bit ADC and also area for either R /C increases. Hence for an optimum performance for TAC's Dynamic range and resolution, an RC of $1\text{x}10^{-9}$ is chosen.

$$t_{range} = 200ps \text{ (signal swing : } -99ps \; to \; 99 \; ps)$$

$$\text{C= 1pF} \quad \text{RC} = 1\text{x}10^{-9} \Rightarrow \text{R=1 K}\Omega$$

From simulations of ideal RC switching circuit for TAC front end in Fig. 2.5, the upper limit of range $t_{\,max}$ - 100ps corresponds to a voltage of 100 mV. By Taylor series and also from above mathematical analysis of RC, assuming linear slope for time to voltage scaling from RC charging/discharging, $\text{resolution} - \text{t}_{\text{LSB}}$ of 0.25 ps corresponds to a voltage of 0.25 mV which is approximately equal to V_{LSB} and hence can be detected by 13-bit ADC. Thus, from these design calculations equipped with simulations, design parameters R and C are approximately evaluated.

$$t_{\,max} - 100 \; ps \rightarrow \; V_{RC} \sim \; 100 \text{ mV}$$

$$t_{\,LSB} - 0.25 \; ps \rightarrow \; V_{RC} \sim \quad 0.25 \text{ mV} \sim V_{LSB}$$

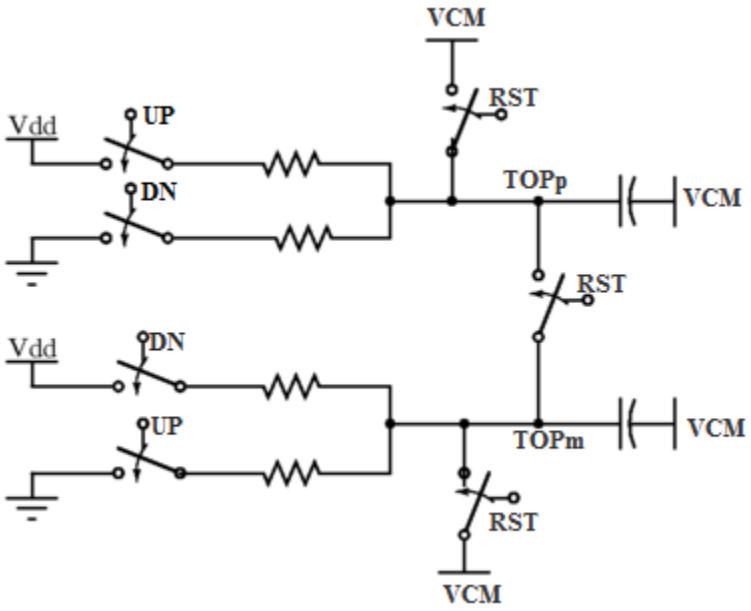


Figure 2.5: TAC's RC switching circuit – Ideal

As the target range of 200 ps in time domain approximately corresponds to 200 mV in voltage domain. Hence the output signal swing of TAC (V_{swing_TAC}) that needs to be detected is 200 mV. This obviates the need of two comparison cycles (2 MSB bits are fixed across the range of 200 mV) for SAR ADC, as the ADC is designed for a signal swing of 2.2 V (+1.1 - -1.1) due to the power supply being 1.1 V. From the calculations below, the reduction of comparison cycles by two result in a voltage swing of 550mV that can be detected by ADC. This limit is reasonably above output signal swing of TAC.

$$\frac{\boldsymbol{V_{swing\_ADC}}}{\boldsymbol{2^{No\ of\ CMP\ cycles}}} = \frac{\boldsymbol{2.2\,V}}{\boldsymbol{2^2}} = 550\text{ mV} > \boldsymbol{V_{swing\_TAC}} \approx \pm 100\text{mV}$$

This also results in increment in 20 dB of SNDR ($\frac{V_{swing\_ADC}}{V_{swing\_TAC}} = \frac{2.2}{0.2} = 10 \sim 20dB$) due to gain compensation of range from time domain to voltage domain. Thus the target SNDR is reduced from 80dB to 60dB.

2.3 Time to Amplitude Conversion (TAC) Front End

The Time to Analog Conversion Front end briefly consists of two parts whose circuit analysis and implementation is discussed in detail in this section.

1. PFD – for generation of UP, DN and PH signals
2. RC switching circuit – responsible for conversion of time domain to voltage domain

2.3.1 Circuit Implementation & Analysis

The PFD (Phase-Frequency Detector), can detect both phase and frequency differences between two periodic signals and generates them as UP and Down (DN) signals whose pulse width is proportional to phase difference [48]. The circuit implementation of PFD is shown in Fig. 2.6 and the timing diagram for clock signal A leading B is presented in Fig. 2.7. The mismatches between capacitive loading of UP and DN signals will result in offset and hence this issue necessitates symmetric NAND and NOR gates at the output. Any kind of mismatches between UP and DN pulse generators due to layout or PVT variations appears as a static offset in time domain which can be resolved during calibration. The D Flip Flop is implemented by two cross-coupled RS latches. Latch 1 and Latch 2 respond to the rising edges of CK and Reset respectively. The UP, DN and PH signals generated from CK1 phase leading CK2 are demonstrated in Fig. 2.7. The PH signal that represents the summation of UP and DN pulses acts as a trigger for the Asynchronous SAR operation which is discussed in further sections.

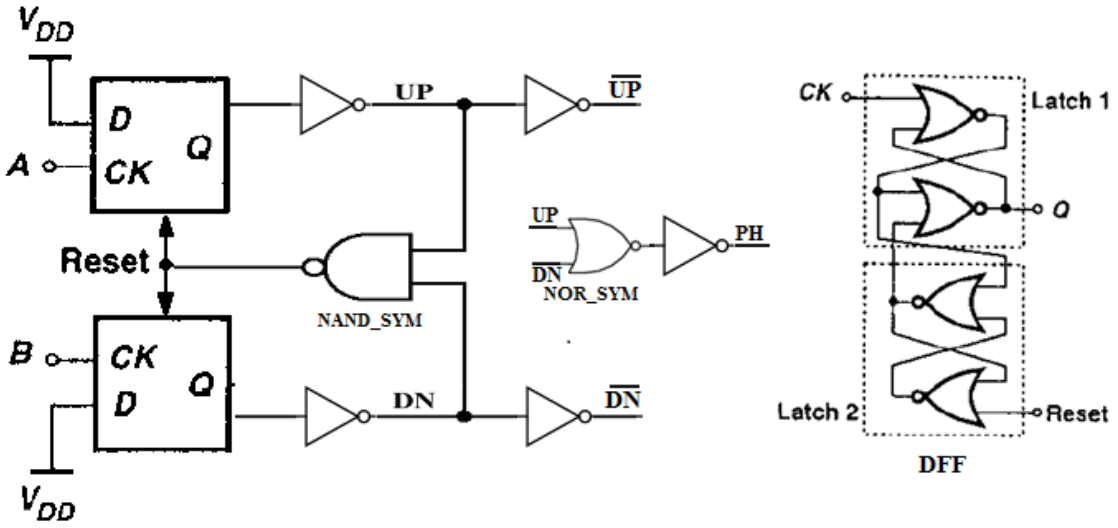


Figure 2.6: PFD Circuit Implementation

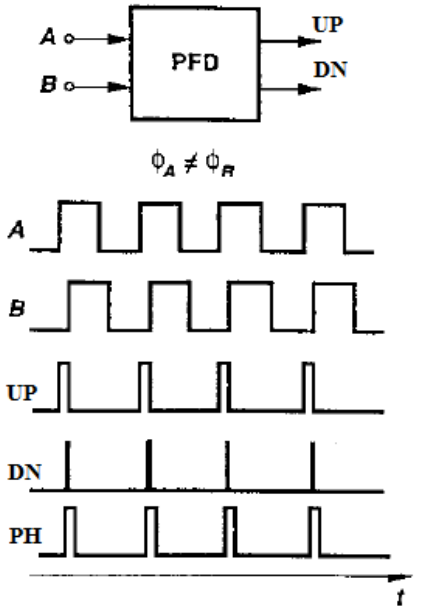


Figure 2.7: Signal Operation of PFD [47]

The circuit implementation of TAC's RC switching circuit is shown in Fig. 2.8 and simulation results for INA leading INB are shown in Fig. 2.9. The UP signal is responsible for charging the positive differential side (top plate) of DAC capacitor array (TOPp) and discharging the negative differential side of DAC capacitor array (TOPm). On the contrary,

DN signal is responsible for charging TOPm and discharging TOPp. Thus the input RC sampling is implemented differentially to obviate even order harmonics and thus improves linearity. The resistance is chosen to be 1K Ω, implemented using poly without salicide, large enough to dominate the non-linear resistance of switches in series. The capacitance is realized from binary weighted DAC array which is approximately 1.02 pF. A pair of NMOS reset switches connected between TOPp and TOPm aids in neutralizing any residual charges differentially and thus improves linearity. These switches are arranged in parallel and of opposite polarity so as to provide symmetrical parasitic capacitances (C_{gs} and C_{gd}) on either sides. During Reset operation, the TOPp and TOPm are charged to common-mode voltage ($V_{CM} = \frac{V_{DD}}{2}$) which is the bias point for the input transistors of comparator. The bottom plate of the capacitors are connected to DAC switching array for ASAR binary operation. The output of TAC front end TOPp and TOPm are connected to the comparator of the ADC. The sizes of the switches are listed in Table 2.1.

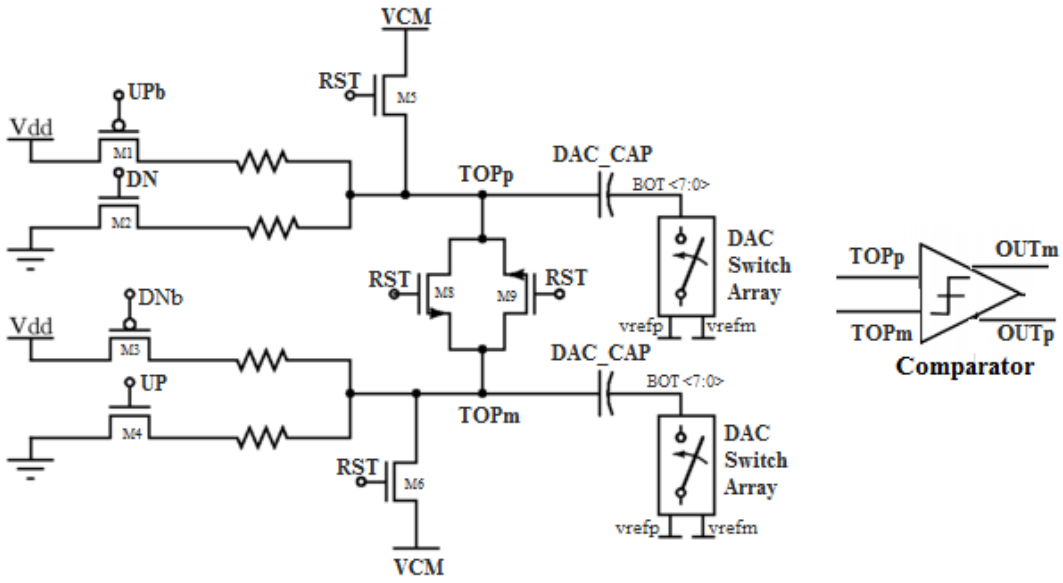


Figure 2.8: TAC's RC switching Circuit

Table 2.1: Sizing of Switches

Transistors	Size (W/L)	Comments
M1, M3	16u/40n	PMOS switch to VDD is in RC charging path and hence its parsitic capacitance should be small enough
M2, M4	8u/40n	NMOS switch to gnd is in RC discharging path and hence its parsitic capcitance should be small enough. Also its resistance and capacitance should be similar to PMOS switch to eliminate mismatch between charging/discharging – hence half its size
M5,M6	1u/40n	Reset NMOS switch to VCM – parasitic capacitance does'nt interfere – hence smaller size
M8,M9	8u/40n	Reset switches – parasitic capacitance results in coupling between TOPp & TOPm – leads to non-linearity (harmonics) Hence larger size – total width 16u

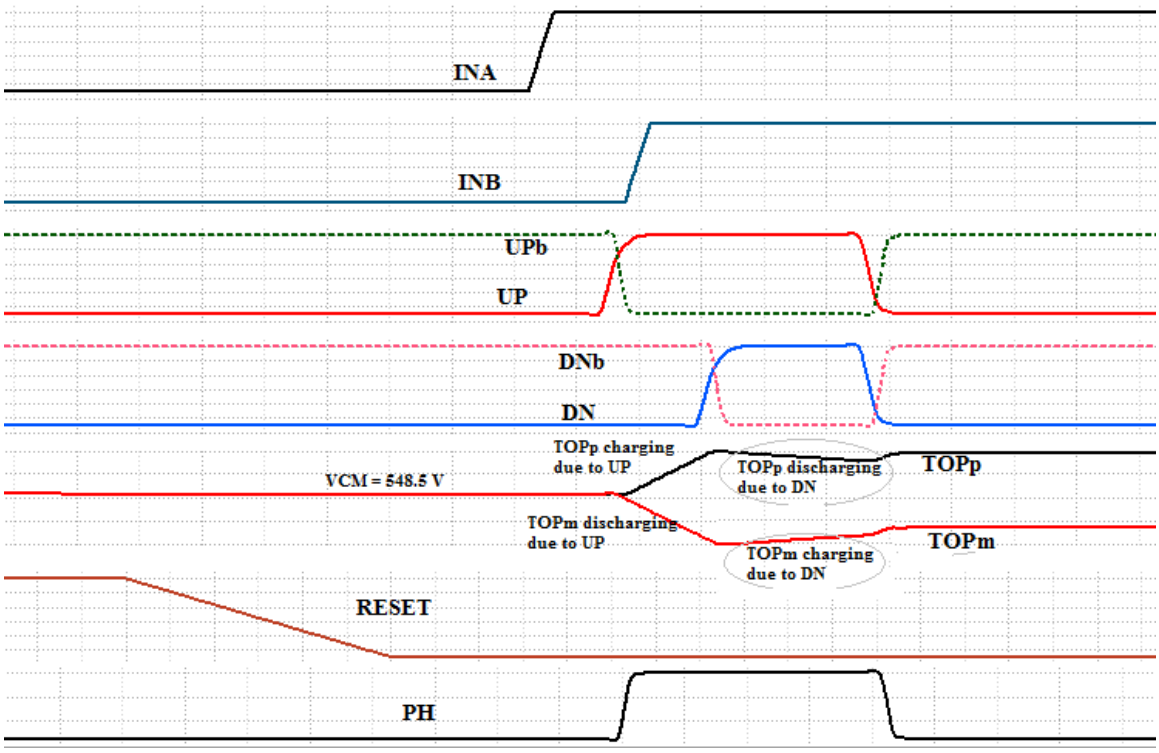


Figure 2.9: Signal and Timing diagram of TAC

2.3.2 Observations

Three observations can be made from the above simulation results of output signals

1. It is evident from Fig. 2.9 that when both UP and DN are high there is resultant discharging of TOPp and charging of TOPm due to both paths on. Nevertheless, this results in overall small reduction of differential output (TOPp - TOPm) which can be compensated by multiplying gain while mapping digital values to time domain without affecting the performance.
2. Also the parasitic capacitances referred at terminals TOPp/ TOPm constituted by inputs of comparator, switch array and reset switches result in overestimation of voltage outputs of TAC due to formation of capacitor divider. However, since these non-linear parasitic capacitances are negligibly small compared to DAC capacitance, the linearity is not affected. Any kind of gain error can be compensated through calibration.
3. It can be observed that during reset operation, the differential outputs doesn't settle exactly to V_{CM} = 550mV but this can be appeared only as offset as differentially both the values TOPp and TOPm are identical to 548.5 mV. This is achieved by the pair of reset switches (M8, M9).

2.3.3 Test Bench Evaluation

Similar to ADC, the performance parameters of TDC such as SNDR, resolution and sampling rate are evaluated by a sinusoidal signal but with respect to time-domain. Two clock signals INA and INB of frequency 100 MHz (Sampling rate) are phase modulated such that their difference in delays (INA-INB) forms Sinusoidal signal of peak to peak amplitude 200ps which represents range. This functionality for generating phase modulated clock signals is accomplished by Verilog AMS model – PM generator. It is observed that the SNDR of PM generator is limited by the step of transient analysis during simulations i.e., if the step size = 0.1ps, range = 200ps, total no of points = $\frac{200\text{ ps}}{0.1}$ = 2000

≈ 11 bits $\rightarrow$ SNDR ≈ 68 dB. Hence, choice of step size for transient analysis plays a crucial role for TDC evaluation. Similarly, for DNL-INL test, a ramp signal in time domain is generated by linear increment of delay of 0.25 ps between clock signals INA and INB.

2.3.4 Simulation Results

The DNL- INL plots for uncompensated and compensated TAC output voltages is shown in the Fig. 2.10. The plot corresponds to time domain ramp signal with step of 1 ps and range of 100ps but later normalized to 0.25 ps. The uncompensated values represent differential voltage output of TAC ($\mathrm{Vout_{TAC}} = \mathrm{TOPp} - \mathrm{TOPm}$) and RC compensated values represent TAC output reverse mapped to time domain from equation below. Gain in this equation represents the attenuation of $\mathrm{Vout_{TAC}}$ when both UP and DN signals are high as discussed earlier. It is evident from the plots (Fig.2.10), that linearity is improved after RC compensation. DNL corresponds to 0.1364/-0.1534 LSB and INL corresponds to 0.04235/-0.1825.

$$\mathrm{t_{RC\_compensated}} = \mathrm{RC} \times \log\left(1 - \frac{\mathrm{Vout_{TAC}}}{\mathrm{Vdd} \times \mathrm{Gain}}\right)$$

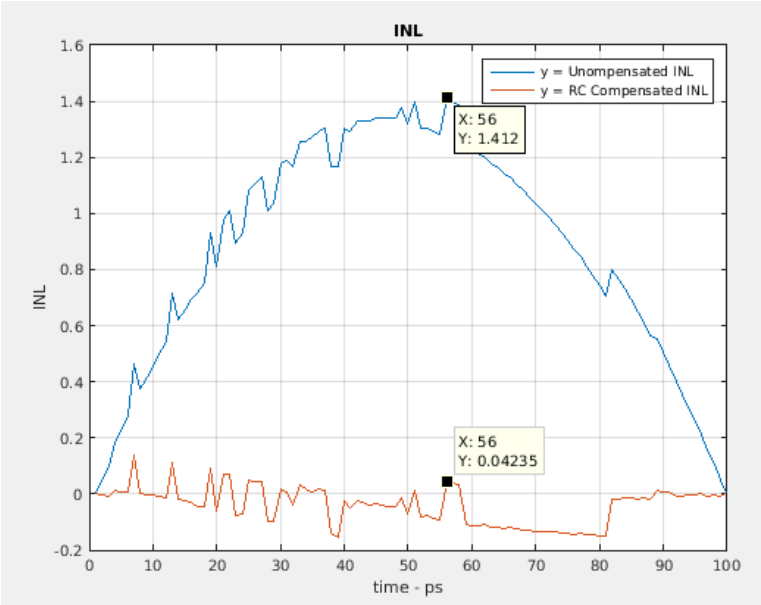


Figure 2.10: INL and DNL plots for TAC

The output spectrum of TAC both RC compensated and uncompensated is shown in Fig. 2.11. The spectrum represents 256 point Fast Fourier Transform (FFT) of the differential output voltage of TAC for a sampling rate of 100 MHz and an input frequency of $\frac{300}{256}$ MHz for time-domain sinusoidal signal step size of transient simulation is set to be 0.2

ps. The SNDR is 63.75 dB ~ 10 bits represents 1024 points which is much greater than $\frac{t_{range}}{t_{res}} = \frac{200\ ps}{0.25\ ps}$ = 800. The 3rd and 5th order harmonics are low enough not to impact the linearity. It can be observed that the SNDR represents 10 bits which is limited by the step size of 0.2 ps used ($\frac{200\ ps}{0.2\ ps}$ = 1000). However, the targeted performance of 0.25 ps from TAC is achieved.

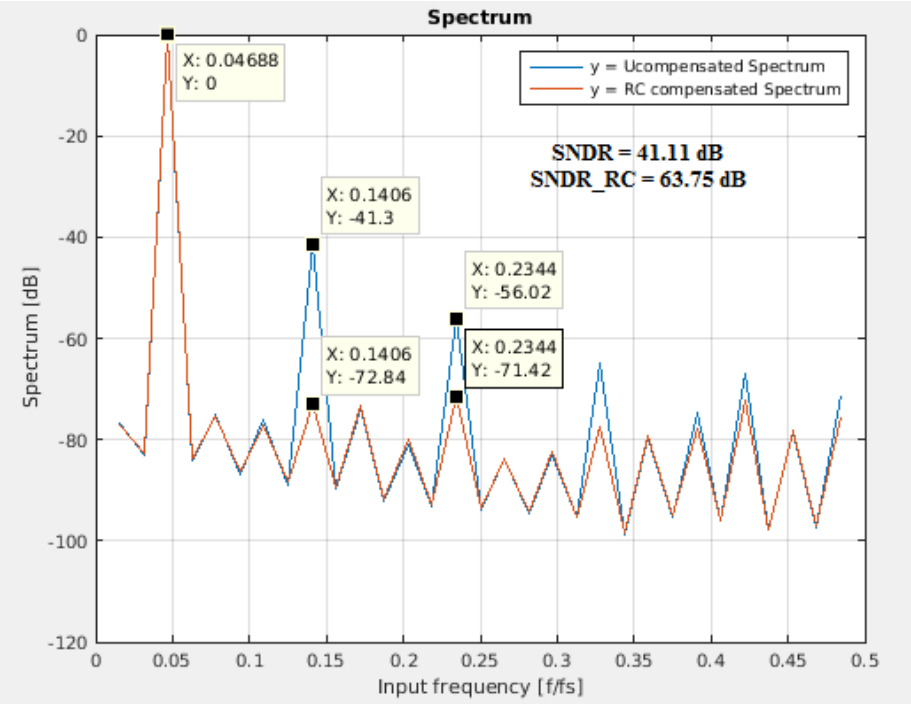


Figure 2.11: Output Spectrum for transistor level PFD

2.4 Noise Shaping Asynchronous SAR ADC backend

Before the discussion of entire noise shaping backend, an initial background of ASAR ADC is presented which aids in understanding of complete architecture and especially helps to appreciate the timing diagram. The 2nd order noise shaping ASAR ADC backend was primarily designed by Dr. Wenjuan Guo.

2.4.1 Asynchronous SAR ADC

2.4.1.1 Background

Successive approximation register (SAR) charge redistribution ADCs are known for their outstanding power efficiency as well as good technology scaling characteristics. However, since SAR ADCs use a serial conversion algorithm, their low power advantage significantly deteriorates at high sampling frequencies around 100 Ms/s.

As the name suggests, SAR ADCs convert an analog input to its digital equivalent by a series of successive approximation steps, usually using a binary search algorithm. A simple block diagram representing this process is shown in Fig. 2.12. The DAC output voltage is compared to the input signal and the result of this comparison is fed back to the DAC, thereby closing the successive approximation loop. The control logic is designed to perform a feedback subtraction and brings the DAC voltage closer to the analog input with every comparison (see Fig. 2.12). As a result, the converter's resolution depends on the number of successive approximation cycles (serial operation). In addition, the resolution is primarily limited by the sensitivity of the comparison block, electronic noise and the accuracy of the DAC.

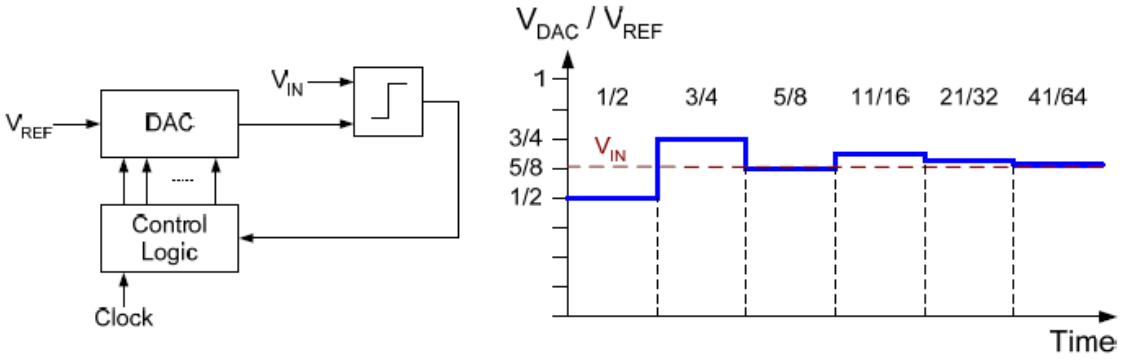


Figure 2.12: Operation of Conventional SAR ADC

2.4.1.2 Principle & Operation of Asynchronous SAR ADC

The concept of ASAR charge redistribution architecture was first introduced in [48]. It aims to eliminate the conversion speed constraint of a conventional synchronous SAR ADC, which relies on an internal clock to divide the time into DAC settling and comparison cycles from MSB to LSB. Since every clock cycle must account worst comparison time and clock jitter as in Fig. 2.13, the conversion speed is highly limited by design especially the comparator. As the input difference becomes increasingly small, the comparison time increases and hence the worst comparison time occurs for lowest possible input voltage - LSB/2. Instead of a synchronous clock driving the ADC, if timing is driven by VALID signal from comparator which represents that end of comparison, reduction in overall comparison time can be achieved as in Fig. 2.13. This also eliminates the necessity of internal high speed clock and thus reduces power consumption. However, a global clock is required for sampling which in this design can be incorporated by PH signal that represents summation of UP & DN signal.

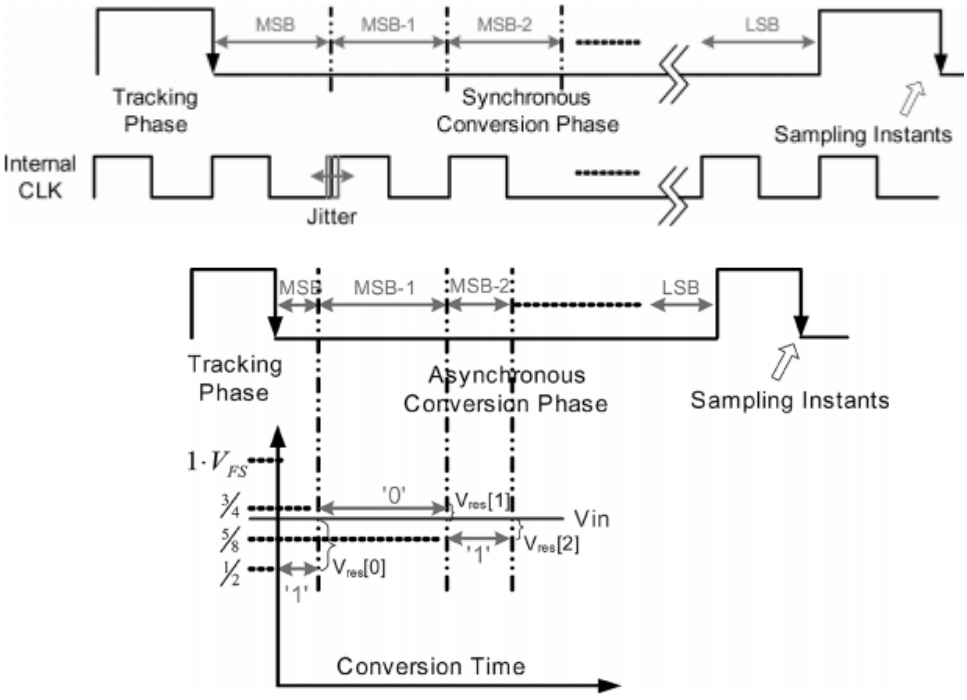


Figure 2.13: Synchronous vs Asynchronous SAR conversion [48]

2.4.2 Sequences of Operation – TDC

A detailed flow chart is presented in Fig. 2.14 and corresponding timing diagram in Fig. 2.15 aids in comprehension of operation of TDC. The PH signal which is generated from PFD block acts as a sampling clock and serves as a trigger for timing logic of noise shaping ADC backend. PH pulse enables the STOP_CMP comparator that acts as a pulse for ASAR ADC operation. When STOP_CMP is low, the comparator is enabled. PH pulse also enables STOP_CLK, which acts as trigger for ASAR logic block. Additionally, PH pulse enables STOP_NS which further enables Noise Shaping sub circuit. STOP_CMP when low generates LATCH signals for eight cycles with a period that can be tuned through v_{bias} for delay cell as shown in Fig. 2.16. LATCH is the control signal for the dynamic comparator. During each cycle which is triggered by Latch clock signal, a VALID signal is generated by the comparator marking the end of comparison and respective clk<n> signal is generated. These clk <n> pulses along with comparator output bits (cntrl<8:1>) acts as control signals for the DAC switching circuit. After DAC switching, a certain delay is allowed for DAC to settle for the charge redistribution. Then again another comparison cycle which involves same sequence of steps is performed. When clk <8> goes high, it marks the end of ASAR operation and disables STOP_CMP (goes high). When STOP_CMP is high and STOP_NS is low, the NS_CLK pulses (3 cycles) are triggered which act as control signal for sequence of Noise Shaping operations. NS_CLK triggers NS <0> during which residual voltage V_{res} on the capacitor is captured and later NS <1> is triggered during which effective 1st order passive integration is performed. When NS<0> goes low, RESET is enabled to clear the voltage on the DAC capacitance array to VCM and reset the sequence generator. Additionally, STOP_CLK is also enabled which makes the asynchronous logic block inactive and the digital output bits are stored onto the latches. When NS <1> goes low which marks the end of 1st order noise shaping cycle, NS <2> is triggered. NS<2> clk cycle is responsible for effective 2nd order passive integration. Reset and NS<2> goes low simultaneously and this marks the end of TDC operation.

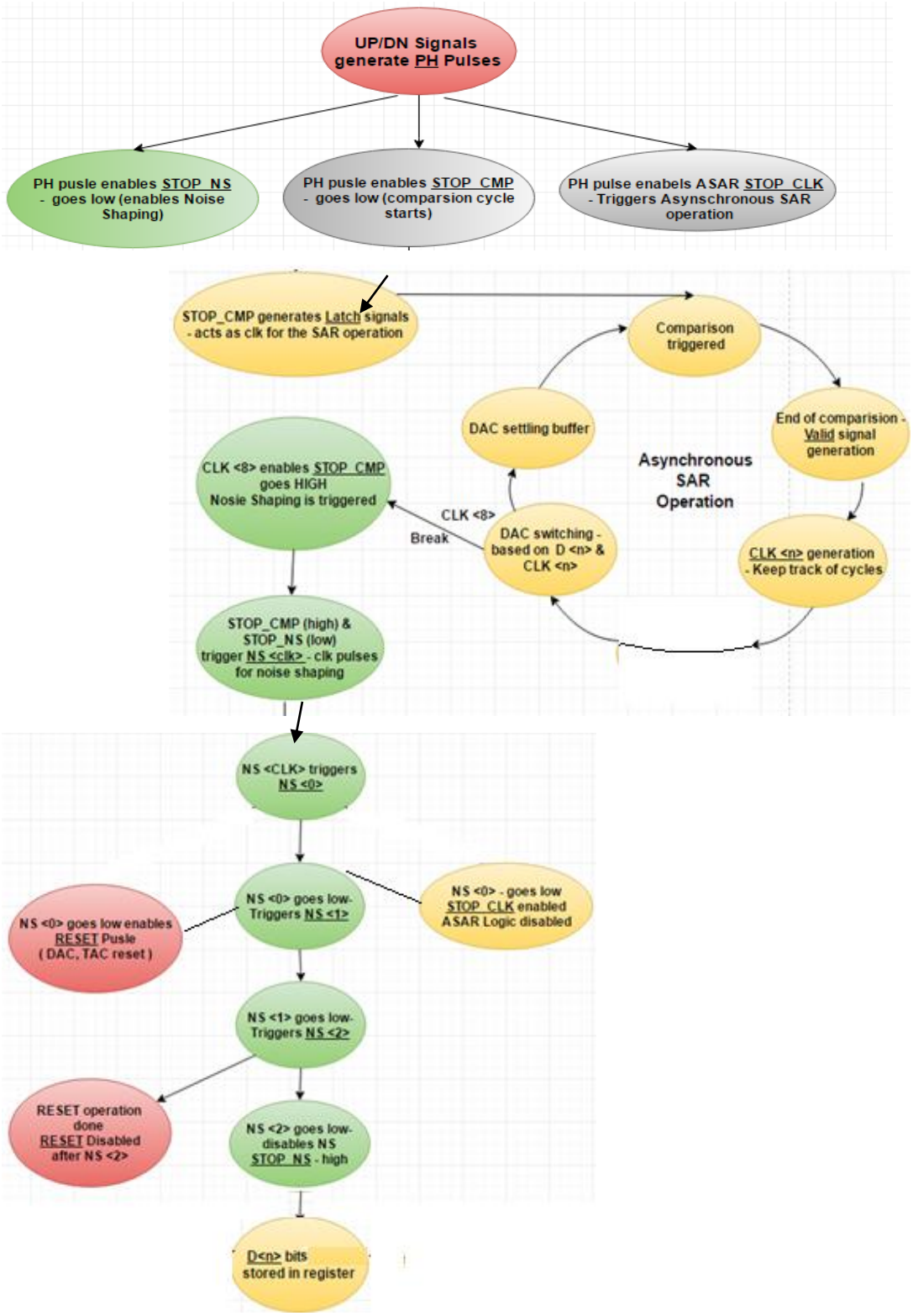


Figure 2.14: Flow chart for sequences of operation - TDC

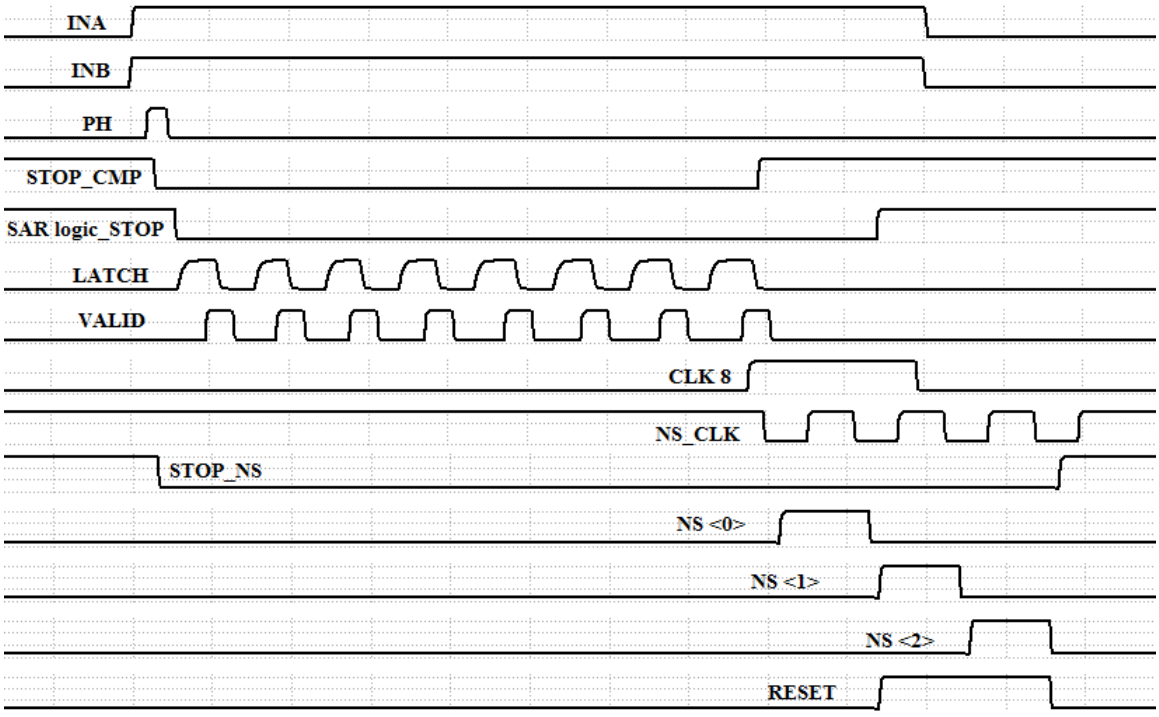


Figure 2.15: Timing Diagram of TDC

2.4.3 Asynchronous SAR ADC – Circuit Implementation & Analysis

The given design parameters dictate high speed of 100Ms/s, low power and an ENOB of at least 10-bits which necessitates an 11-bit fully differential Asynchronous SAR architecture.

The proposed converter combines a variety of design techniques: (1) judicious optimization of DAC settling with variable DAC switching circuit and optimized SAR logic with asynchronous timing, (2) a comparator designed for the optimum tradeoff between its settling time, noise & input capacitance, and (3) a symmetrically switched DAC using top-plate sampling and small unit MOM capacitance of 1.79 fF.

The ASAR architecture is presented in the Fig. 2.16 and the flow chart for sequences of operations is illustrated in Fig. 2.17. When STOP_CMP goes low, latch signal are

generated with period controlled by bias voltage (V_{bp}) in delay cell as in Fig. 2.16. This latch signals acts as control signals for the dynamic comparator. The end of the comparison is marked by the VALID signal generated from a skew NAND gate to avoid metastability issues. The Valid signal triggers the sequencer to generate clk <n> signals that keep track of comparison cycles. Based on the control signals generated from asynchronous logic, the capacitors of DAC is switched between V_{refp} $(= V_{DD})$ and ground. A delay buffer is allowed for the DAC to settle for the charge redistribution and then the comparison is again triggered. Thus the cycle continues until clk <8> goes high which marks the end of ASAR operation. Each of these blocks are discussed detail in further sections.

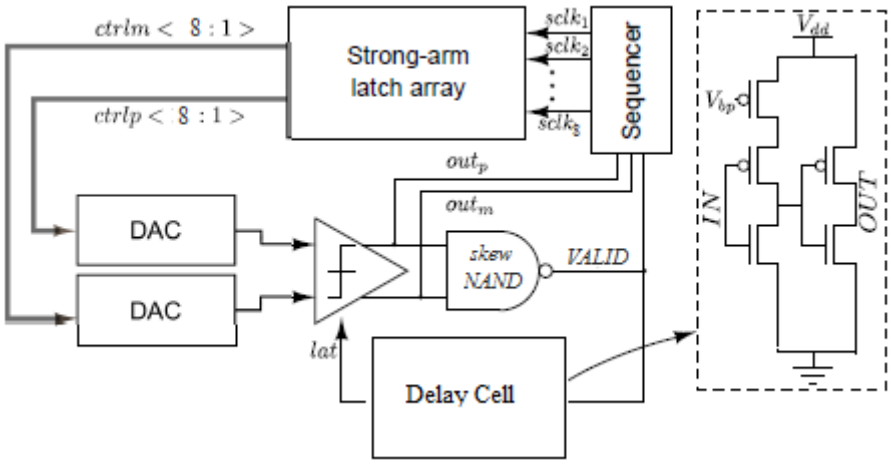


Figure 2.16: Asynchronous SAR architecture

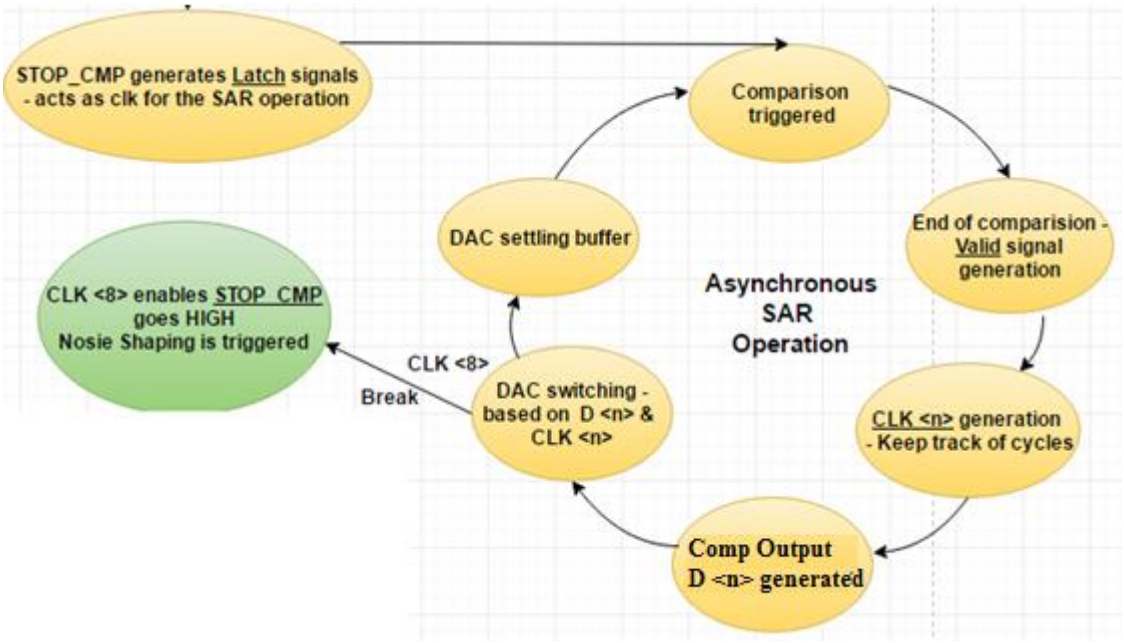


Figure 2.17: Sequences of operation – ASAR ADC

2.4.3.1 DAC Array – Circuit Implementation

Majority of power consumption in any ASAR ADC is attributed to DAC array and ASAR logic. Hence, keeping low power metric and high speed into consideration, various low power DAC switching techniques are also analysed, as shown in Table 2.2. Bidirectional switching Technique emerges to be a best fit for the given architecture as it achieves 4X capacitance reduction over conventional technique, 95% power reduction, simplicity in switching logic and moderately constant common mode voltage that relaxes the comparator design. In addition, this switching method improves the settling speed of the DAC capacitor network and therefore the sampling rate.

Table 2.2: Comparison of DAC Switching Techniques

Topology	Power	Variation in V_{CM}	Capacitance Reduction	Complexity in Switching Logic
Conventional	None	None	None	Simple
V_{CM} based	75%	None	2X	Moderate
Split Capacitor	56%	High	2X	Moderate
Monotonic	81%	High	2X	Complex
Bidirectional	95%	Moderate	4X	Complex

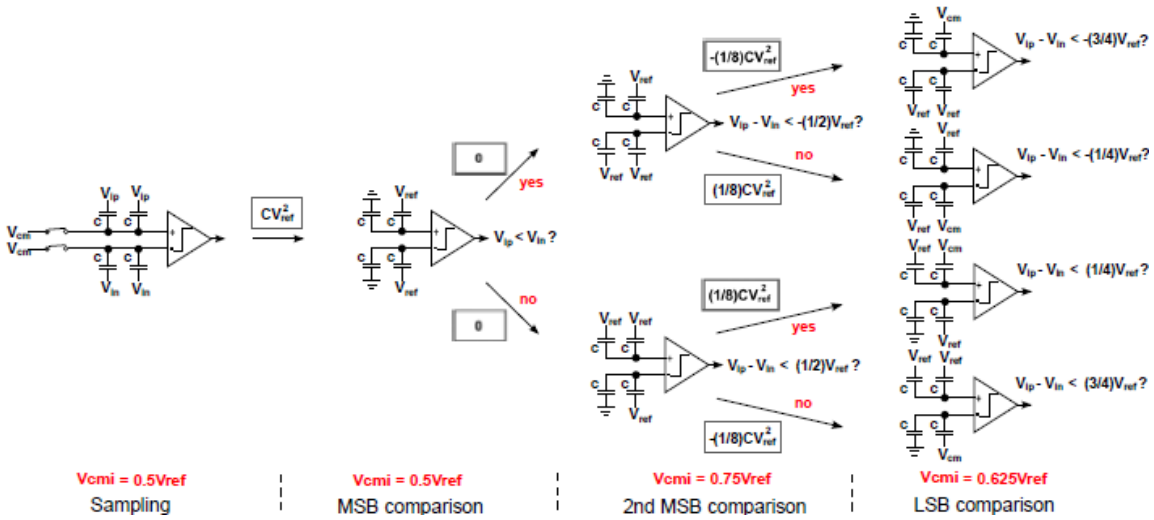


Figure 2.18: Bidirectional Switching for 3-bit SAR ADC with bottom plate sampling [50]

Fig. 2.18 illustrates the operation of the Bidirectional switching for 3-bit SAR ADC facilitated with bottom plate sampling [48-49]. At the sampling phase, the top plates of the capacitors are charged to output voltage of TAC via RC switching circuit. The PH pulse represents sampling clock. The comparator directly performs the first comparison without switching any capacitor. According to the comparator output, the MSB capacitor is switched to ground and the other capacitor (on the lower side) remains unchanged and vice versa. The ADC repeats this procedure until the LSB is decided i.e., for about eight latch cycles.

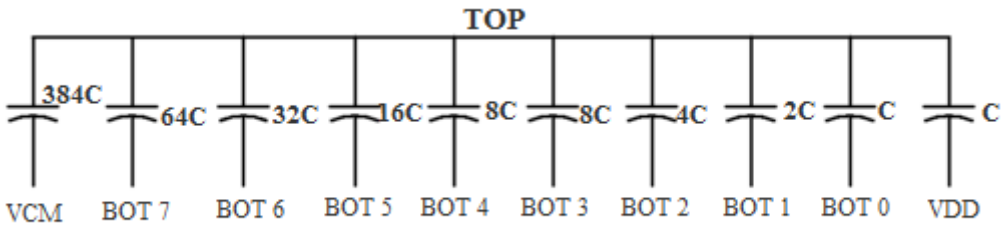


Figure 2.19: Binary weighted DAC capacitance array with redundancy

The binary weighted DAC capacitive array is implemented using MOM capacitors due to the advantages of high density and non-special process, comparing with metal insulator-metal (MIM) capacitors. Furthermore, attributed to the finger-type structure, a MOM capacitor is easy to be scaled like a CMOS transistor. The unit MOM capacitance consists of 6 horizontal and vertical fingers, M4 as bottom metal layer and M6 as top metal layer due to lesser parasitics associated with higher metal layers and minimum possible capacitance available in 40 nm technology with these metal layers constitutes to the unit capacitance of 1.7195 fF which is quite low. Hence, it necessitates the comparator and switching array to have low capacitance in order to avoid degradation in SNDR due to capacitive loading.

The trend in decreasing capacitor size is constrained by thermal noise and capacitor mismatch due to layout and parasitic capacitance. The total capacitance of the Binary DAC array is 2^{N-1} times the unit capacitance (i.e., 0.931 fF), as shown in Fig. 2.19. The relaxation of two MSB bits among 10 bits can be explained by reduced range of voltage that needs to be detected mapped from time domain range of 200 ps to voltage domain of 200 mV discussed in section 2.2.1. Hence, the MSB capacitors 256C and 128C are combined to form 384C for the simplicity of layout and connected to V_{CM} which further reduces the impact of V_{CM} variations due to bidirectional switching. Moreover, the latch cycles are reduced from ten to eight as the last two MSB bits are fixed.

The linearity of a SAR ADC system is limited by the DAC capacitor mismatch. This issue is resolved by common centroid layout the whole 8-bit DAC array (from C to 64C) as in Fig. 2.20. The whole DAC is divided into two segments, MSB DAC (from 8C to 64C) and the LSB DAC (C to 4C). The layout consists of an array of 8 vertical and 17 horizontal unit MOM capacitors. Dummy cells, represented as D in the floorplan, are placed for better matching since they reduce the impact of edge effects on capacitor mismatch. They are connected to ground to ensure the same parasitic capacitances. The highest metal M6 is used for connections of the capacitor's top plates on which input is sampled since higher metal layer has lower associated parasitics while a lower metal M4 is used to connect the bottom plates. From parasitic extraction of the capacitor values in Table, it is evident that for MSB capacitors BOT 6 & BOT 7, the error is greater than $\frac{1}{4}$ LSB which might impact linearity. It can be observed that, LSB capacitors and MSB capacitors relatively match well among the banks. The variation between LSB capacitors and MSB capacitors is larger and accumulative as MSB capacitance increases. The error induced by the LSB DAC capacitor mismatch is much less than the quantization and hence is negligible. Thus, we only need to calibrate the last 3 MSB DAC capacitor's mismatch (64C to 16C). The MSB DAC incorporates a redundant capacitor (8C) whose value is equal to the summation of all the capacitors in the LSB DAC. This capacitor provides a sufficient redundancy required by the calibration. It also facilitates the sampling of the input signals.

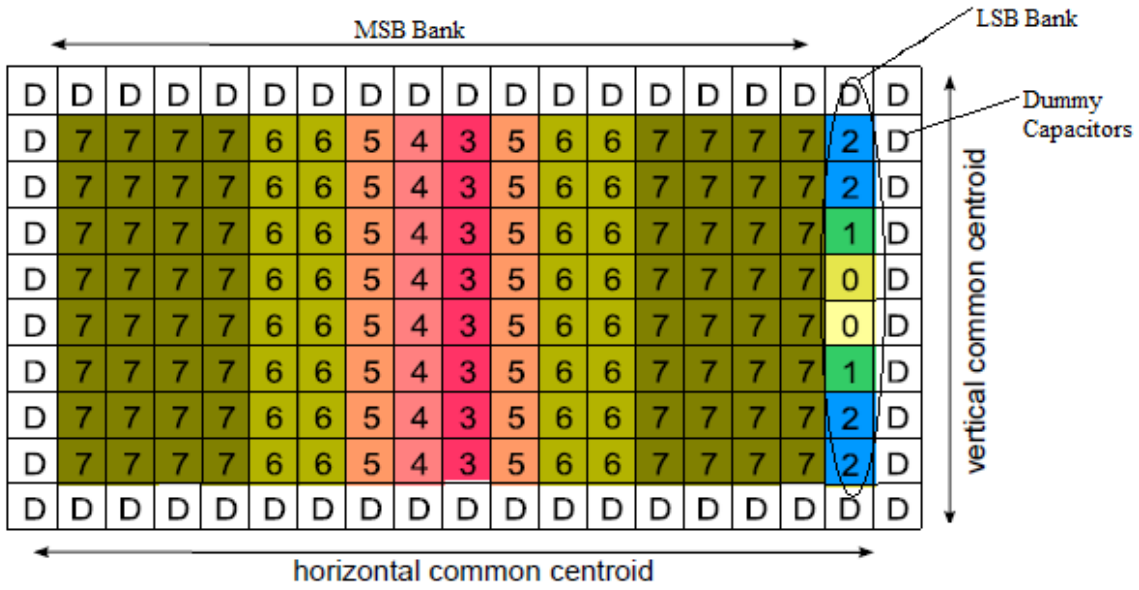


Figure 2.20: Floorplan of DAC capacitor array

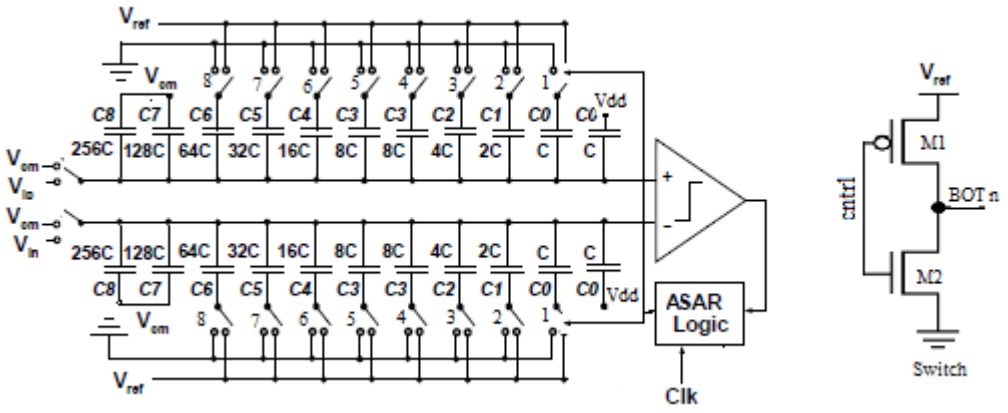
Table 2.3: Parasitic Extracted (PEX) capacitances from layout

Capacitor	PEX Value	Ratio ($\frac{\text{BOT N}}{\text{BOT 0}}$)	Error (LSB)
BOT 0	1.75065 fF	1	0
BOT 1	3.50285 fF	2.00088	0.00088
BOT 2	7.00839 fF	4.0033	0.0033
BOT 3	14.0797 fF	8.0425	0.0425
BOT 4	14.0797 fF	8.0425	0.0425
BOT 5	28.1593 fF	16.085	0.085
BOT 6	56.318 fF	32.169	0.169
BOT 7	112.566 fF	64.2995	0.2995

2.4.3.2 DAC Switching Circuit

With conventional switching scheme, the DAC settling time is limited by the MSB capacitor. As switch size is increased (to decrease Ron – Lower settling time), the increase in nonlinear parasitic capacitances of the switch significantly affect SNDR. Hence, to avoid

this limitation, variable switches of similar ratios are used for the binary capacitor array as shown in Fig. 2.21(a). The switching logic resembles a simple inverter as shown in Fig. 2.21(b). The transistor sizes of the switching array is presented in Table 2.4. As the width is increases, the driving strength of switching logic also increases to support increased capacitive load.



(a) (b)

Figure 2.21: (a) DAC switching array – ASAR ADC (b) DAC switch Implementation

Table 2.4: Sizing of DAC switching array

Switch	PMOS - M1 (W/L)	NMOS - M2 (W/L)
1	300n/40n	150n/40n
2	300n/40n	150n/40n
3	600n/40n	300n/40n
4	1.2u/40n	600n/40n
5	1.2u/40n	600n/40n
6	2.4u/40n	1.2u/40n
7	4.8u/40n	2.4u/40n
8	9.6u/40n	4.8u/40n

2.4.3.3 Sequencer - Implementation

To avoid using an external high-frequency clock generator for SAR operation, the proposed ADC uses an asynchronous control circuit to internally generate the necessary clock signals. Fig. 2.22 shows a schematic of sequence generator for Asynchronous SAR ADC and a timing diagram of the asynchronous control logic. The valid signal from the comparator triggers the sequencer. Clk1-Clk8 represent the sequence of 8 comparison cycles as shown in Fig. 2.23 and serve as control signals for DAC switching.

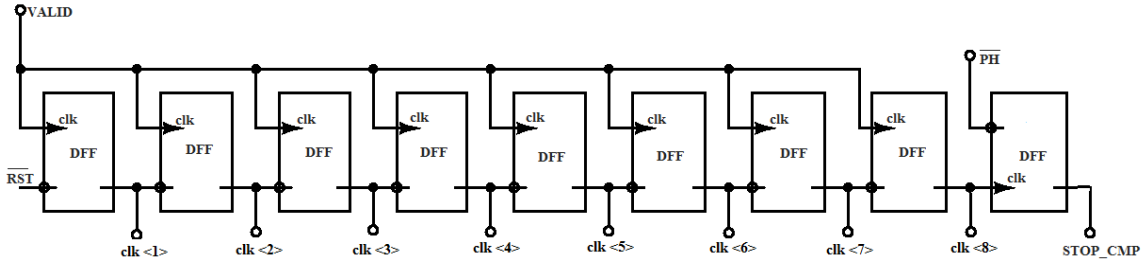


Figure 2.22: Sequencer circuit implementation

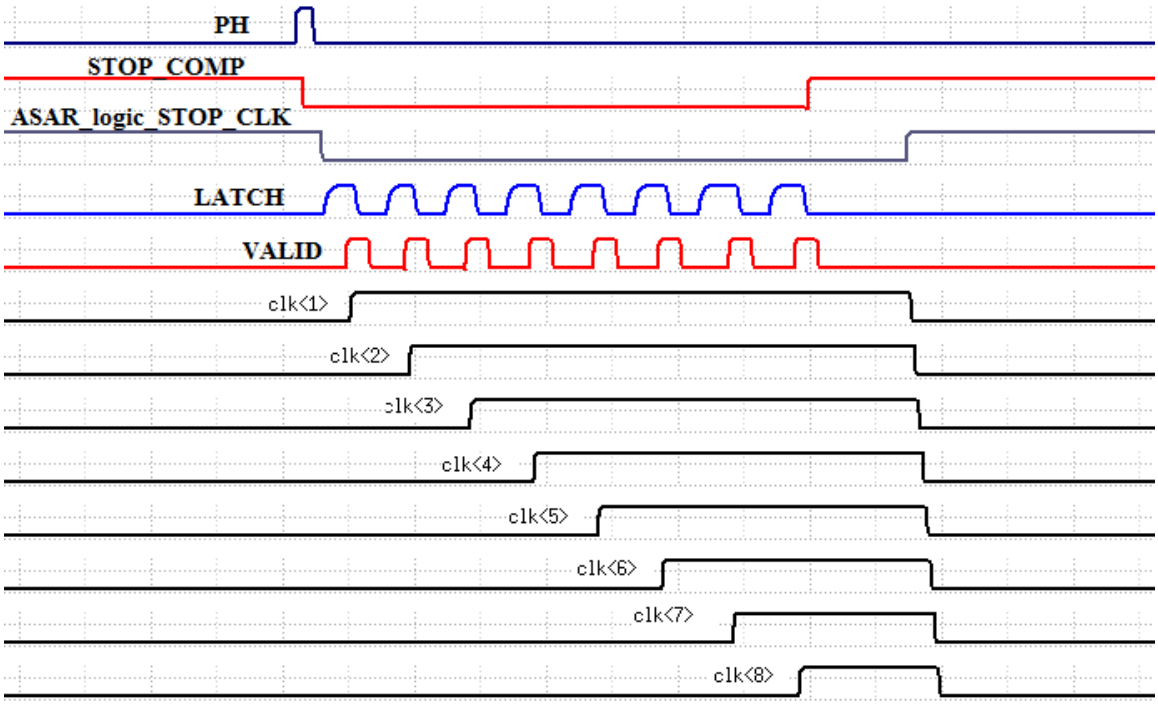


Figure 2.23: Timing diagram of Asynchronous SAR ADC

2.4.4 Noise Shaping

Though this section briefly discusses the 2nd order passive Noise Shaping technique, it can be understood in more detail from chapter - 2 of [51]. The performance of SAR architecture is limited by comparator noise, DAC mismatch, settling errors and $\frac{KT}{C}$ noise. These issues can be resolved by using noise shaping techniques for DAC's residual voltages after asynchronous SAR operation. Noise-shaping is conventionally implemented by using FIR filter and IIR filter, as shown in Fig. 2.24 [52]. FIR filter is based on two capacitor banks which are used to sample the residue voltages where as IIR filters are based on Operational amplifier (opamp) that acts as an active integrator to realize noise shaping function. This is not an attractive technique as the FIR filter not only introduces extra noise but also increases the ADC's area and power consumption. In addition, opamp based integrator is hard to scale and its design becomes difficult with technology and supply voltage scaling [53].

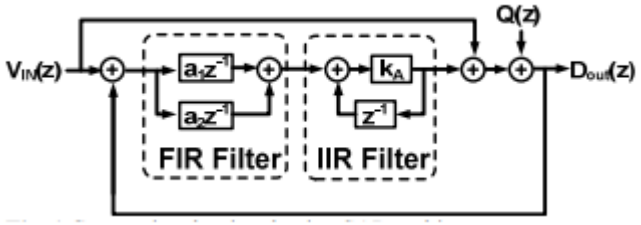


Figure 2.24: Conventional Noise Shaping Architecture [53]

Hence a fully passive noise shaping is employed to solve the issues of comparator noise, DAC mismatch and settling error. The noise-shaping technique presented provides a means to enhance the resolution of SAR ADCs without a significant modification to the basic SAR ADC structure. Additionally, this passive implementation has high power efficiency and is compatible with low voltage operation and CMOS technology scaling as it largely consists of digital circuits.

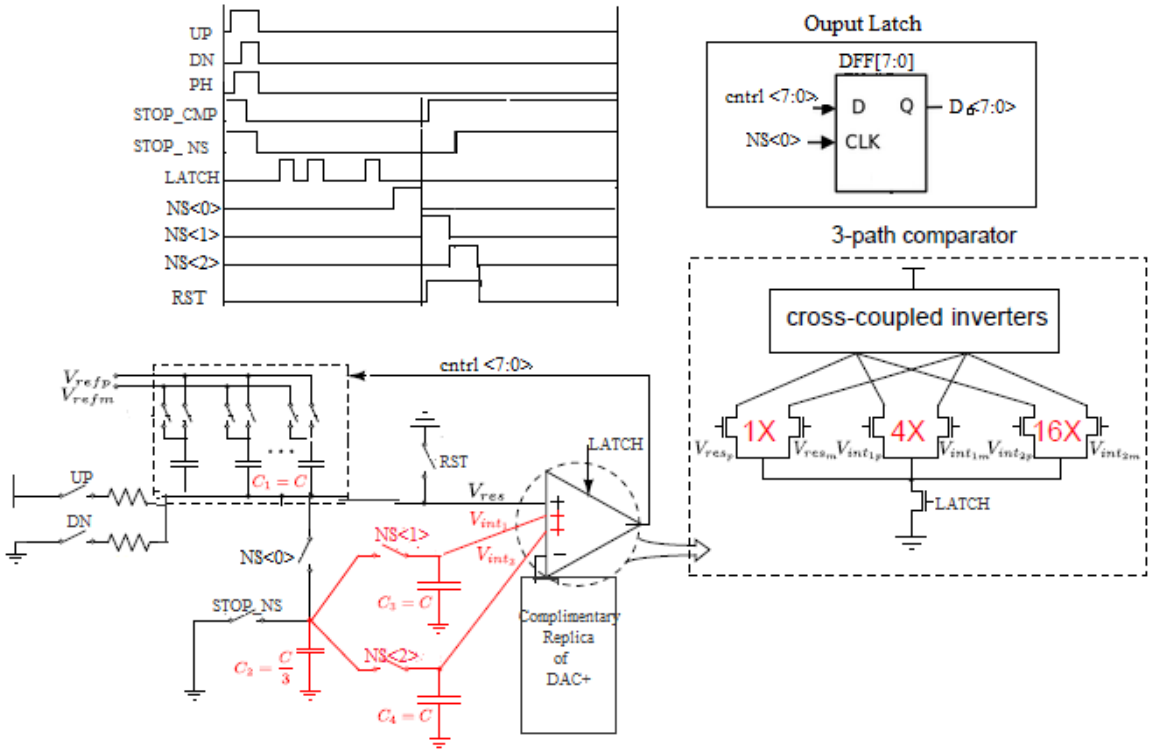


Figure 2.25: 2nd order passive Noise Shaping Architecture and Timing

This 2nd order passive-noise shaping technique implemented from [54-55]. After the end of ASAR operation, the residue voltage left on the top-plate of capacitive DAC has all the ADC error information, including quantization noise, comparator noise, and DAC mismatch and settling error. To realize 1st-order noise shaping, the key is to integrate the residual voltage V_{res} and feed it back to the comparator input before next noise shaping conversion begins. During NS<0> cycle, $C_2 = \frac{C}{3}$ is merged with the DAC capacitor, C1 = C and at the end of NS<0> cycle, C_2 will carry $0.75V_{res}$. This is followed NS<1> cycle, where C_2 dumps its charge onto another capacitor, C_3 = C, effectively realizing a passive 1st order integration resulting in voltage V_{int1} which is connected to 4X comparator input path. This is further followed by NS<1> cycle, where C_3 dumps its charge onto another capacitor, C_4 = C, effectively realizing a passive 2nd order integration resulting in voltage V_{int2} which is connected to 16X comparator input path. The comparator has 3- inputs paths

sized so as to provide relative gain among V_{res} , V_{int1} and V_{int2} respectively to compensate for the attenuation of V_{res} due to passive integration only a fraction of V_{res}. From the timing diagram in Fig. 2.25, RESET is enabled and comparator is disabled (STOP_CMP goes high) after NS<0> goes low which marks the acquisition of $0.75V_{res}$. Also as NS<0> goes high, the output bits [7:0] of comparator that are stored in strong-arm latch array as in Fig. 2.16 are processed to output latch for digital output bits D[7:0] – Fig. 2.25. This signifies that Noise shaping cycles doesn't consume additional time and happen simultaneously with Output Latch and RESET operation of TDC.

2.4.5 Simulation results of ADC Backend

The timing signals generated from the transistor level implementation of the backend is shown in Fig, 2.26.

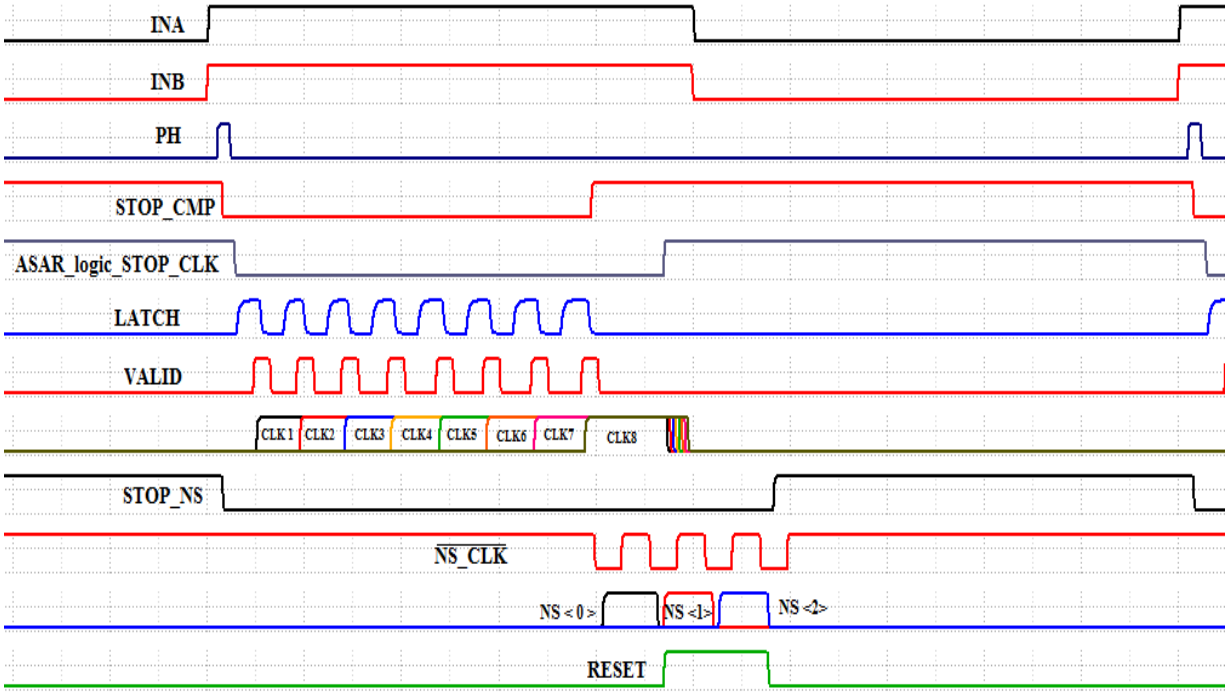


Figure 2.26: Timing signals for the simulations of TDC

The output spectrum of ASAR backend both RC compensated is shown in Fig. 2.27. The spectrum represents 256 point FFT of the digital output at a sampling rate of 100 MHz and an input frequency of $\frac{300}{256}$ MHz for voltage domain sinusoidal signal. The SNDR is 80.35 dB for an Oversampling ratio (OSR) of 8 as in Fig. 2.28 corresponds to an ENOB of 13.1 bits. The 3rd and 5th order harmonics are low enough not to impact the linearity. These simulation results are for full scale range of ADC - 2.2 V, i.e. 10 latch cycles for ASAR architecture and MSB capacitors (256C & 128C) are connected to BOT 8 and BOT 9 resulting in 2 extra MSB bits.

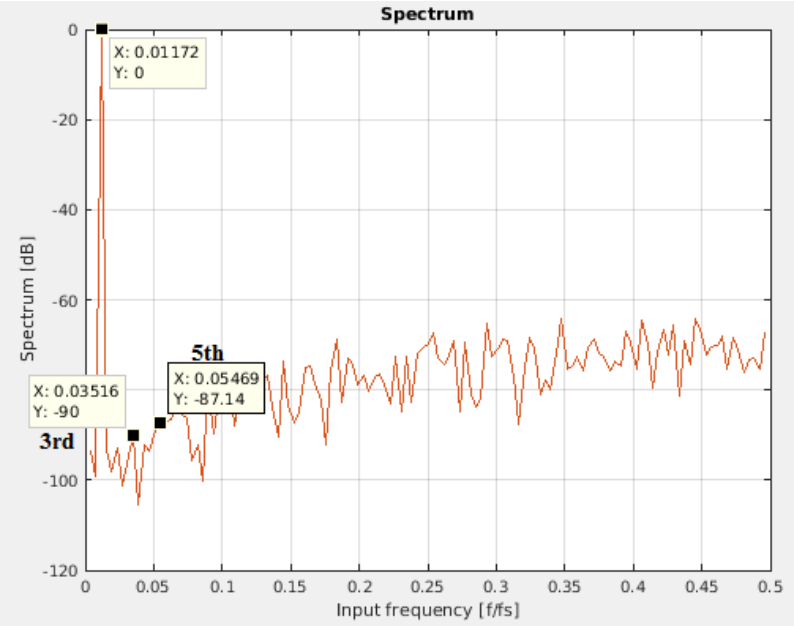


Figure 2.27: Output Spectrum of ADC Backend

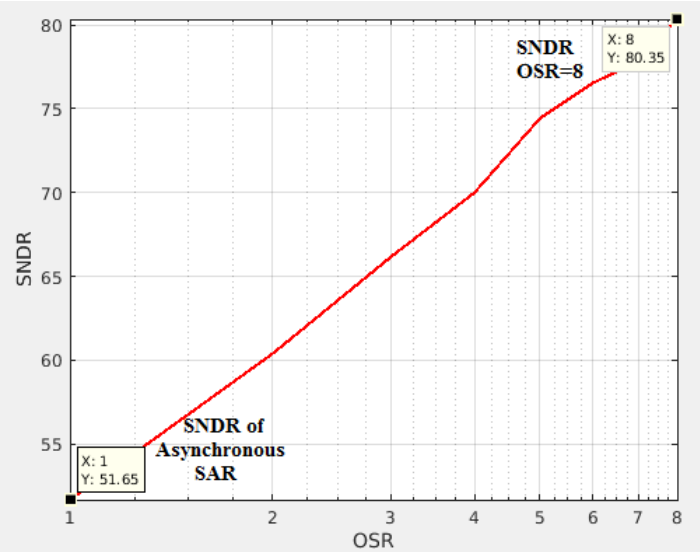


Figure 2.28: SNDR vs OSR

The DNL- INL plots for uncompensated and compensated digital output is shown in the Fig. 2.29. This simulations are run for ideal TAC frontend followed by ASAR ADC backend. The plot corresponds to time domain ramp signal with step of 0.25 ps and range of 100ps. The uncompensated values represent differential voltage output of TDC and RC compensated values represent TDC output reverse mapped to time domain from equation as described in section - . DNL corresponds to 0.1377/-0.1317 LSB and INL corresponds to 0.1641/-0.1472.

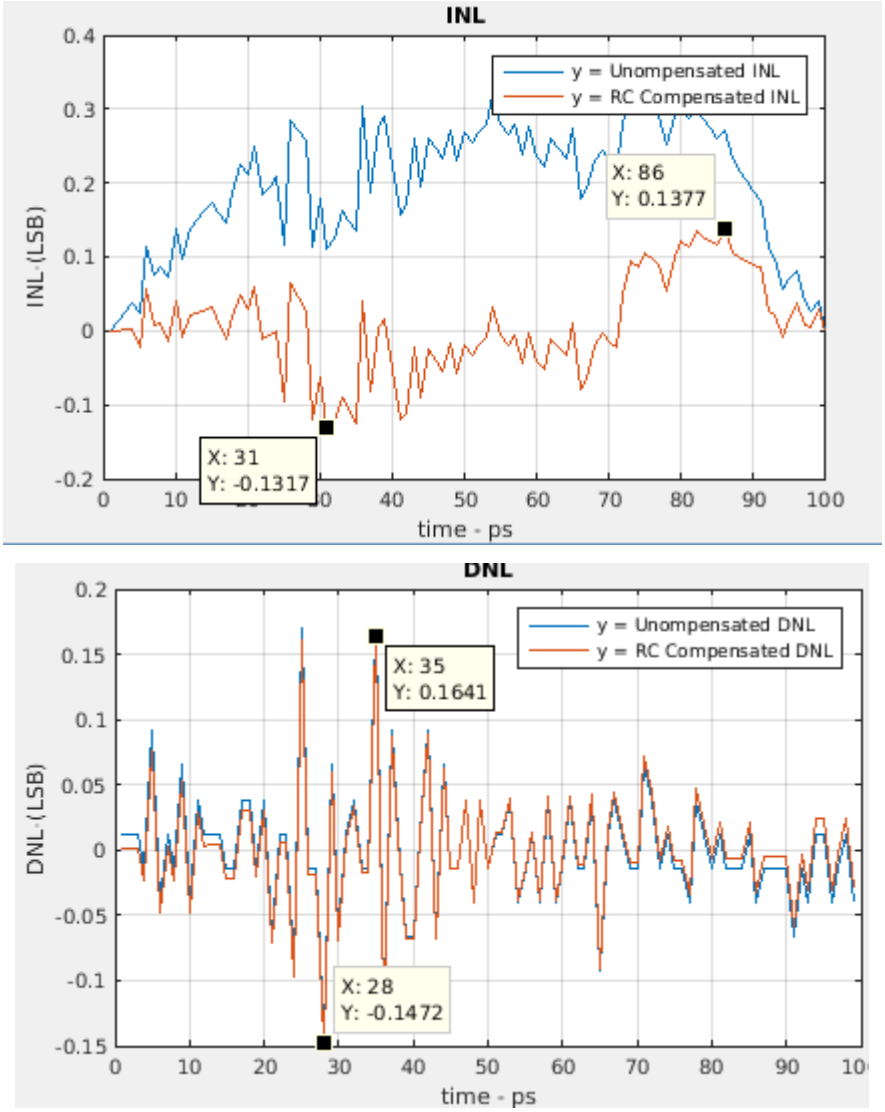


Figure 2.29: INL/DNL plots for Asynchronous SAR ADC with ideal TAC

2.5 Performance Evaluation of TDC

This section presents the simulation results of TDC. The output spectrum with noise and without noise is shown in Fig. 2.30. The spectrum represents 256 point FFT of the differential output voltage of TAC for a sampling rate of 100 MHz and an input frequency of $\frac{300}{256}$ MHz for time domain sinusoidal signal with peak-peak amplitude of 200ps. The SNDR from TDC with noise enabled and without noise enabled after an OSR of 8 is 58.78

from Fig. 2.31 which is further incremented by 20dB to compensate for input voltage range reduction from 2.2 V to 200 mV. Hence, the overall SNDR of TDC with noise enabled and without noise enabled is 78.78 dB and 84.14 dB respectively. After thermal noise is enabled, the SNDR drops from 84.14 dB to 78.78.dB by 6 dB. This corresponds to σ_{noise} of around 0.176 mV, which is smaller than target 0.25 mV (LSB). Hence the target performance of 0.25 ps resolution is achieved.

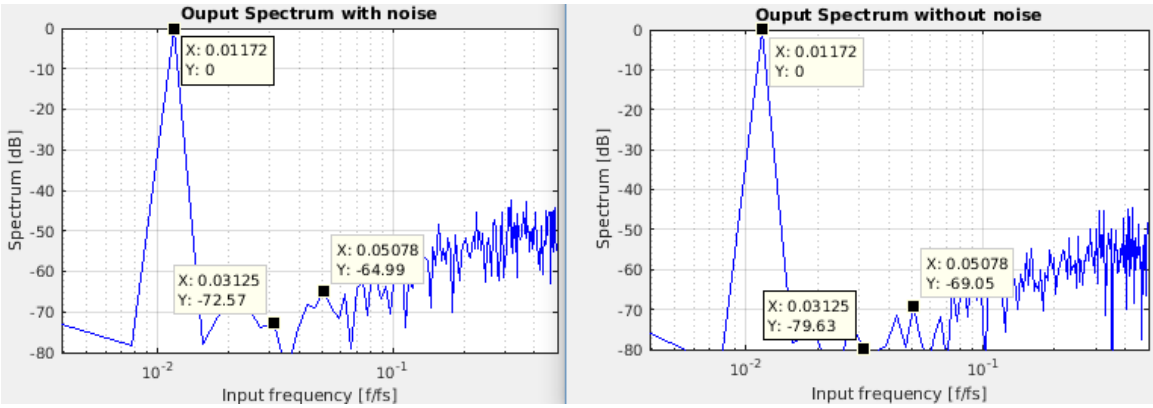


Figure 2.30: Output Spectrum TDC with noise enabled and without noise enabled

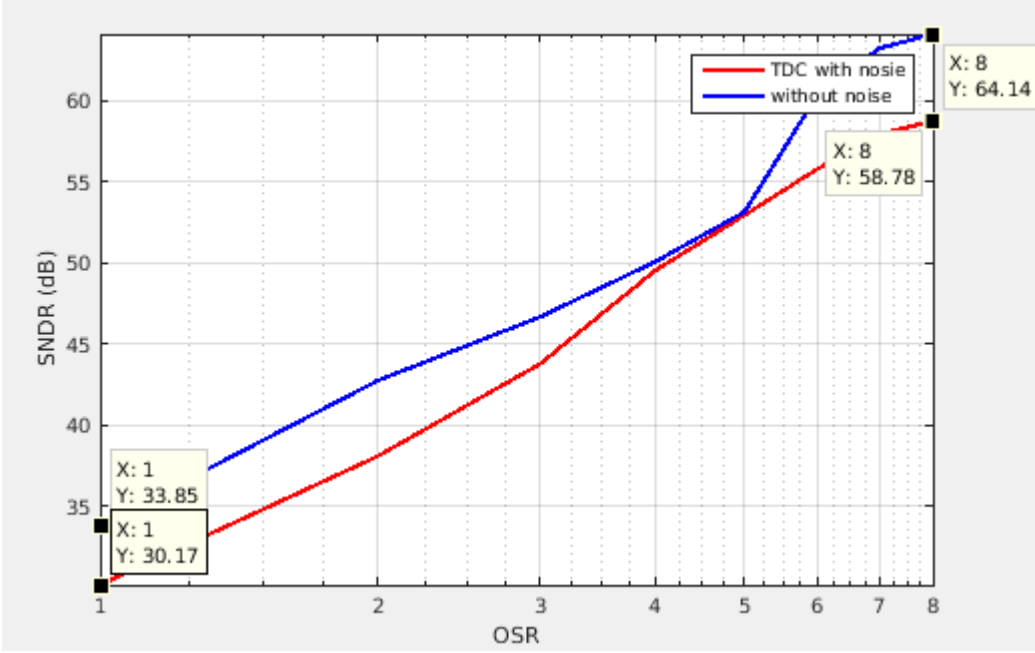


Figure 2.31: SNDR vs OSR with noise & without noise

The total power consumption of TDC is 0.32 mW which corresponds to an FOM of only 12.5 fJ/conv. The power breakdown with respect to various blocks is illustrated in Fig. 2.32. NS_TriCMP represents 3-path input comparator and capacitors for noise shaping and it consumes highest power due to large size input path transistors for gain compensation.

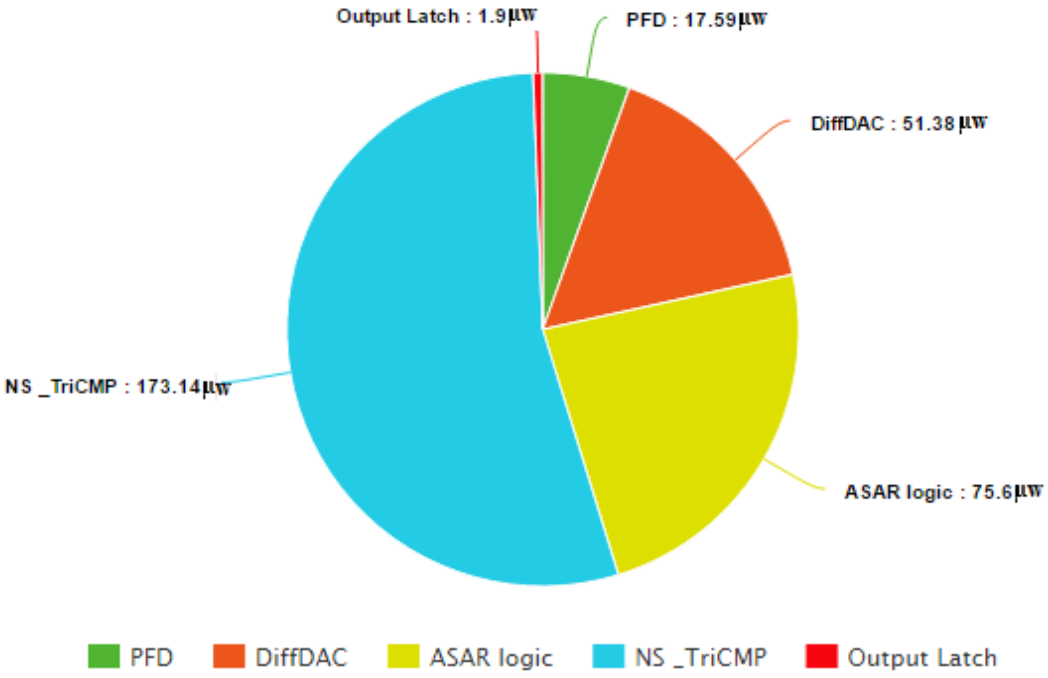


Figure 2.32: Power Breakdown of TDC

Though the targeted range of 200ps is achieved, the dynamic range can go beyond 200ps until the TDC is saturated. Theoretically, an approximate limit on range is evaluated. Due to reduction of 2 MSB cycles, range detectable by ADC backend is reduced from 2.2 V to 550 mV (V_{swing_ADC}) which corresponds to $t_{max} - 250\ ps$ ($V_{swing\_TAC} \approx \pm 250mV$). Thus, theoretically the range might go beyond 200 ps until 500 ps, though this not yet tested. The bandwidth of TDC represents the maximum input signal frequency (in time-domain) as in rate of change in the phase error. It can also be termed as conversion rate. For this ADC,

since ASAR conversion rate is more than sampling rate, the bandwidth is determined by noise shaping i.e., $\frac{f_s}{2*OSR}$ = 6.25 MHz.

Table 2.5: Performance Metrics

Technology	40 nm CMOS
Supply	1.1 V
Bits	13
SNDR	84.14 dB
Resolution	0.25 ps
Sampling Rate	100 Ms/s
Conversion Rate	6.25 Ms/s
FOM	12.5 fJ/conv
Type	SAR

2.6 Key Aspects - Post Layout

Some key considerations are made during and after layout especially for processing post simulation data.

- For layout, symmetry was ensured between the positive and negative differential side of TAC in order to reduce the offset or any gain error. Though, any kind of mismatch can be resolved by digital calibration or offset cancellation techniques.
- DAC mismatch errors can result in non-linearity for the TDC. This was resolved by iterated common centroid layout for the CRT-MOM capacitor array until the variations among parasitic extracted values are less than $\frac{\Delta}{4}$ as discussed in section - .However, digital calibration is employed to account for any post layout mismatches especially between MSB capacitors (BOT 7, BOT 6 & BOT 5) and LSB capacitors – unit capacitances.
- Though a resolution of 0.25 ps is achieved by schematic and even post layout, σ_{res} should be less than 0.25 ps over PVT variations. This can be accomplished by

dynamic offset cancellation techniques at the TAC front end and foreground calibration for a DAC mismatch variations.

- It's observed that for post layout simulations, the sampling rate was reduced from 100 MHz to roughly 50-60 MHz due to increased loading of parasitic capacitances. Resolution and range are not affected. This is not a big deal with respect to high bandwidth PLL applications like frequency synthesizer as the divider ratio can be modulated to produce sufficiently high frequencies.

Based on brief discussions throughout this report, an approximate comparative study of the popular current state of art TDC architectures and the proposed design is presented qualitatively in the Table 2.6.

Table 2.6: Qualitative summary of various TDCs including proposed work

Architecture	**Vernier**	**Pipeline**	**Interpolating**	**Oversampling**	**Cyclic**	**Stochastic**	**This work**
Resolution	medium	high	low	medium	high	low	highest
Range	medium	medium	high	high	medium	medium	medium
Speed	medium	high	high	low	low	high	medium
Power	medium	high	medium	medium	low	medium	low
Scaling Compatibility	high	medium	medium	low	high	high	high
Area	medium	high	high	high	low	medium	low

Chapter 3: Conclusion

This report presents the design and development of highest resolution TDC among the current state of art architectures with reasonable dynamic range of 200 ps and maybe also beyond. This report started with an initial background and motivation behind high resolution TDCs. A brief overview of current popular TDC architectures and their limitations are presented and a comparative study with respect to resolution in particular among the best performances of these architectures is made. A brief discussion of [46] is made from which the 2^{nd} order Noise Shaping ASAR based TDC architecture is inspired. This TAC + 2^{nd} Order Noise shaped ASAR architecture is implemented in 40nm CMOS technology and achieves a resolution of 0.25 ps, a dynamic range of 200ps and FOM of only 8 fJ/conv. Various key aspects for layout and calibration techniques for post layout are briefly discussed. The limitation of this design is tradeoff among resolution and range which is ubiquitous among most of the architectures discussed. This can be addressed by digitally configurable DAC capacitor array. This technique brings in the flexibility of increasing dynamic range at the expense of resolution by adding more MSB capacitors – bits. Thus, apart from high bandwidth PLLs this architecture has unbounded possibilities of applications with respect to particle physics, PET , digital oscilloscopes , time domain ADCs etc., as high dynamic range and as well as resolution can be achieved.

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