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Design and Implementation of Radix-3/Radix-2 Based Novel Hybrid SAR ADC In Scaled CMOS Technologies

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Design and Implementation of Radix-3/Radix-2 Based Novel Hybrid SAR ADC In Scaled CMOS Technologies

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Dedicated to my parents, my wife and our lovely daughter Amelia.

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Design and Implementation of Radix-3/Radix-2 Based Novel Hybrid SAR ADC In Scaled CMOS Technologies

Md. Manzur Rahman, Ph.D.
The University of Texas at Austin, 2017

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This thesis focuses on low power and high speed design techniques for successive approximation register (SAR) analog-to-digital converters (ADCs) in nanoscale CMOS technologies. SAR ADCs' speed is limited by the number of bits of resolution. An N-bit conventional SAR ADC takes N conversion cycles. To speed up the conversion process, we introduce a radix-3 SAR ADC which can compute 1.6 bits per cycle. To our knowledge, it is the first fully programmable and efficiently hardware controlled radix-3 SAR ADC. We had to use two comparators per cycle due to ADC architecture and we proposed a simple calibration scheme for the comparators. Also, as the architecture of the DAC array is completely different from the architecture of conventional radix-2 SAR ADC's DAC arrays, we came up with an algorithm for calibration of capacitors of the DAC.

Low power SAR ADCs face two major challenges especially at high resolutions: (1) increased comparator power to suppress the noise, and (2) increased DAC switching energy due to the large DAC size. Due to our proposed architecture,

the radix-3 SAR ADC uses two comparators per cycle and two differential DACs. To improve the comparator's power efficiency, an efficient and low cost calibration technique has been introduced. It allows a low power and noisy comparator to achieve high signal-to-noise ratio (SNR).

To improve the DAC switching energy, we introduced a radix-3/radix-2 based novel hybrid SAR ADC. We use two single ended DACs for radix-3 SAR ADC and these two single ended DACs can be used as one differential DAC for radix-2 SAR ADC. So, overall, we only have a single DAC as conventional radix-2 SAR ADC. In addition, a monotonic switching technique is adopted for radix-2 search to reduce the DAC capacitor size and hence, to reduce switching power. It can reduce the total number of unit capacitors by four times. Our proposed hybrid SAR ADC can achieve less DAC energy compared to radix-3 and radix-2 SAR ADCs. Also, to utilize technology scaling, we used the minimum capacitor size allowed by thermal noise limitations. To achieve high resolution, we introduced calibration algorithm for the DAC array.

As mentioned earlier, the radix-3 SAR ADC offers higher power than conventional radix-2 SAR ADC because of simultaneous use of two comparators. In the proposed hybrid SAR ADC, we will be using radix-3 search for first few MSB bits. So, the resolution required for radix-3 comparators are much larger than the LSB value of 10-bit ADC. By implementing calibration of comparators, we can use low power, high input referred offset and high speed comparators for radix-3 search. Radix-2 search will be used for rest of the bits and the resolution of the radix-2 comparator has to be less than the required LSB value. So, a high power,

low input referred offset and high speed comparator is used for radix-2 search. Also, we introduced clock gating for comparators. So, radix-3 comparators will not toggle during radix-2 search and the radix-2 comparators will be inactive during radix-3 search. By using the aforementioned techniques, the overall comparator power is definitely less than a radix-3 SAR ADC and comparable to a conventional radix-2 SAR ADC.

A prototype radix-3/radix-2 based hybrid SAR ADC with the proposed technique is designed and fabricated in 40nm CMOS technology. It achieves an SNDR of 56.9 dB and consumes only 0.38 mW power at 30MS/s, leading to a Walden figure of merit of 21.5 fJ/conv-step.

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Chapter 1

Introduction

1.1 Motivation

In modern life, electronic equipments are frequently used in different fields such as communication, transportation, entertainment, etc. Modern electronic systems store and process information in the digital domain. Analog to digital converters (ADCs) and digital to analog converters (DACs) are very important components in electronic equipment. Since most real world signals are analog, these two converting interfaces are necessary to allow digital electronic equipments to process the analog signals. For example, in wireless system, ADCs and DACs should support a wide bandwidth with high resolution which depends on the actual application. Current 5G cellular systems require a resolution of 12 bits or above with a wide spur free dynamic range and low power [Roh et al. [2014]]. The signal processing system is a crucial block in wireless communication and ADCs play vital role to improve the performance of this block. To process signals with pure analog circuits is not cost effective and it has long development cycle time. On the other hand, digital signal processing (DSP) provides a cheaper solution with fast development cycle and at a much lower cost. To take advantage of such features, analog signals have to be converted to digital signals in an early stage of the processing chain, making the analog-to-digital converter a critical design block. It also needs to be

mentioned that, the overall signal processing performance primarily depends on analog-to-digital converter's performance, signal to noise ratio, speed and power. So, in the modern world, ADCs and DACs play a crucial role in digital signal processing.

Moore's law continues to predict the scaling of complementary metal-oxide-semiconductor (CMOS) and levels of integration fairly well and the rate of scaling even outperforms the prediction in recent years [Chou [2005]]. ADCs can exploit the benefits of continuous technology scaling, and can be improved in terms of speed, power efficiency and integration with electronic systems. Now-a-days, the state-of-the-art demands continuous development in high-performance and low power data converters to allow more signal processing to be done in the digital domain in order to take full advantage of tremendous DSP power as it improves steadily with process scaling.

Moreover, todays portable devices including smart phones, netbooks, tablets, GPS, portable gaming platforms, etc. promise consumers the rich and satisfying experience that they have come to expect and demand. To keep pace with consumers expectations, portable devices have to provide not only high performance, but also good power efficiency. As all the portable devices are battery powered, lots of design efforts have been invested in long battery life. This current trend creates a number of challenges to achieve high performance, high resolution and low power ADC in the same design, especially in the deeply scaled CMOS technologies.

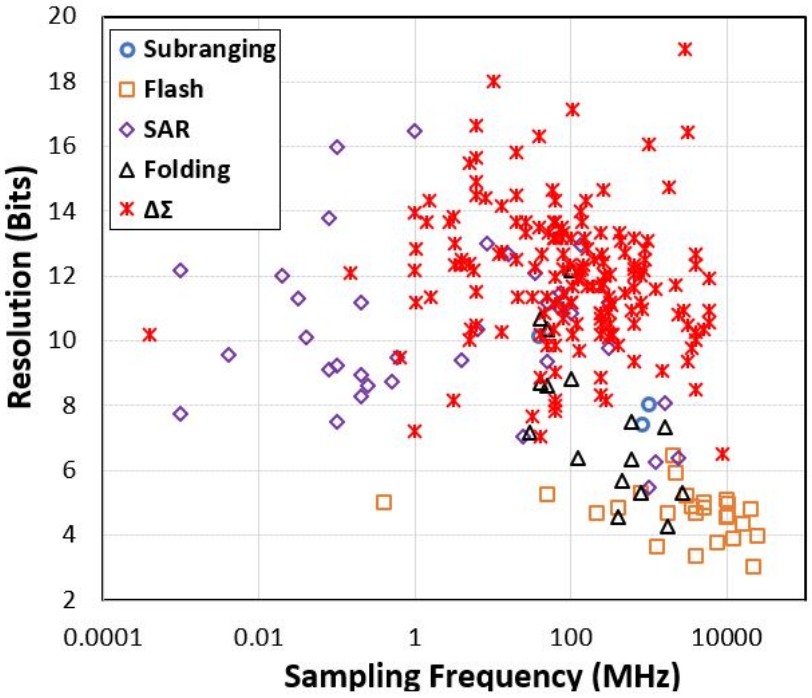


Figure 1.1: Sampling frequency versus resolution plot for recently published ADCs in ISSCC and VLSI conferences.

1.2 ADC Architecture Overview

Application of any ADC is decided by it's speed, resolution and overall performance. ADC's resolution versus sampling frequency is shown in Fig.1.1 for all of the ADCs published in leading technical conferences (ISSCC and VLSI) between 1997 and 2017 [Murmann]. It shows that the number of bits decreases with the increment of sampling frequency. The plot also shows that flash and folding ADCs are good candidates for high sampling frequency, but with the low resolution. $\Delta\Sigma$ converters dominate the high resolution and low sampling frequency region. Successive-approximation-register (SAR) converters are applicable for low-

to-medium speed and medium-to-high resolution applications, and pipelined converters are used for medium-to-high speed and resolution.

The flash topology has been the popular choice for high-speed and low-resolution applications, but it suffers from a number of drawbacks. The number of comparators grows exponentially with the resolution. So, the area and power grows accordingly and also, it introduces some other design concerns for comparators such as large input loading and kickback noise. As a result, accuracy of references voltage and as well as speed of the ADC gets degraded. For these difficulties, flash ADCs can not be used for high speed and high resolution data conversion.

Pipelined ADCs are traditionally used for medium-to-high speed and resolution applications. Unlike flash ADCs, the hardware requirement of pipelined ADCs scales linearly with the number of bits. Another major advantage of this architecture is that the resolution of the overall pipelined ADC can be increased by adding an extra pipeline stage. The parallelism enables high throughput at the cost of extra power consumption and latency. Another issue with this architecture is, we have to use operational amplifiers to amplify the residue from the previous stage to the next stage, which requires large gain and bandwidth. However, in scaled CMOS technologies, with scaled power supply, it is hard to achieve the required performance of the op-amp.

$\Delta\Sigma$ converters are traditionally used for high resolution, low bandwidth digital audio applications. $\Delta\Sigma$ converters trade speed for resolution. In order to perform noise shaping, it samples the input much faster than the Nyquist rate. Advancement of technology has recently demonstrated that $\Delta\Sigma$ can achieve improved

speed at a few megahertz samples per second [Shettigar and Pavan [2012]] and [Srinivasan et al. [2012]]. Unlike nyquist rate ADCs, the internal circuits have to run at speed much faster than the sampling rate and the power consumption can be significantly higher.

Successive-approximation-register (SAR) ADCs were introduced in 1975 by [McCreary and Gray [1975]] and have been extensively used for medium-speed applications. SAR ADCs are a popular choice due to the simple architecture and short development cycle. They are more digital friendly and do not require any opamps compared to pipeline ADCs or $\Delta\Sigma$ ADCs. A conventional SAR ADC includes a digital-to-analog converter (DAC), dynamic comparator and digital logic block. The DAC is typically composed of binary-weighted capacitors, which also serve as the input sampling capacitor. After sampling the input signal, the digital logic block sends code to the DAC so that it can perform a binary search. The output terminals of DAC are connected to dynamic comparator. The comparator makes a decision based on the residue voltages generated by the DAC and sends it to the digital logic block. Then the logic block performs a binary search and creates the correct digital output bits to minimize the difference between voltage on the DAC and analog input. The architecture has very high energy efficiency as the internal blocks only consume dynamic power. Digital scaling helps improve the speed of CMOS technologies and therefore, it is making SAR a viable option for higher speed applications. Moreover, because of its highly digital nature, scaling issues affecting other architectures are not present in SAR ADCs.

The fundamental factor that limits SAR ADCs' speed is the number of com-

parison cycles needed to complete a full conversion process [McCreary and Gray [1975]] and [Johns and Martin [1999]]. For a conventional radix-2 SAR ADC, the capacitor will be switched to one of the two reference voltages V_{refp} or V_{refn} at the end of every comparison cycle, and it only updates one binary bit to the output per comparison cycle. Thus, for an N-bit radix-2 ADC, it takes N comparison cycles to complete a full conversion.

In this thesis, we present a new radix-3 SAR ADC that can resolve a ternary bit each comparison cycle. For the same target resolution, our architecture is 1.6 times faster than conventional SAR ADC. Instead of binary search, we perform ternary search in our proposed architecture and hence, it requires 40% fewer comparison cycles. To achieve this performance, we use two dynamic comparators instead of one. Also, we modified the DAC architecture to perform ternary search. The ratio between adjacent capacitors is changed to three instead of two in the conventional radix-2 SAR ADC. We also need another voltage V_{cm} is used as the third reference voltage besides V_{refp} and V_{refn}. By doing this, we get $log_2 3 \approx 1.6$ binary bits each comparison cycle.

Though the radix-3 SAR ADC is a good candidate for high resolution and high speed data conversion, it is not applicable for medium to low power applications. For this reason, we came up with a modified architecture that can fit in medium to low power and high resolution applications. We propose a novel hybrid SAR ADC which uses single ended radix-3 search for first few bits and differential radix-2 search for rest of the least significant bits (LSB). Overall, we are using only one DAC similar as radix-2 SAR ADC. Though we will be using three com-

parators (two comparators for radix-3 search and one for radix-2 search), radix-3 search provides fast convergence rate and requires low-resolution and low-power comparators. Differential radix-2 search mitigates the effect of comparator offset with comparator of higher resolution and higher power. We introduce clock gating of the comparators and radix-3 comparators will be much lower power than radix-2 comparators, overall, only single comparator power is consumed. Another challenge for low power and high resolution SAR ADC design is to reduce the DAC switching energy. The DAC is commonly implemented with binary capacitors in SAR ADCs. To suppress the sampling kT/C noise and provide good matching accuracy in high resolution designs, the capacitive DAC needs to be large, leading to a significant power consumption out of the total ADC power. Using an efficient switching scheme [Sanyal and Sun [2014]] during radix-2 search and clock gating among low and high power comparators, the proposed hybrid ADC maintains both accuracy and efficiency in power and speed. ADC linearity highly depends on capacitor matching. In this thesis, to reduce capacitor mismatch, a fully digital calibration method has been proposed which does not require any extra capacitor DAC.

1.3 Organization

This thesis is organized as follows: Chapter 2 of the thesis presents the radix-3 architecture of the SAR ADC. It includes the radix-3 algorithm, characterization and description of circuit level design. It also includes the calibration technique of the capacitor array of radix-3 SAR ADC. Chapter 3 presents the radix-

3/radix-2 hybrid SAR ADC. It includes characterization, comparison and circuit level implementation. Capacitor calibration of the DAC and offset calibration of comparators have also been discussed here. Chapter 4 describes the chip measurement results of the prototype designed in 40nm CMOS process. Conclusions are drawn in Chapter 5.

Chapter 2

Radix-3 SAR ADC

This chapter [1] presents a new radix-3 successive approximation register (SAR) analog-to-digital converter (ADC). Our proposed radix-3 SAR ADC can generate $1.6N$ binary bits during N comparison cycles. The radix-3 SAR ADC is 60% faster than the conventional radix-2 SAR ADC. Our prototypes are designed with 4- and 7-ternary-bits using 180nm CMOS technology. They can achieve a signal-to-quantization-noise ratio (SQNR) of 39 dB and 66 dB which are equivalent to 6.2 and 10.7 binary bits respectively.

This chapter also presents a calibration technique for radix-3 successive approximation register (SAR) ADCs. The performance largely depends on the matching of capacitors in digital to analog converters (DACs). The effect of capacitor mismatches on signal-to-quantization-noise ratio (SQNR) is demonstrated and calibration technique is simulated in 180nm CMOS technology. This calibration tech-

[1] This chapter is a partial reprint of the following publications:
Manzur Rahman, Long Chen, and Nan Sun, "Algorithm and implementation of digital calibration of fast converging radix-3 SAR ADC," *IEEE* International Symposium on Circuits and Systems (*ISCAS*), pp.1336–1339, 2014. I did the modeling and design of the proposed idea.
Long Chen, Manzur Rahman, and Nan Sun, "A fast radix-3 SAR analog-to-digital converter," *IEEE* International Midwest Symposium on Circuits and Systems (*MWSCAS*), pp. 1148–1151, 2013.
I helped in modeling and designing of the proposed idea. I thank all the co-authors for their valuable advice in designing the prototype.

nique does not require any extra capacitor DAC and is programmable for any radix-3 SAR ADC. To prove the calibration concept, a 7-ternary-bit-radix-3 SAR ADC is designed which can achieve signal to noise and distortion ratio (SNDR) of 67 dB with up to 10% capacitor mismatch.

This chapter is organized as follows: an introduction of existing techniques is first presented. Then we revisit the existing radix-2 SAR ADC technique. After that, a detailed description of a radix-3 SAR ADC is presented. Later, we introduce several characterizations of our proposed radix-3 SAR ADC. Then, we describe the proposed algorithm for capacitor calibration of the radix-3 SAR ADC. Next, we go through detailed circuit level description. Finally, a SPICE simulation result is presented where the circuit was designed in 180nm CMOS process.

2.1 Introduction

Rapid advancement in wireless sensor nodes and biomedical devices place demanding requirements on low power and high resolution analog-to-digital converters (ADCs) [Verma and Chandrakasan [2007]], and [Van Helleputte et al. [2012]]. Due to its proven record of high energy efficiency, the successive approximation register (SAR) analog-to-digital converter (ADC) is a popular choice. SAR ADCs are reported to be among the lowest power consuming ADCs in literature because of minimum active analog circuit requirements [Hadidi et al. [1990]] and [Sauerbrey et al. [2003]].

SAR ADCs exploit the benefits of the ever-shrinking technology nodes and the high switching speed of nanometer CMOS processes. Improvements in gener-

ations of technologies make it possible to use SAR ADCs for video applications, where sample frequencies of at least 10 MSample/s are necessary[Kuttner [2002]]. SAR ADCs are a popular choice due to the simple architecture and short development cycle. It consists of only a capacitive DAC, a comparator, and a digital SAR logic. Due to highly digital nature and simple architecture, SAR ADCs do not consume any static power. As a result, they can achieve an excellent power efficiency of only a few femtojoule (fJ) per conversion step, especially at low resolution with a target effective number of bits (ENOB) below 10-bit [Tai et al. [2014]], and [Harpe et al. [2014]]. The operation speed of SAR ADCs has improved with the scaling of CMOS technology. With growing transistor bandwidth, a single-channel SAR ADC can achieve a sampling speed of up to a few hundred MS/s with a resolution of 8 to 12 bits [Huang et al. [2013]], and [Tsai et al. [2015]].

Despite many advantages of SAR ADCs, it is not possible to maintain a high power efficiency when extending the resolution above 10 bits. The fundamental factor that limits SAR ADC's speed is the number of comparison cycles needed to complete a full conversion process[McCreary and Gray [1975]]. For a conventional radix- 2 SAR ADC, the capacitor will be switched to one of the two reference voltages at the end of every comparison cycle, and it only updates one binary bit to the output per comparison cycle. Thus, for an N-bit SAR ADC, it takes N comparison cycles to complete a full conversion. Also, to reach higher signal-to-noise ratio (SNR), the comparator noise needs to be reduced. This can be achieved by increasing the transistor sizes and power. The other challenge for a high-resolution SAR ADC is its exponentially growing capacitive DAC size. For an N-bit SAR

ADC, it takes 2^N unit capacitors, which results in greatly increased DAC power. Facing these challenges, it is highly desirable to develop a more efficient way to increase SAR ADC resolution without significantly increasing the comparator power and the DAC size.

Recently, a radix-3 SAR ADC has been proposed in [Thirunakkarasu and Bakkaloglu [2010]], which is implemented with a large number of capacitors. In order to get N-ternary bits in a differential implementation, the number of capacitors is 4×3^N , which increases exponentially with number of bits. For example, to obtain 4 ternary bits, 4×3^4 = 324 capacitors are needed. This makes it difficult to use in high resolution applications since more capacitors leads to more hardware complexity and power consumption.

Another paper on multi-bit-per-cycle SAR ADC was presented in [Cao et al. [2009]] which converges 2-binary-bits/cycle. It used 3 differential structures. For N-binary bits, the number of capacitors is 6×2^N. It also uses a power hungry architecture which also limits the resolution.

In this chapter, we present a new radix-3 SAR ADC that can resolve a ternary bit (1.6 binary bits) on each comparison cycle. For the same target resolution, our architecture takes 40% less comparison cycles compared to conventional radix-2 SAR ADCs and thus, the speed is increased by 1.6 times. Key changes that we have introduced in our architecture are:

1. We use two comparators per comparison cycle and perform a ternary search instead of a binary search.

2. The ratio between adjacent capacitors is changed to three instead of two in the conventional radix-2 SAR ADC.

3. Another voltage V_{cm} is used as the third reference voltage besides V_{refp} or V_{refn}. By doing this, we get $\log_2 3 \approx 1.6$ binary bits on each comparison cycle. To get N ternary bits in our proposed radix-3 SAR ADC, the number of capacitors is $4 \times (N + 1)$, which increases linearly with N. Our ADC needs only 20 capacitors to get 4 ternary bits, which is more than 15 times reduction compared to [Thirunakkarasu and Bakkaloglu [2010]]. Also, to get 4 binary bits, [Cao et al. [2009]] requires 36 capacitors which is 1.8 times more than ours.

In order to get more binary bits per comparison cycle, the ratio of the adjacent capacitors needs to be exactly three times and the ADC performance is highly dependent on capacitor matching. To reduce capacitor mismatch, the DAC capacitor size is usually much larger than that needed from sampling noise considerations [Schreier et al. [2005]].

In this chapter, for the first time, a fully digital calibration method is presented for a radix-3 SAR ADC which does not include any extra capacitor DAC. Also, it reduces the minimum size requirement of the capacitors to maintain linearity and hence, reduce the dynamic power and area of the whole circuit.

To verify our idea, 4- and 7-ternary-bit radix-3 SAR ADCs were designed in 180nm CMOS process. Also, the capacitor mismatch was introduced in simulation and the proposed calibration scheme was verified by signal-to-noise-and-distortion (SNDR) value.

2.2 Conventional Radix-2 SAR-ADC Review

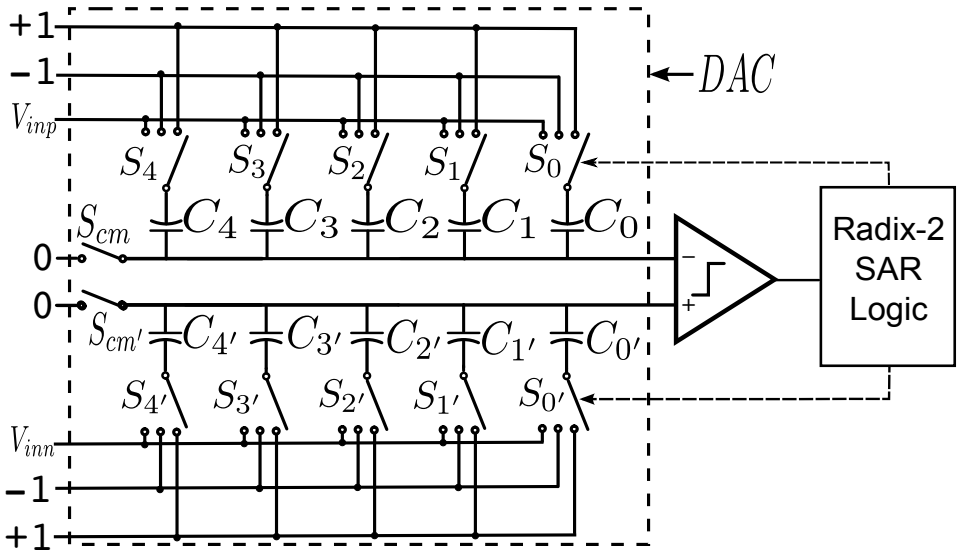


Figure 2.1: Architecture of the conventional radix-2 SAR ADC.

Fig. 2.1 shows the architecture of a conventional radix-2 SAR ADC. The capacitor values are chosen to be: $C_i = 2^{i-1}C_0$ for $i \in [1, N]$ and C_0 is the required unit capacitor of the DAC. By choosing this capacitor ratio, a binary search algorithm can be guaranteed due to $C_i = \sum_{j=0}^{i-1} C_j$. Since each DAC capacitor in the radix-2 SAR is connected to either V_{refp} or V_{refn}, only 1 binary bit is generated at the end of each comparison cycle. As a result, N binary weighted capacitors will only generate N bits of resolution after N comparison cycles in the conventional radix-2 SAR ADC, and total number of capacitors are 2×2^N. For example, to resolve 4 binary bits, 4 comparison cycles are needed and total capacitor count will be 32 (assuming unit capacitor value as 1). If we use D_i to represent the digital output of C_i, the final 4-bit digital output will be: $D_{out} = \sum_{i=1}^{4} 2^{i-1} D_i / 2^3$.

2.3 Proposed Radix-3 SAR ADC

2.3.1 Comparison Levels

To understand the architecture of any ADC, it is very important to review of the comparison levels. For that purpose, Fig.2.2 presents the comparison levels of the proposed radix-3 SAR ADC containing 3-ternary ($\approx$ 4.8-binary) bits. Assuming input voltage, $V_{in+} \in [-1, 1]$ and $V_{in-} \in [-1, 1]$, so $V_{in} \in [-2, 2]$. To resolve a ternary bit, the reference level has to be $2/3$ and $1/3$ of the input range as $\log_2 3 \approx 1.6$ binary bit. We will design the circuit in a way that it can generate the required reference levels for a radix-3 search algorithm. In first cycle, it is compared against $2/3$ and $-2/3$ which is $2/3$ and $1/3$ of the input voltage range respectively, and one ternary bit is resolved in cycle1. In cycle2, the residue voltage can be in any of three regions: $[-2, -2/3]$ or $[-2/3, 2/3]$ or $[2/3, 2]$. Depending on the decision of first cycle, the comparison levels can be $[-14/9, -10/9]$ or $[-2/9, 2/9]$ or $[10/9, 14/9]$ and another ternary bit will be resolved. In cycle3, depending on the decision of cycle2, the residue voltage can be in any of the nine ranges: $[-2, -14/9]$ or $[-14/9, -10/9]$ or $[-10/9, -2/3]$ or $[-2/3, -2/9]$ or $[-2/9, 2/9]$ or $[2/9, 2/3]$ or $[2/3, 10/9]$ or $[10/9, 14/9]$ or $[14/9, 2]$. So, the circuit of radix-3 SAR ADC will generate comparison levels which can be $(50/27, 46/27)$ or $(38/27, 34/27)$ or $(26/27, 22/27)$ or $(14/27, 10/27)$ or $(2/27, -2/27)$ or $(-10/27, -14/27)$ or $(-22/27, -26/27)$ or $(-34/27, -38/27)$ or $(-46/27, -50/27)$ and another ternary bit will be resolved. Hence, a total of $(3 \times 1.6) = 4.8$ binary bits are achieved from 3 cycles.

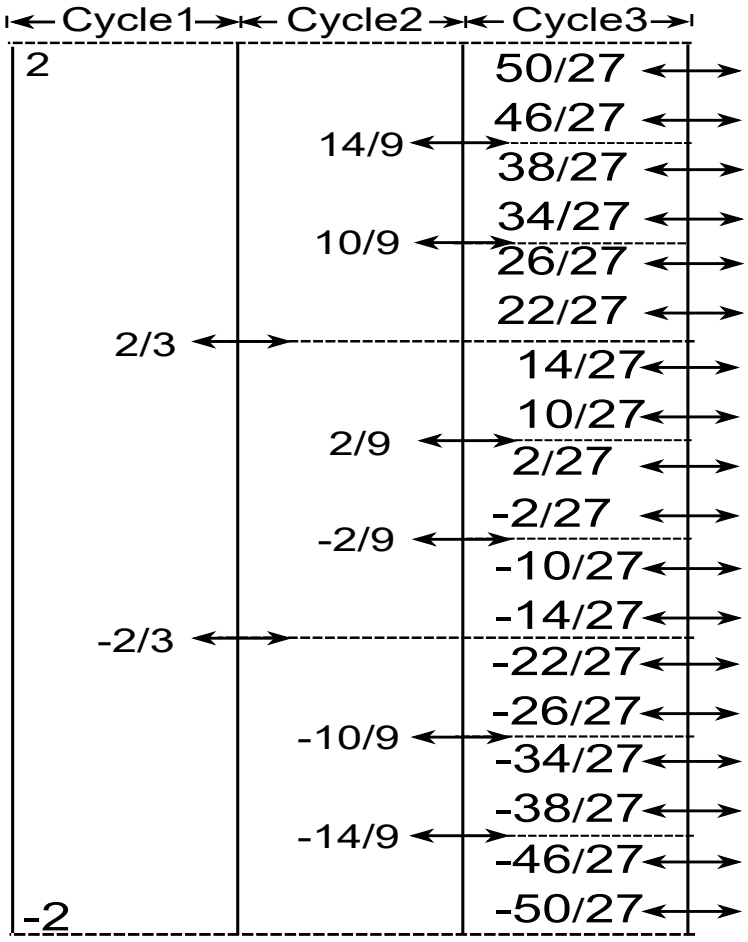


Figure 2.2: Reference voltage levels of 3-ternary-bit radix-3 SAR ADC.

2.3.2 Circuit Architecture

Fig.2.3 shows the architecture of proposed N-ternary-bit radix-3 SAR ADC containing N capacitors in each DAC where capacitors are:

$$C_i = \begin{cases} 2\sum_{j=1}^{i-1} C_j & \text{where } i \in [2, N] \\ C_u & \text{where } i = 1 \end{cases} \tag{2.1}$$

where C_u is the required unit capacitor of the DAC array. In this architecture, two comparators and two capacitor DACs are used to perform the ternary search. For

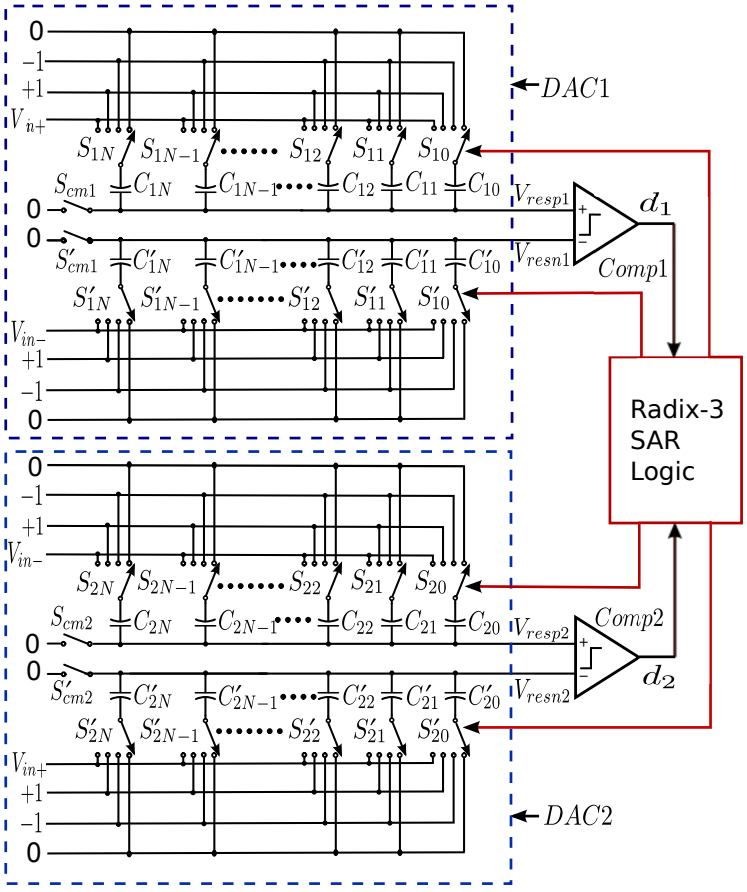


Figure 2.3: Architecture of N-ternary-bit radix-3 SAR ADC.

an N-ternary-bit radix-3 SAR ADC N comparison cycles are needed to generate the final digital output.

We assume a full swing input $V_{in+} \in [-1, 1]$ and $V_{in-} \in [-1, 1]$, thus $V_{in} \in [-2, 2]$. C_{10} to C_{1N} and C'_{10} to C'_{1N} create differential DAC DAC_1. Similarly, C_{20} to C_{2N} and C'_{20} to C'_{2N} create differential DAC DAC_2. $Comp_1$ and $Comp_2$ are used for the ternary search. Switches S_{10} to S_{1N} and S'_{10} to S'_{1N} represent sampling switch and logic transition switches for DAC_1. Switches S_{20} to S_{2N} and S'_{20} to

S'_{2N} represent sampling switch and logic transition switches for DAC_2. During the sampling phase, the positive input signal V_{in+} is sampled on C_{1N} to C_{10} and C'_{2N} to C'_{20}. The negative input signal V_{in-} is sampled on C'_{1N} to C'_{10} and C_{2N} to C_{20}.

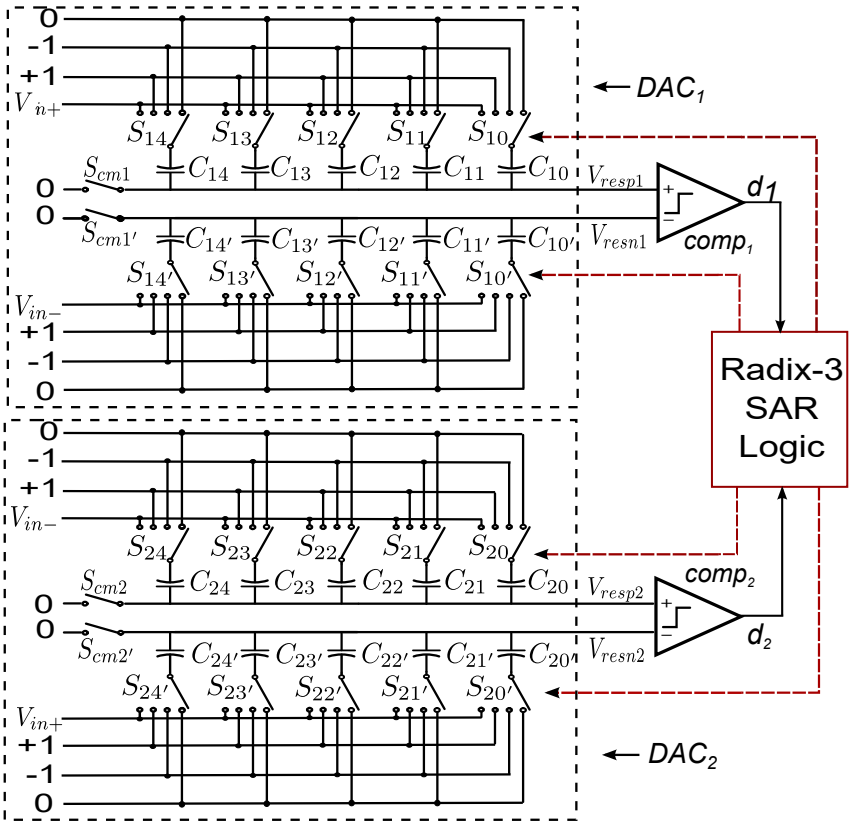


Figure 2.4: Architecture of 4-ternary-bit radix-3 SAR ADC.

The radix-3 SAR logic has two functions. First, it generates the control signals for DAC comparison operations. Second, it is used to generate the comparison clocks to fire the comparators. The values of capacitors are set by (2.1). We can easily expand the ternary bits by adding more capacitors under this rule. The reason why we choose the capacitor values as above will be shown later. Fig.2.4 is a

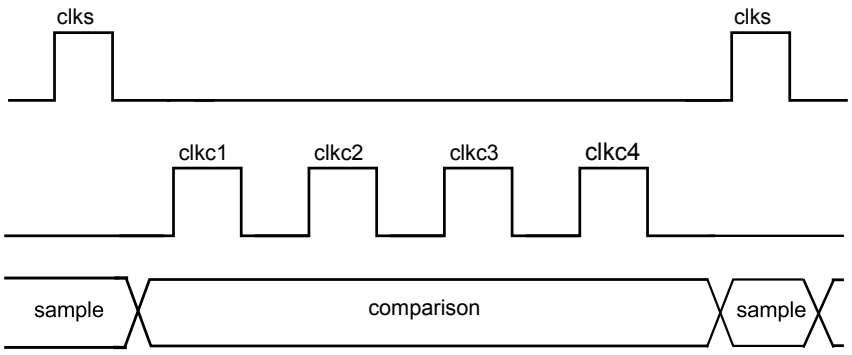


Figure 2.5: Sampling and comparison clocks for 4-ternary-bit radix-3 SAR ADC.

modified version from Fig.2.3 for a 4-ternary-bit radix-3 ADC. For an N-ternary-bit radix-3 SAR ADC, N comparison cycles are needed to generate the final digital output. For our example of Fig.2.4, it takes 4 comparison cycles. Fig.2.5 shows the timing diagram of the sampling clock and the comparison clock. It follows the same rule as regular radix-2 SAR ADCs. It takes one clock cycle for sampling and four clock cycles for convergence (clkc$_1$-clkc$_4$).

In Fig.2.4, we define V_{refp} as $+1$, V_{refn} as -1 and V_{cm} as 0. During the sampling phase, the positive input signal V_{in+} is sampled on C_{10} to C_{14} and $C_{20'}$ to $C_{24'}$. The negative input signal V_{in-} is sampled on $C_{10'}$ to $C_{14'}$ and C_{20} to C_{24}. All top plates of the capacitors are initially connected to a common mode voltage 0 through switches S_{cm1}, $S_{cm1'}$, S_{cm2}, and $S_{cm2'}$ respectively. After the sampling phase, the switches S_{cm1}, $S_{cm1'}$, S_{cm2} and $S_{cm2'}$ are opened. The radix-3 search algorithm is realized by the following operations.

In the first comparison cycle clkc$_1$, the following steps are performed simultaneously.

- For $DAC1$, C_{14} and $C_{14'}$ are connected to 0. C_{10} to C_{13} are connected to 1. $C_{10'}$ to $C_{13'}$ are connected to -1.

- For $DAC2$, C_{24} and $C_{24'}$ are connected to 0. C_{20} to C_{23} are connected to 1. $C_{20'}$ to $C_{23'}$ are connected to -1.

According to charge conservation at the V_{resp1} node,

$$-V_{in+} \times \sum_{i=0}^{4} C_i = V_{resp1} \times C_4 + (V_{resp1} - 1) \times \sum_{i=0}^{3} C_i$$

$$\implies V_{resp1} = -V_{in+} + 1/3 \tag{2.2}$$

Similarly:

$$V_{resn1} = -V_{in-} - 1/3 \tag{2.3}$$

From (2.2) and (2.3), we obtain:

$$V_{resp1} - V_{resn1} = -V_{in} + 2/3 \tag{2.4}$$

Therefore, d_1 is given by

$$d_1 = \begin{cases} 1 & \text{if } V_{in} < 2/3 \\ 0 & \text{if } V_{in} > 2/3 \end{cases} \tag{2.5}$$

Due to symmetry, we also have the output of comparator 2 as:

$$d_2 = \begin{cases} 1 & \text{if } V_{in} > -2/3 \\ 0 & \text{if } V_{in} < -2/3 \end{cases} \tag{2.6}$$

Based on the above analysis, we can see that in the first comparison cycle, $DAC1$ and $DAC2$ are doing the radix-3 search for V_{in}. If (d_1, d_2) is (1, 1), V_{in} is in the region of $[-2/3,\ 2/3]$. Similarly, if (d_1, d_2) is (1, 0), $V_{in} \in [-2, -2/3]$ and if (d_1, d_2) is (0, 1), $V_{in} \in [2/3,\ 2]$. (d_1, d_2) equals to (0, 0) is impossible in our structure. If there are capacitor mismatches, the determined levels will not be exactly $-2/3$ and $2/3$. Depending on the outputs of two comparators, the back-end SAR logic determines which region V_{in} is in and generates the next set of decision levels to be used in the next comparison cycle.

During the next comparison cycle clkc$_2$:

If $V_{in} \in [2/3,\ 2]$,

- For $DAC1$, C_{14} is connected to 1 and $C_{14'}$ is connected to -1. C_{13} and $C_{13'}$ are connected to 0. C_{10} to C_{12} are connected to 1. $C_{10'}$ to $C_{12'}$ are connected to -1.
- For $DAC2$, C_{24} is connected to -1 and $C_{24'}$ is connected to 1. C_{23} and $C_{23'}$ are connected to 0. C_{20} to C_{22} are connected to 1. $C_{20'}$ to $C_{22'}$ are connected to -1.

Following the same calculation as the first comparison cycle, we have:

$$d_1 = \begin{cases} 1 & \text{if } V_{in} < 14/9 \\ 0 & \text{if } V_{in} > 14/9 \end{cases} \tag{2.7}$$

$$d_2 = \begin{cases} 1 & \text{if } V_{in} > 10/9 \\ 0 & \text{if } V_{in} < 10/9 \end{cases} \tag{2.8}$$

$10/9$ and $14/9$ are the 1/3 and 2/3 levels of $[2/3,\ 2]$.

If $V_{in} \in [-2/3,\ 2/3]$,

- For $DAC1$, C_{14} and $C_{14'}$ are connected to 0. C_{13} and $C_{13'}$ are connected to 0. C_{10} to C_{12} are connected to 1. $C_{10'}$ to $C_{12'}$ are connected to -1.
- For $DAC2$, C_{24} and $C_{24'}$ are connected to 0. C_{23} and $C_{23'}$ are connected to 0. C_{20} to C_{22} are connected to 1. $C_{20'}$ to $C_{22'}$ are connected to -1.

Similar to the first comparison cycle, we have:

$$d_1 = \begin{cases} 1 & \text{if } V_{in} < 2/9 \\ 0 & \text{if } V_{in} > 2/9 \end{cases} \quad d_2 = \begin{cases} 1 & \text{if } V_{in} > -2/9 \\ 0 & \text{if } V_{in} < -2/9 \end{cases} \tag{2.9}$$

$-2/9$ and $2/9$ are the 1/3 and 2/3 levels of $[-2/3,\ 2/3]$.

If $V_{in} \in [-2,\ -2/3]$,

- For $DAC1$, C_{14} is connected to -1 and $C_{14'}$ is connected to 1. C_{13} and $C_{13'}$ are connected to 0. C_{10} to C_{12} are connected to 1. $C_{10'}$ to $C_{12'}$ are connected to -1.
- For $DAC2$, C_{24} is connected to 1 and $C_{24'}$ is connected to -1. C_{23} and $C_{23'}$ are connected to 0. C_{20} to C_{22} are connected to 1. $C_{20'}$ to $C_{22'}$ are connected to -1.

As a result:

$$d_1 = \begin{cases} 1 & \text{if } V_{in} < -10/9 \\ 0 & \text{if } V_{in} > -10/9 \end{cases} \quad d_2 = \begin{cases} 1 & \text{if } V_{in} > -14/9 \\ 0 & \text{if } V_{in} < -14/9 \end{cases} \tag{2.10}$$

$-14/9$ and $-10/9$ are the 1/3 and 2/3 levels of $[-2,\ -2/3]$.

We can easily see from the above analysis that our proposed ADC is doing the radix-3 search in the second comparison cycle clkc_2. For the following comparison cycles clkc_3 and clkc_4, our proposed radix-3 SAR operates the same way as in clkc_2. The calculation above also shows that the reason we choose the capacitor ratio by $C_i = 2\sum_{j=1}^{i-1} C_j$ is to generate 1/3 and 2/3 levels of the corresponding region according to the radix-3 SAR logic outputs. If we define Q_i to be the ternary bit output corresponding to C_i, the relation between $(d_1,\ d_2)$ and Q_i is shown in Table 2.1. The final 4-ternary-bit digital output is: $D_{out} = (4\sum_{i=1}^{4} 3^{i-1}Q_i)/3^4$.

Table 2.1: The radix-3 SAR output representations

d_1	d_2	$Region$	D_i
0	1	$V_{in} \in [2/3,\ 2]$	1
1	1	$V_{in} \in [-2/3,\ 2/3]$	0
1	0	$V_{in} \in [-2, -2/3]$	-1
0	0	$not\ Possible$	$-$

To clearly show the operation of our ADC, an example of V_{in}=$-1/4$ is given as the input signal to the radix-3 SAR ADC. Fig.2.6 shows this operation. It takes four comparison cycles to finish a full conversion. Assuming, unit capacitor value as C, each DAC contains $C, 2C, 6C, 18C$ and $54C$ for 4-ternary-bit radix-3 SAR ADC. The region of V_{in} at the end of every corresponding comparison cycle is also shown in Fig.2.6. In clkc_1, V_{in} is compared against '$2/3$' and '$-2/3$' as explained by (2.4). As (d_1, d_2) becomes $(1, 1)$, V_{in} is within $[-2/3, 2/3]$) range and according to Table 2.1, capacitor $54C$ will be connected to '0'. Clearly the proposed SAR ADC is doing the radix-3 search.

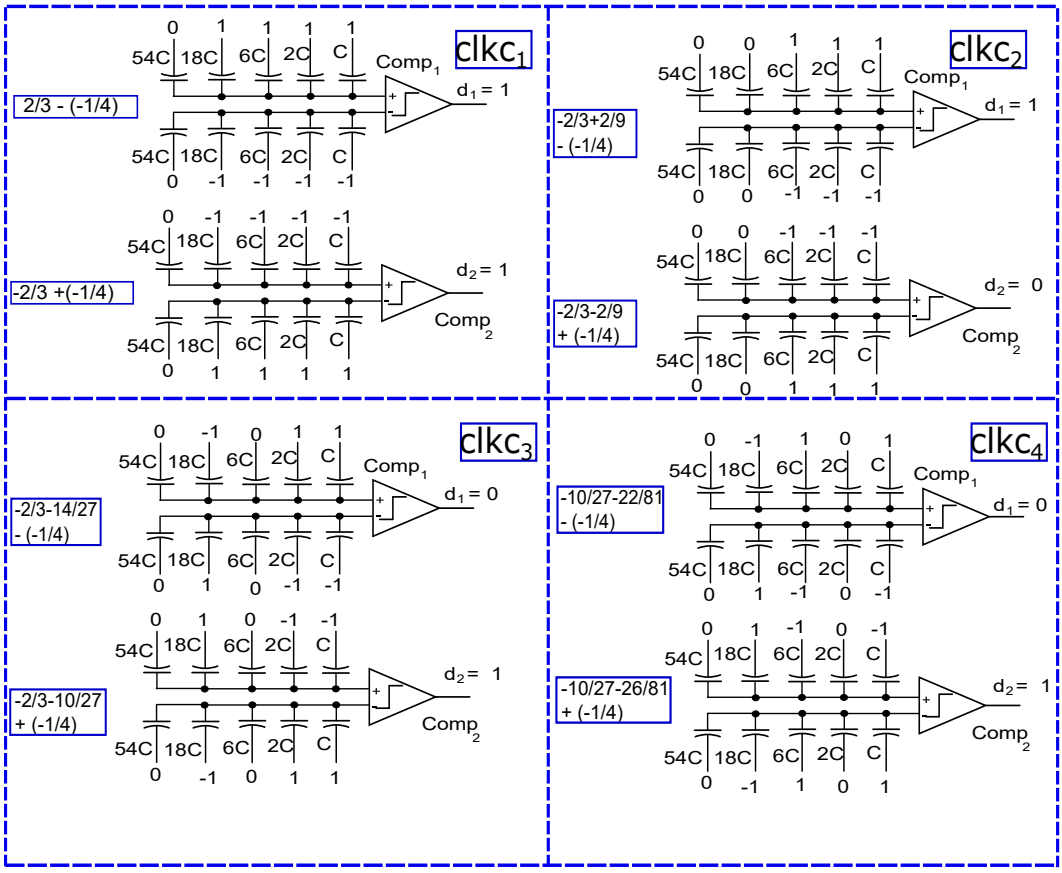


Figure 2.6: Operation example of 4-ternary-bit radix-3 SAR ADC.

In clkc$_2$, V_{in} is compared against ' $-2/9$' and '$2/9$' and (d_1, d_2) becomes $(1, 0)$, V_{in} is within $[-2/3, -2/9]$ range and according to Table 2.1, capacitor $18C$ of $DAC1$ will be connected to '-1' and capacitor $18C$ of $DAC2$ will be connected to '1' as shown in Fig.2.6.

In clkc$_3$, V_{in} is compared against ' $-10/27$' and ' $-14/27$' and (d_1, d_2) becomes $(0, 1)$, V_{in} is within $[-10/27, -2/9]$ range and according to Table 2.1, capacitor $6C$ of $DAC1$ will be connected to '1' and capacitor $6C$ of $DAC2$ will be

connected to '-1' as shown in Fig.2.6.

In clkc$_4$, V_{in} is compared against ' $-22/81$' and ' $-26/81$' and (d_1, d_2) becomes $(1, 0)$, V_{in} is within $[-12/81, -2/9]$ range and according to Table 2.1, capacitor $2C$ of $DAC1$ will be connected to '1' and capacitor $2C$ of $DAC2$ will be connected to '-1' as shown in Fig.2.6.

The final digital output is $D_{out} = (0, -1, 1, 1)|_3 = 4 \times (0 - 18 + 6 + 2)/81 = -20/81$. The quantization error is $-1/324$, which is within the 4-ternary-bit accuracy.

To illustrate the circuit level operation, we take another example of input voltage '$\frac{75}{108}$' for 3-ternary-bit radix-3 SAR ADC. In the first comparison cycle, clkc$_1$, capacitor 18C of $DAC1, 2$ are connected to '0' and rest of the capacitors are connected to '1' and '-1' which generate two reference levels '$2/3$' and '$-2/3$' as shown in Fig.2.7. Comparators' outputs (d_1, d_2) become (0, 1) which means that the input voltage is within [2/3, 2] range and a simple logic circuit converts that to single control inputs D$_1$ and D'$_1$ for MSB capacitors of $DAC1$ and $DAC2$ respectively. Thus the first 1.6 bits are obtained in cycle clkc$_1$.

In the second comparison cycle, clkc$_2$, capacitor 18C of $DAC1, 2$ are already assigned with required values. Capacitor 6C of $DAC1, 2$ are connected to '0' and rest of the capacitors are connected to '1' and '-1' which generate two reference levels'$\frac{10}{9}$' and '$\frac{14}{9}$' as shown in Fig.2.7. Comparators' outputs (d_1, d_2) become $(1, 0)$ which means that the input voltage is within [10/9, 2/3] range and a simple logic circuit converts that to single control inputs D$_2$ and D'$_2$ for capacitors

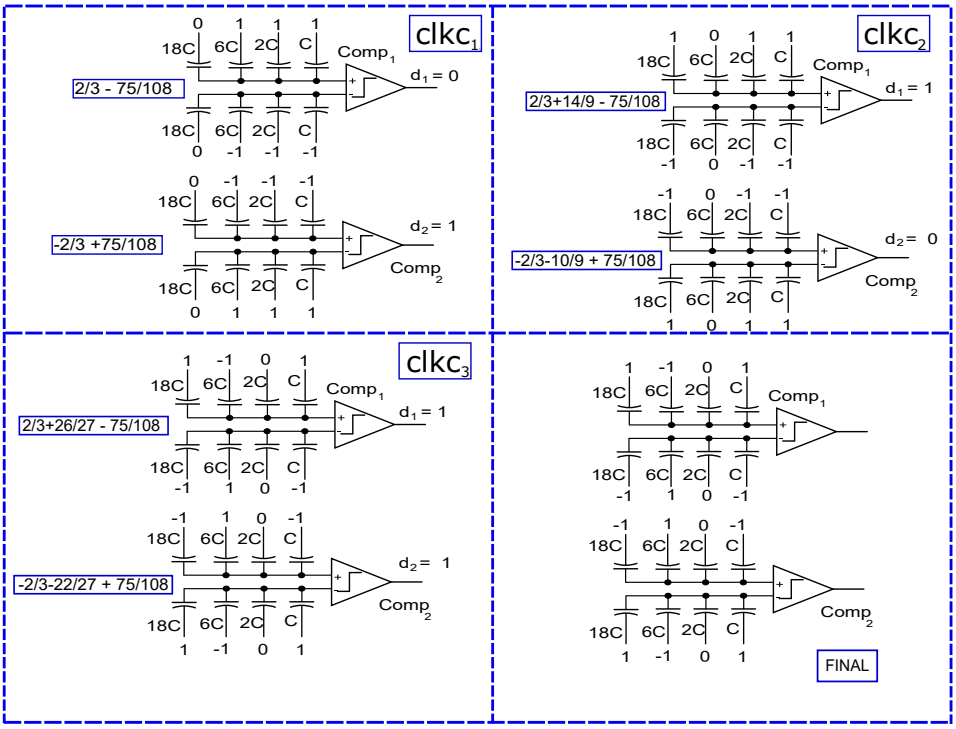


Figure 2.7: Conversion steps of 3-ternary-bit radix-3 ADC for input voltage of '75/108'.

6C of $DAC1$ and $DAC2$ respectively. Thus the second 1.6 bits are obtained in cycle clkc$_2$.

In the third comparison cycle, clkc$_3$, capacitor 6C of $DAC1, 2$ are already assigned with required values. Capacitor 2C of $DAC1, 2$ are connected to '0' and rest of the capacitors are connected to '1' and '-1' which generate two reference levels '$\frac{22}{27}$' and '$\frac{26}{27}$' as shown in Fig.2.7. Comparators' outputs (d_1, d_2) become (1, 1) which means that the input voltage is within [26/27, 22/27] range and a simple logic circuit converts that to single control inputs D$_3$ and D'$_3$ for capacitors 2C of $DAC1$ and $DAC2$ respectively. Thus the second 1.6 bits are obtained in cycle

clkc$_3$.

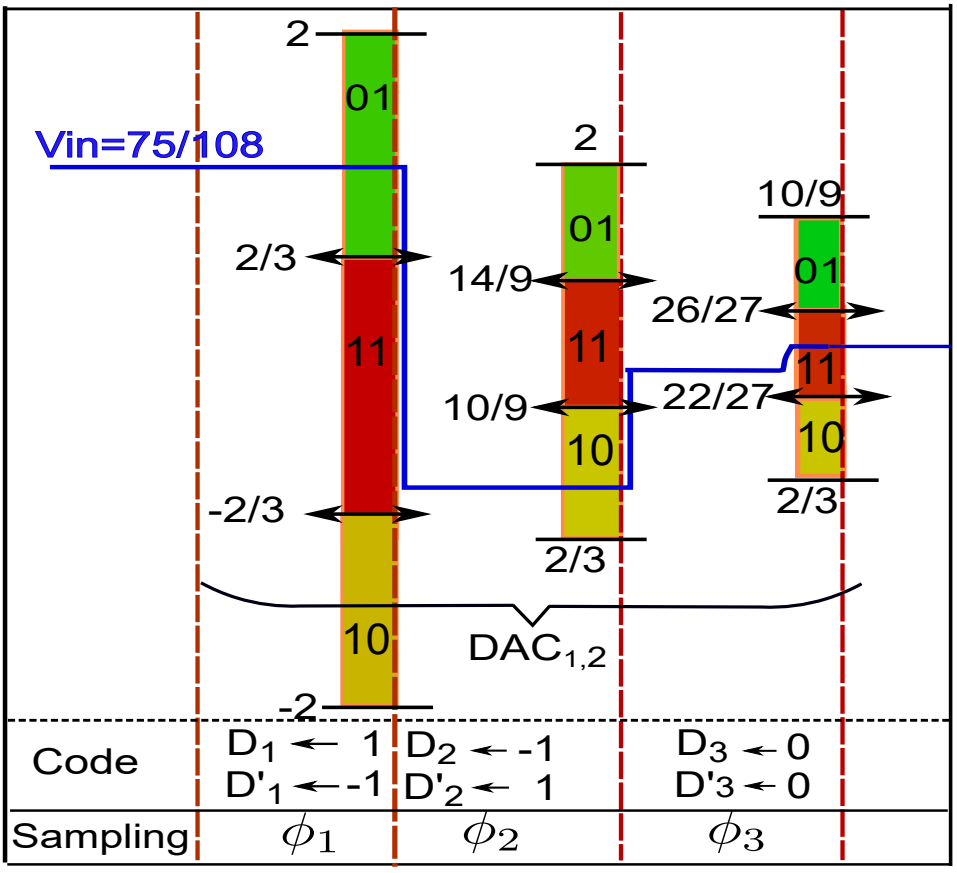


Figure 2.8: Sampling and comparison phases of 3-ternary-bit radix-3 ADC for input voltage of '75/108'.

Fig.2.8 explains the residual voltage for the conversion of input voltage '$\frac{75}{108}$' for 3-ternary-bit radix-3 SAR ADC.

To explain the generalized operation for N-ternary-bit radix-3 SAR ADC, we have introduced the flow diagram as shown in Fig.2.9.

The convergence starts at the MSB bit which is the N-th bit and the radix-3

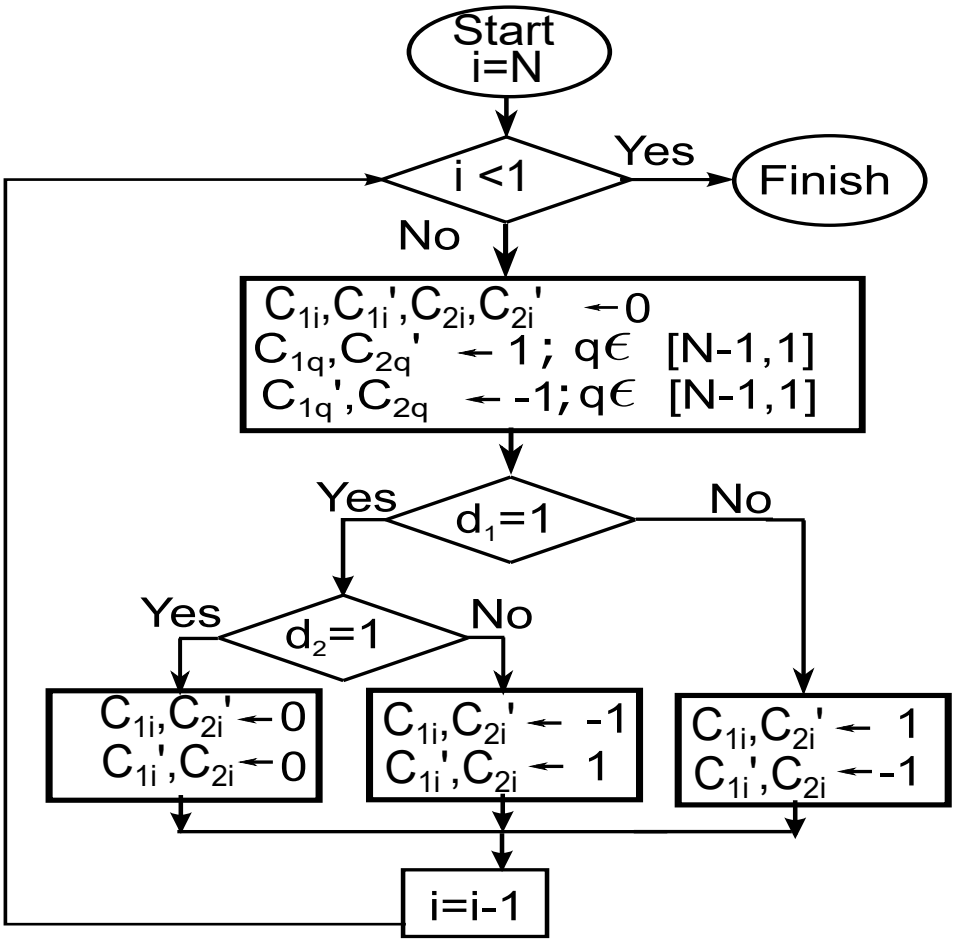


Figure 2.9: Conversion flow diagram for N-ternary-bit radix-3 SAR ADC.

search continues till the last bit. Each bit, before convergence, is assigned $'0'$ and rest of the bits are assigned $'1'$ and $-'1'$. As shown in Fig.2.4, two comparators will be used in radix-3 search. After comparator decisions (d_1,d_2), digital codes D_i and D_i' are generated based on Table 2.1 values and assigned to respective capacitors as shown in Fig.2.9.

2.4 Radix-3 SAR ADC Characterization

2.4.1 Effect of Comparator Offset

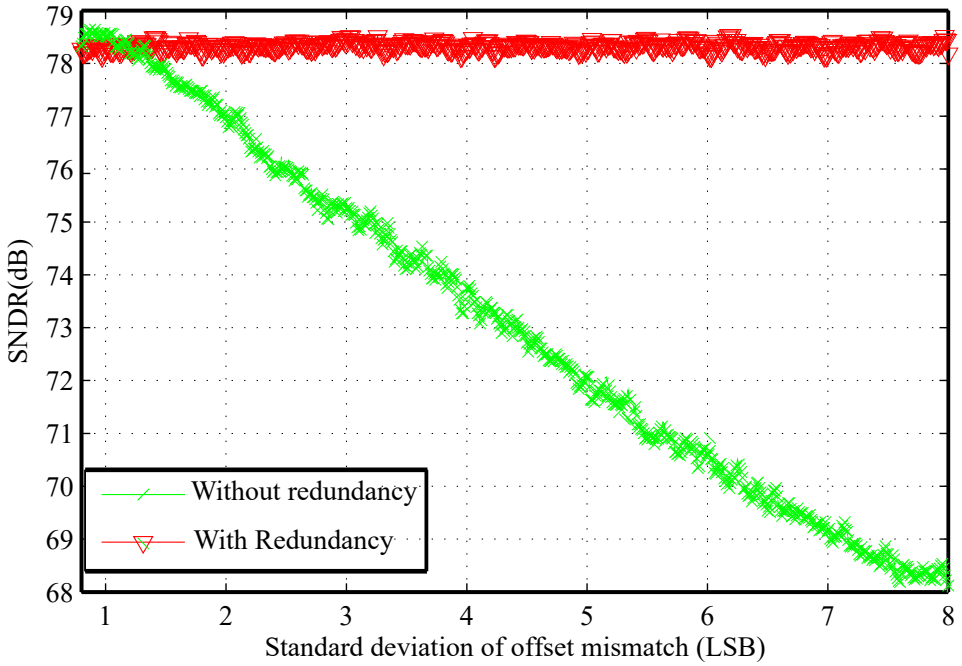


Figure 2.10: Monte-Carlo simulation to compare the effect of comparator offset.

The LSB of a radix-3 SAR ADC with N ternary bits is $2V_{ref}/2^{(1.6N)}$. During radix-3 search, comparator offset should be less than $V_{ref}/2^{1.6N}$ which is half of the LSB and though two comparators are used simultaneously, the offset mismatch between the comparators should not affect the linearity as long as it does not cross the over range limit set by the redundancy capacitor [Chang et al. [2013]], which is 9 LSB in our design. In the radix-3 SAR ADC, linearity is affected by the comparator offset mismatch since two comparators are used simultaneously during all the conversion steps. The variation of comparator offset is modeled by the Gaussian random variable with standard deviation. In Fig.2.10, SNDR was plotted based on

the result of 10000-sample Monte Carlo simulations for 8-ternary-bit ($\approx$ 13- binary-bit) radix-3 ADC with and without redundancy. As explained earlier, radix-3 SAR ADC with redundancy shows consistent SNDR over the whole range of variation as long as the redundancy level holds the over range to handle comparator offset mismatch. On the other hand, radix-3 ADC's linearity degrades significantly when there is no redundancy capacitor. Similarly, input common mode voltage variation will not affect the DAC linearity as we are using differential DACs.

2.4.2 Comparison of Energy

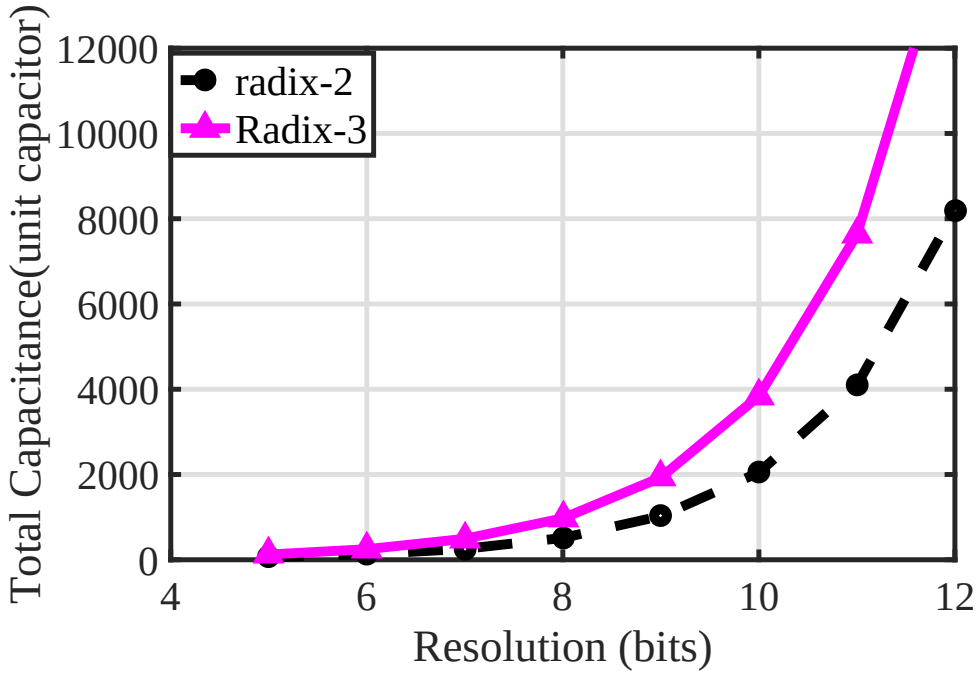


Figure 2.11: Comparison of total number of DAC capacitors.

One of the major contributors to power consumption in ADC is capacitor DAC. To achieve N binary bits, a radix-2 ADC requires a total of 2×2^N unit

capacitors. For the same binary resolution, a radix-3 ADC requires $\frac{N}{1.6}$ ternary bits and a total of $4 \times 3^{\frac{N}{1.6}}$ unit capacitors. Fig.2.11 compares the required unit capacitors for radix-2 and radix-3 SAR ADC. It shows that a radix-3 ADC requires more capacitors than a radix-2 SAR ADC to achieve the same resolution.

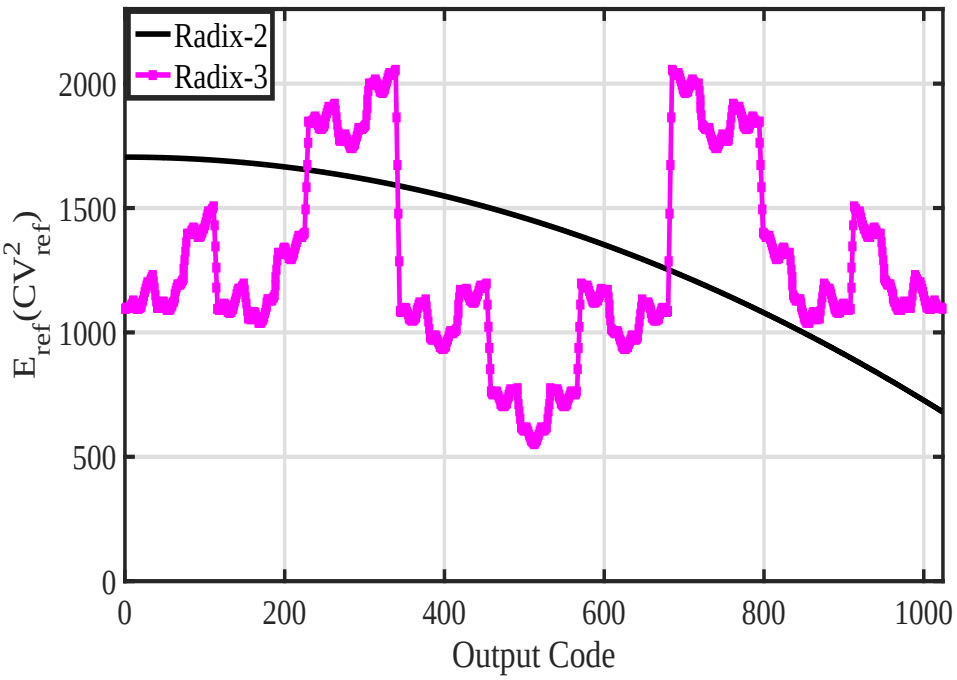


Figure 2.12: Comparison of DAC reference energy of radix-2 and radix-3 SAR ADC.

During radix-3 conversion, the converging capacitors are first connected to V_{cm}. If input voltage levels are within the $[1/3, 2/3]$ region of V_{ref}, then none of the capacitors will switch and the energy will be zero. So, in each conversion, either two capacitors or none will switch. Fig.2.12 compares the DAC reference energy of a 10-bit radix-2 and a radix-3 SAR ADC. Due to it's distinct architecture, it is

evident that to obtain equivalent binary bits, a radix-3 SAR ADC consumes more power than a conventional radix-2 SAR ADC for certain portion of the input range.

2.4.3 Comparison of Speed

To achieve K binary bits of resolution, a radix-3 SAR ADC requires $\frac{K}{1.6}$ cycles and a conventional radix-2 SAR ADC requires K cycles. Fig.2.13 presents the conversion cycles of radix-2 and radix-3 SAR ADCs. It clearly shows that, because of the architecture, a radix-3 SAR ADC converges faster than a conventional radix-2 SAR ADC.

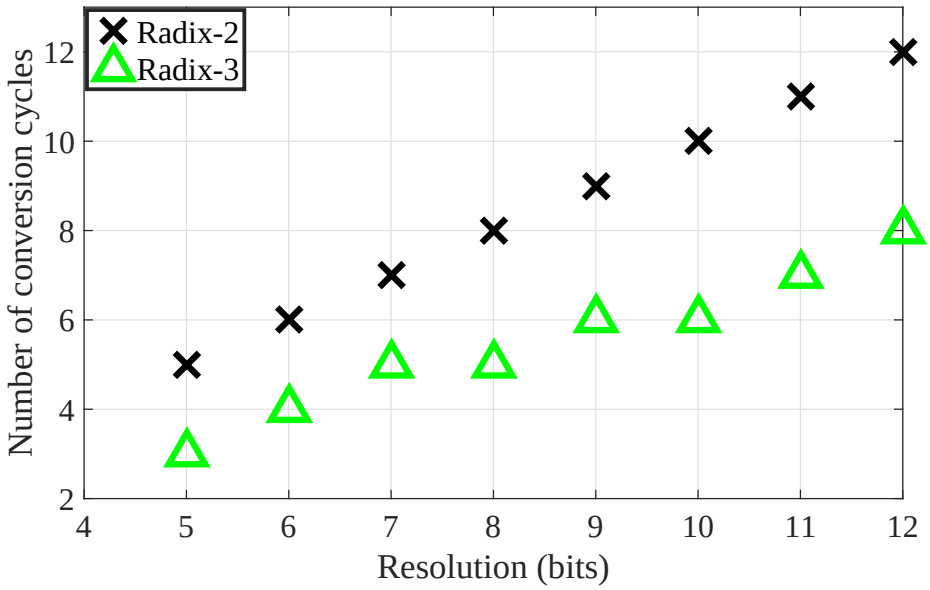


Figure 2.13: Comparison of conversion cycles of radix-2 and radix-3 SAR ADC.

Table 2.2 compares the speed gain of a radix-3 SAR ADC over a conventional radix-2 SAR ADC. T_{conv} means the number of conversion cycles radix-2

requires and $T_{radix-3}$ means the number of conversion cycles radix-3 requires to resolve an analog input. By varying the resolution from 6-binary-bits to 12-binary-bits, it is evident that a radix-3 ADC can achieve a maximum 37% speed gain over a conventional SAR ADC.

Table 2.2: Speed gain of radix-3 ADC over radix-2 SAR ADC.

Resolution	(T_{conv}-$T_{radix-3}$)/T_{conv} (%)
6	33.3
7	28.6
8	37.5
9	33.3
10	30
11	36.3
12	30

2.4.4 SAR Logic Power:

The major contributor to logic power are flip flops and logic circuits that connect the capacitors to correct voltage levels. For N binary bit resolution, a radix-2 ADC requires $(N+1)$ DFFs to latch the data for capacitor DAC, where a radix-3 ADC requires $(\frac{2N}{1.6}+1)$. Similarly, the required control circuits (MOSFETS) for capacitor DACs for a radix-2 ADC is $\sim (2N+2)$, and for a radix-3 ADC is $\sim (\frac{6(N+1)}{1.6})$. Fig.2.14 shows the comparison of total DFFs and Fig.2.15 shows control circuits.

Considering above facts, it shows that a radix-3 SAR ADC offers partly higher and partly lower DAC energy than a conventional radix-2 ADC depending

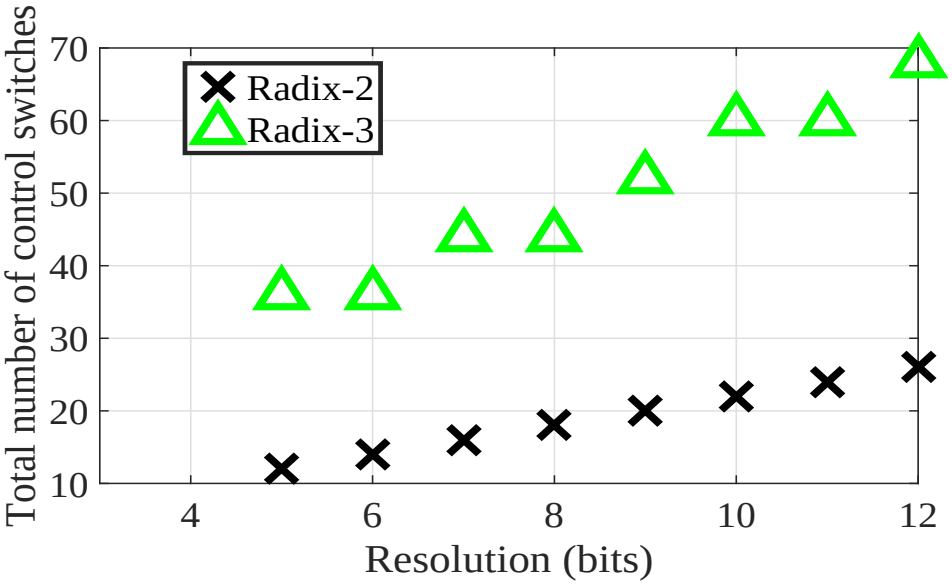


Figure 2.14: Comparison of total number of control switches.

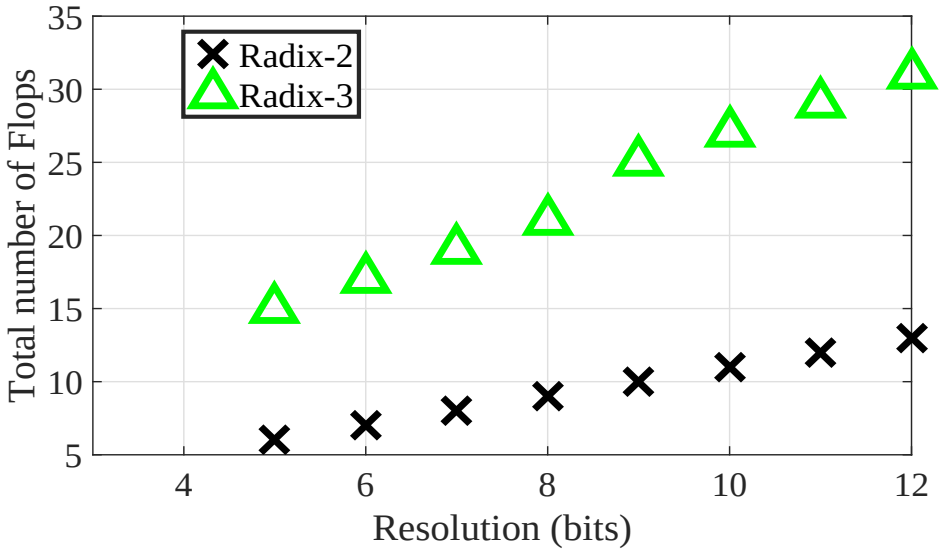


Figure 2.15: Comparison of total number of DFFs.

on the input voltage magnitude. It offers more power in logic circuit and control switches than radix-2 ADC. Considering the speed gain over a radix-2 ADC and equivalent accuracy as a radix-2 ADC, a radix-3 SAR ADC can be a good candidate for high speed data conversion.

2.5 Algorithm and Theoretical Analysis of Capacitor Calibration

Fig.2.16 is a simplified version of Fig.2.3. It just shows one side of the DAC for simplicity. A redundant capacitor C_{Rd} is required for calibration purpose. Due to process variation, it is assumed that each capacitors has varied by a proportion of ϵ [Lee et al. [1984]]:

$$C_n = \begin{cases} 2 \cdot 3^{n-2} C_{unit}(1+\epsilon_n) & \text{if } n > 1 \\ C_{unit}(1+\epsilon_n) & \text{if } n = 1 \end{cases} \tag{2.11}$$

If number of LSB capacitors used for calibration is Q, then

$$C_{Rd} = 3^{Q-1} C_{unit}(1+\epsilon_{Rd}) \tag{2.12}$$

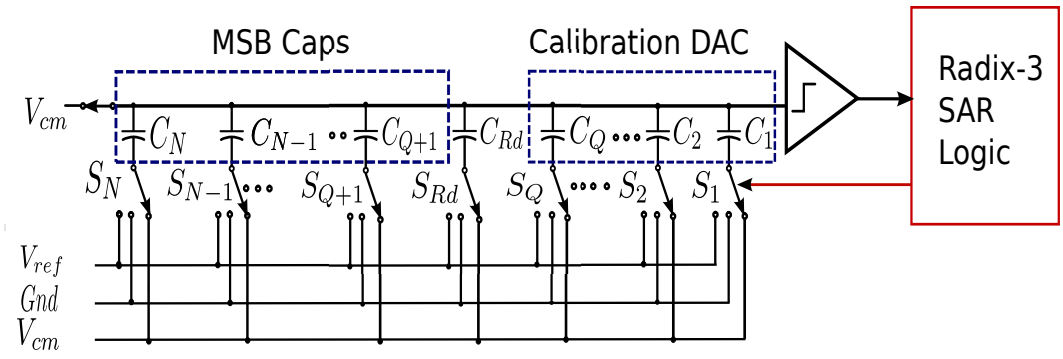


Figure 2.16: Simplified radix-3 DAC.

where C_{unit} is the unit capacitor and can be defined in terms of total capacitor C_{tot} as:

$$C_{unit} = \frac{C_{tot}}{3^{N-1}+3^{Q-1}}$$

$$= \frac{C_{unit}(2\sum_{i=2}^{N} 3^{i-2}(1+\epsilon_i)+(1+\epsilon_1)+3^{Q-1}(1+\epsilon_{Rd}))}{3^{N-1}+3^{Q-1}} \tag{2.13}$$

$$C_{unit} = C_{unit} + \frac{C_{unit}(2\sum_{i=2}^{N} 3^{i-2}\epsilon_i+\epsilon_1+3^{Q-1}\epsilon_{Rd})}{3^{N-1}+3^{Q-1}} \tag{2.14}$$

From (2.14) it is found that:

$$2\sum_{i=2}^{N}(3^{i-2}\epsilon_i)+\epsilon_1+3^{Q-1}\epsilon_{Rd}=0 \tag{2.15}$$

The output voltage V_{out} can be found in terms of the digital output code D_i where $i \in [2, N]$ and D_{Rd}:

$$V_{out} = \frac{V_{ref}(\sum_{i=2}^{N} C_i D_i + C_{Rd}D_{Rd})}{C_{total}}$$

$$= \frac{V_{ref}(2\sum_{i=2}^{N} 3^{i-2}(1+\epsilon_i)D_i+3^{Q-1}(1+\epsilon_{Rd})D_{Rd})}{(2\sum_{i=2}^{N} 3^{i-2}\epsilon_i+\epsilon_1+3^{Q-1}\epsilon_{Rd})(1+2\sum_{i=2}^{N} 3^{i-2}+3^{Q-1})}$$

From (2.15) we get that:

$$V_{out} = \frac{V_{ref}(2\sum_{i=2}^{N} 3^{i-2}(1+\epsilon_i)D_i+3^{Q-1}(1+\epsilon_{Rd})D_{Rd})}{3^{N-1}+3^{Q-1}} \tag{2.16}$$

If there is no mismatch, i.e $\epsilon_i = \epsilon_{Rd} = 0$, then the ideal output voltage will be:

$$V_{out,ideal} = \frac{V_{ref}(2\sum_{i=2}^{N} 3^{i-2}D_i+3^{Q-1}D_{Rd})}{3^{N-1}+3^{Q-1}} \tag{2.17}$$

So, the error voltage is:

$$V_{error} = V_{out} - V_{out,ideal}$$

$$V_{error} = \frac{V_{ref}(2\sum_{i=2}^{N} 3^{i-2}\epsilon_i D_i + 3^{Q-1}\epsilon_{Rd} D_{Rd})}{3^{N-1}+3^{Q-1}} \tag{2.18}$$

Defining the error voltage for the n-th capacitor as V_{ϵ_n} and for the redundant capacitor as $V_{\epsilon_{Rd}}$

$$V_{\epsilon_n} = \frac{2\ V_{ref} 3^{n-2}\epsilon_n}{3^{N-1}+3^{Q-1}} \tag{2.19}$$

$$V_{\epsilon_{Rd}} = \frac{V_{ref} 3^{Q-1}\epsilon_{Rd} D_{Rd}}{3^{N-1}+3^{Q-1}} \tag{2.20}$$

So, from (2.18), (2.19) and (2.20) we get:

$$V_{error} = \sum_{i=2}^{N} V_{\epsilon_i} D_i + V_{\epsilon_{Rd}} D_{Rd} \tag{2.21}$$

In the current ADC architecture, the N-th capacitor, C_N is equal to twice the sum of the LSB capacitors C_i, where $i \in [1, N-1]$. LSB capacitors C_i, $i \in [1, Q]$ do not require calibration as their mismatch error is negligible [Lee et al. [1984]]. So, calibration is performed on MSB capacitors C_i, $i \in [Q+1, N]$. Calibration is started by finding the mismatch of N-th MSB capacitor. V_{ref} is sampled across bottom plate of the MSB capacitor C_N and rest of the bottom plates of capacitors are connected to V_{cm} as shown in Fig.2.17.

Then V_{ref} is sampled on the bottom plate of all the capacitors except C_N and C_i, $i \in [1, Q]$ which will be connected to ground as shown in Fig.2.18. So,

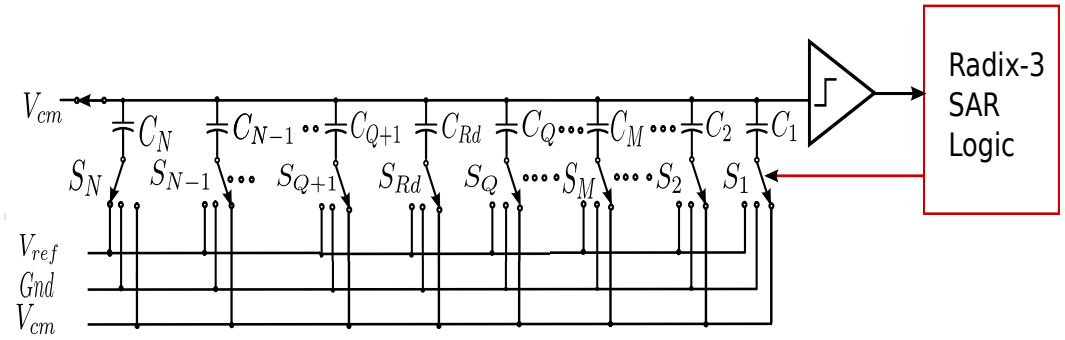


Figure 2.17: Precharging phase of calibration.

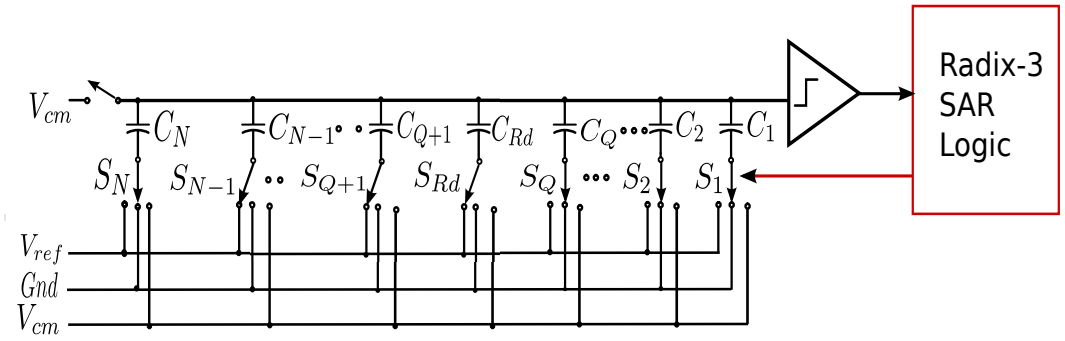


Figure 2.18: Charge distribution phase of calibration.

according to charge conservation, the residual charge at the top plate of the capacitors:

$$Q_{x_{resN}} = V_{ref}(\frac{1}{2}C_N - \sum_{i=Q+1}^{N-1} C_i - C_{Rd})$$

$$= V_{ref}C_{unit}(3^{N-2}\epsilon_N - 2\sum_{i=Q+1}^{N-1} 3^{i-2}\epsilon_i - 3^{Q-1}\epsilon_{Rd}) \tag{2.22}$$

As explained earlier, assuming that the mismatch errors of the LSB capacitors are negligible, i.e $\epsilon_i = 0$, $i \in [1, Q]$. From (2.15):

$$2 \cdot 3^{N-2}\epsilon_N = -2\sum_{i=Q+1}^{N-1} 3^{i-2}\epsilon_i - 3^{Q-1}\epsilon_{Rd} \tag{2.23}$$

So, from (2.22) and (2.23):

$$Q_{x_{resN}} = C_{unit} V_{ref} 3^{N-1} \epsilon_N \tag{2.24}$$

Hence, residual voltage:

$$V_{x_N} = \frac{Q_{x_{resN}}}{C_{total}} = \frac{3}{2} \frac{2 \cdot V_{ref}}{(3^{N-1} + 3^{Q-1})} \epsilon_N 3^{N-2} \tag{2.25}$$

From (2.20) and (2.25)

$$V_{x_N} = \frac{3}{2} V_{\epsilon_N} \tag{2.26}$$

Similarly, it can be shown that, the relationship between the residual voltage V_{xn} and the error voltage V_{ϵ_n}, $n \in [Q+1, N-1]$:

$$V_{\epsilon_n} = \frac{2}{3}(V_{xn} - \sum_{i=n+1}^{N} V_{\epsilon_i}) \tag{2.27}$$

After quantizing the error, the digitized error voltages DV_{ϵ_q} and the quantized residue voltage, $DV_{x_q}$are:

$$DV_{\epsilon_q} = \begin{cases} \frac{2}{3} DV_{x_q} & \text{if } q = N \\ \frac{2}{3}(DV_{x_q} - \sum_{i=q+1}^{N} DV_{\epsilon_i}) & \text{if } N > q \geq Q+1 \end{cases} \tag{2.28}$$

Which implies that, for an N-bit radix-3 SAR ADC, the digitized error voltage for the N-th bit MSB is:

$$DV_{\epsilon_N} = \frac{2}{3} DV_{x_N} \tag{2.29}$$

And the digitized error voltage for the rest of the MSB bits are:

$$DV_{\epsilon_n} = \frac{2}{3}(DV_{xn} - \sum_{i=n+1}^{N} DV_{\epsilon_i}), n = 2, 3 \,..\, N-1 \tag{2.30}$$

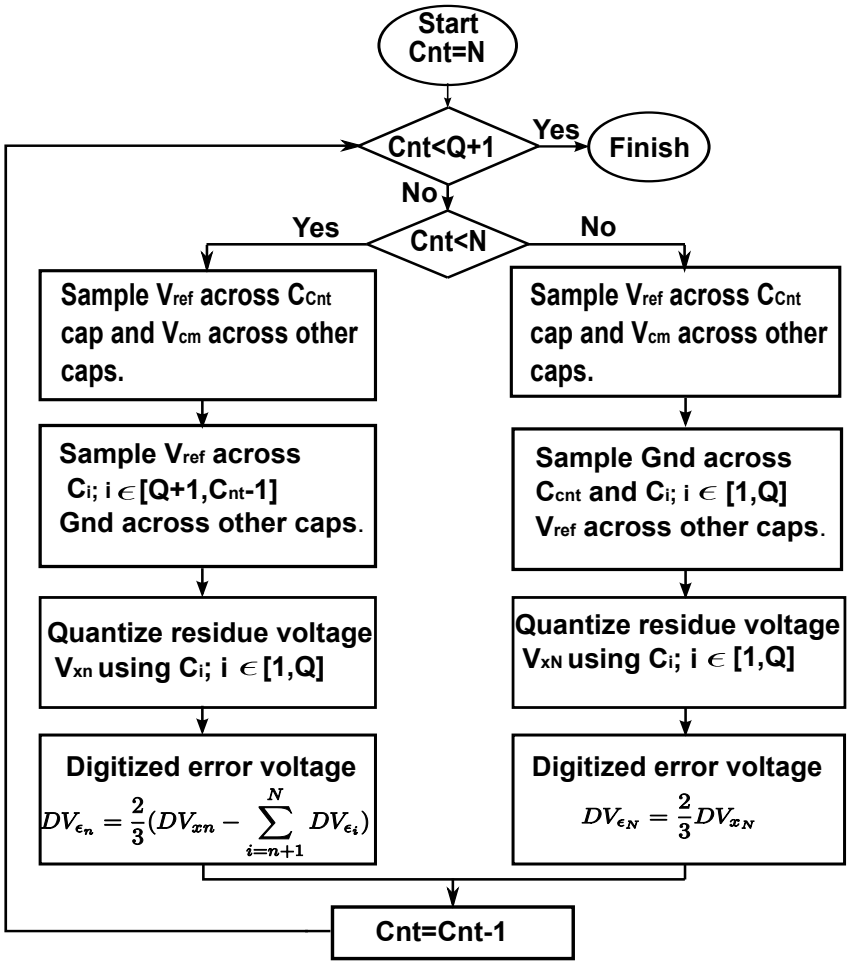


Figure 2.19: Steps for proposed calibration.

Fig.2.19 shows the calibration steps for the radix-3 SAR. As we see from (2.28) that the quantized digital voltages are different, for the MSB and rest of the MSBs, so the flow diagram shows two branches for calibration. In this flow, calibration is only done for first Q number of capacitors. The flow diagram is generalized and can be expandable for any size capacitor array. During normal conversion cycles, the calibration logic is de-activated and the converter works in the same way as a regular radix-3 SAR ADC. Finally the error correction voltages are added based on the DAC digital input code of the first $N - Q$ MSB capacitors. If the i-th bit is assigned as V_{ref}, V_{cm} or Gnd, then the corresponding error voltage DV_{ϵ_i} will be DV_{ϵ_i}, $(1/2)DV_{\epsilon_i}$ or 0 respectively. C_i, $i \in [1, Q]$ can be used for digitizing the error terms using the radix-3 algorithm. Quantizing the error voltage does not affect the calibration performance much as the quantized values closely follow the original error voltages.

2.6 Key Circuit Building Blocks

2.6.1 SAR Logic and Control

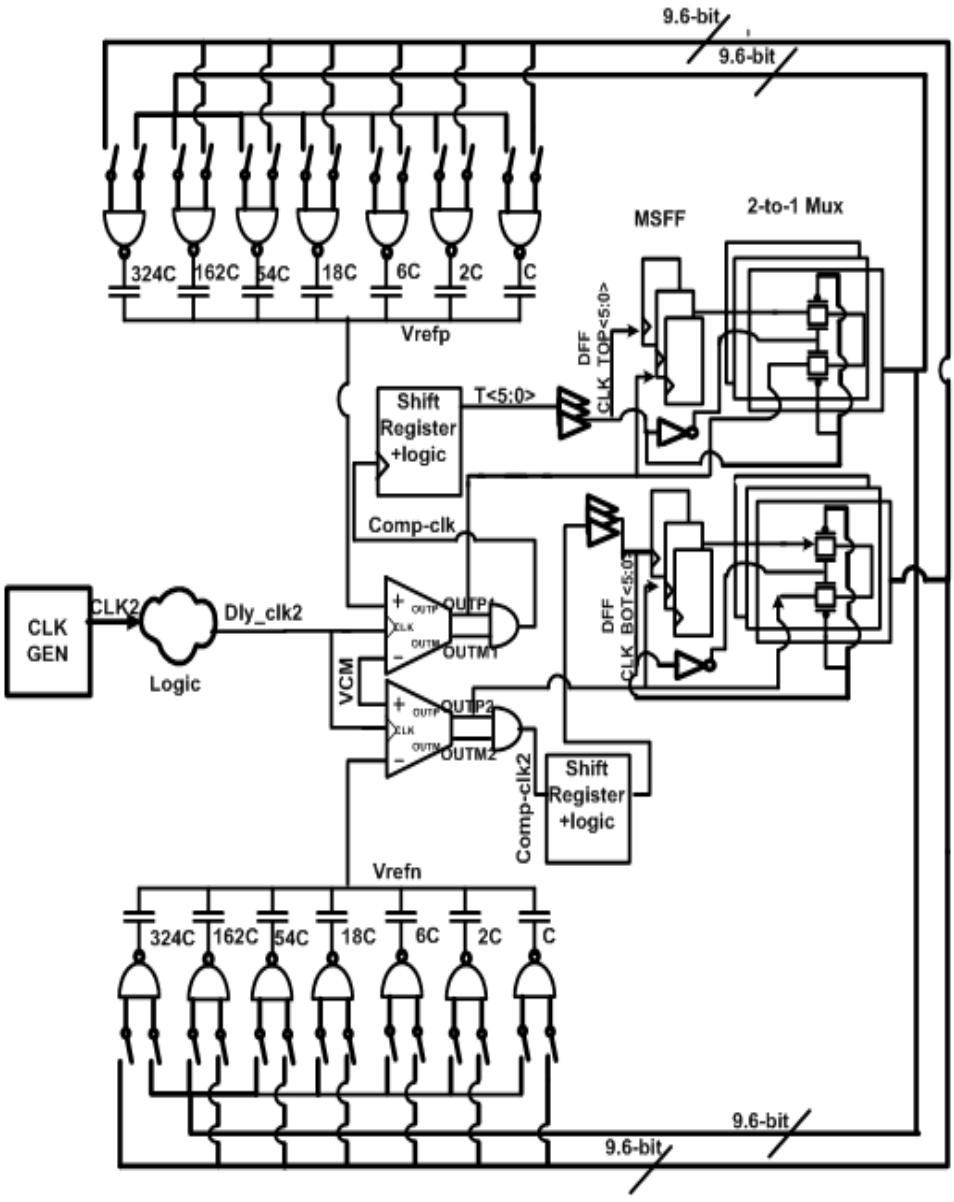


Figure 2.20: Top level circuit diagram of the proposed radix-3 SAR ADC.

In this subsection, we discuss the logic design of the radix-3 SAR ADC. Fig.2.20 shows the detail top level schematic of the proposed 6-ternary-bits ($\approx$ 9.6-binary-bit) radix-3 SAR ADC. The ADC consists of two differential capacitor arrays. The cap arrays are driven by logic circuits which include mux and flip flops. The data are driven to the flops by the comparators. The ADC uses two comparators with a fully synchronous architecture. Details on the logic and other circuits will be discussed in the following subsections.

2.6.2 Clock Generation Logic

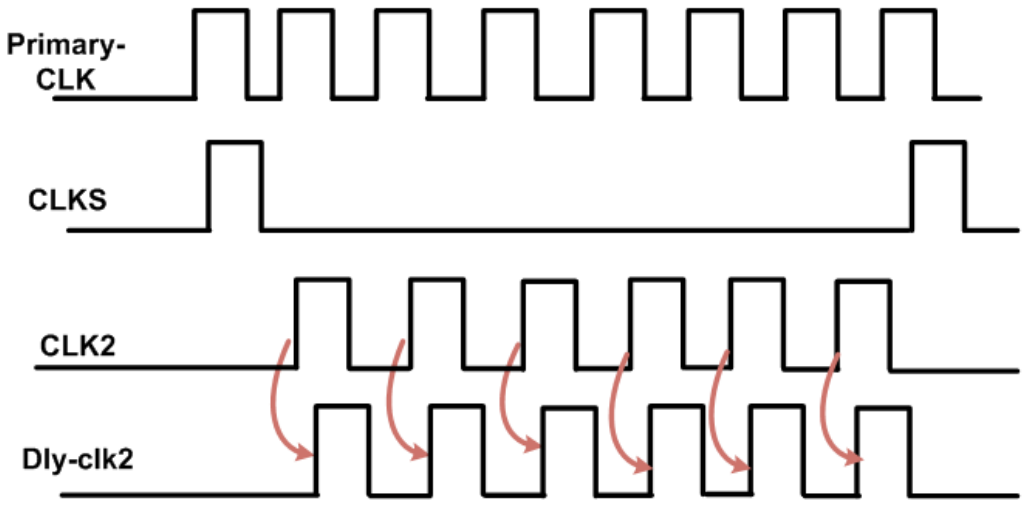


Figure 2.21: Timing diagram of the proposed radix-3 SAR ADC.

In this design, we will have 1 clock cycle $CLKS$ for sampling. 6 clock cycles for comparison and convergence of SAR ADC. The important thing about the design is, we don't need any extra clock cycle to send the data to PAD. Fig.2.21

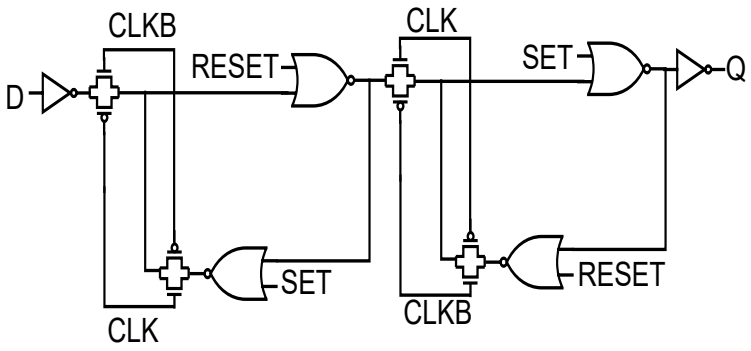


Figure 2.22: MSFF flip-flop used in radix-3 SAR ADC design.

shows the timing diagram for the ADC. $Primary - CLK$ is the external clock input. It goes to a 6-bit counter and it generates the radix-3 comparator clock $CLK2$. $CLK2$ goes through delay cell and generates $Dly - clk2$ for the radix-3 SAR ADC comparators.

Fig.2.22 shows the circuit diagram of the MASTER-SLAVE flip flop (MSFF) used in our design with SET and $RESET$ options. Fig.2.23 shows the timing diagram of the MASTER-SLAVE flip flop (MSFF) and when the data is available at the input of the capacitor switching circuits.

Fig.2.24 shows circuits for the clock generation for the data flops which latch the data of the radix-3 comparison. The clocks are generated from a 6-bit shift register. Fully synchronous logic has been used for our design. The sampling clock $CLKS$ sets/resets the flops in the shift register. The clock for the shift register's flops ($Comp\_clk$) are generated by the the outputs of the radix-3 comparator. In each cycle, depending on the input values of the comparator, either $outp$ or $outm$ of the comparator will fire a '1' and with the delay circuit, a pulse will be generated.

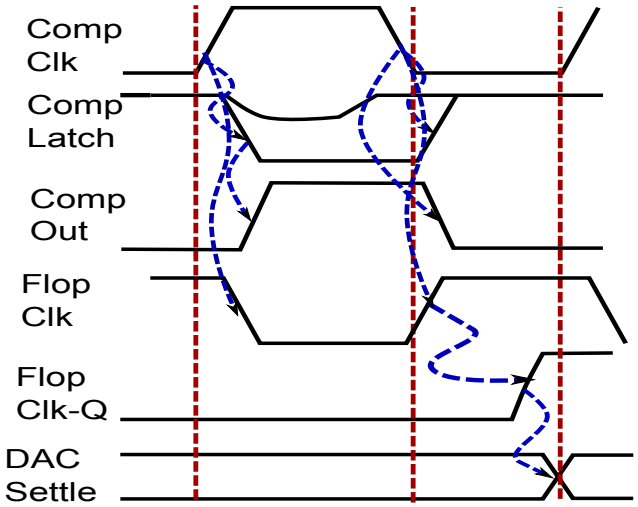


Figure 2.23: Timing waveform of MSFF.

After that, the shift register consisting of $DFFS$ and $DFFR$ generates the timing signals $T<0>$ - $T<5>$. To drive the output load, buffers are required and thus, $DFF\_CLK<5:0>$ are generated from the outputs of buffers.

Fig.2.25 shows the timing diagram for clock generation for the data flops to latch data of the radix-3 comparison output. While $CLKS$ is high, T_{ini} is high and $T<0>$-$T<5>$ becomes low. $Dly-clk2$ is generated from $CLK2$ signals after few buffer delays as shown on Fig.2.25. $Dly-clk2$ acts as comparator clock and in each cycle, one of the comparators' outputs will be high which generates the signal $Comp-clk$. $Comp-clk$ acts as the clock to the flops of the shift register and the shift register generates $T<0>-T<5>$ signals and after buffer delays $DFF\_CLK<5:0>$ are generated. So, the delay from comparator output to the DFF_CLK is:

OR-gate-delay+ FLOP-delay+ Buffer-delay.

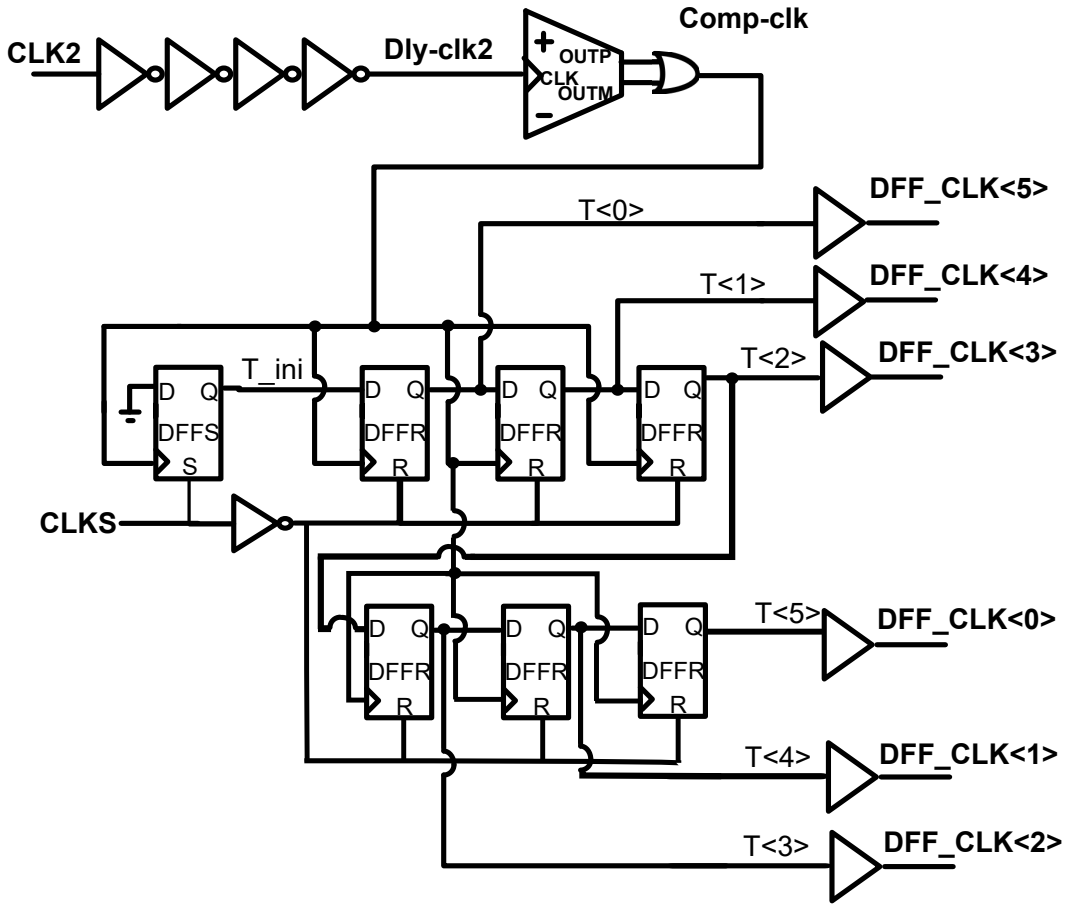


Figure 2.24: Clock generation circuit for 6-bit shift register.

2.6.3 MUX Logic

Fig.2.26 shows the circuit including the mux and the DFF. The 2:1 mux is used to select data between $FLOP\_out$ and $COMP\_out$.

The 2:1 mux consists of transmission gates and it is controlled by the CK, the same clock that goes to DFF and is generated from comparator output as discussed before. When RST is high, $FLOP\_out$ goes low and as CK is low, the

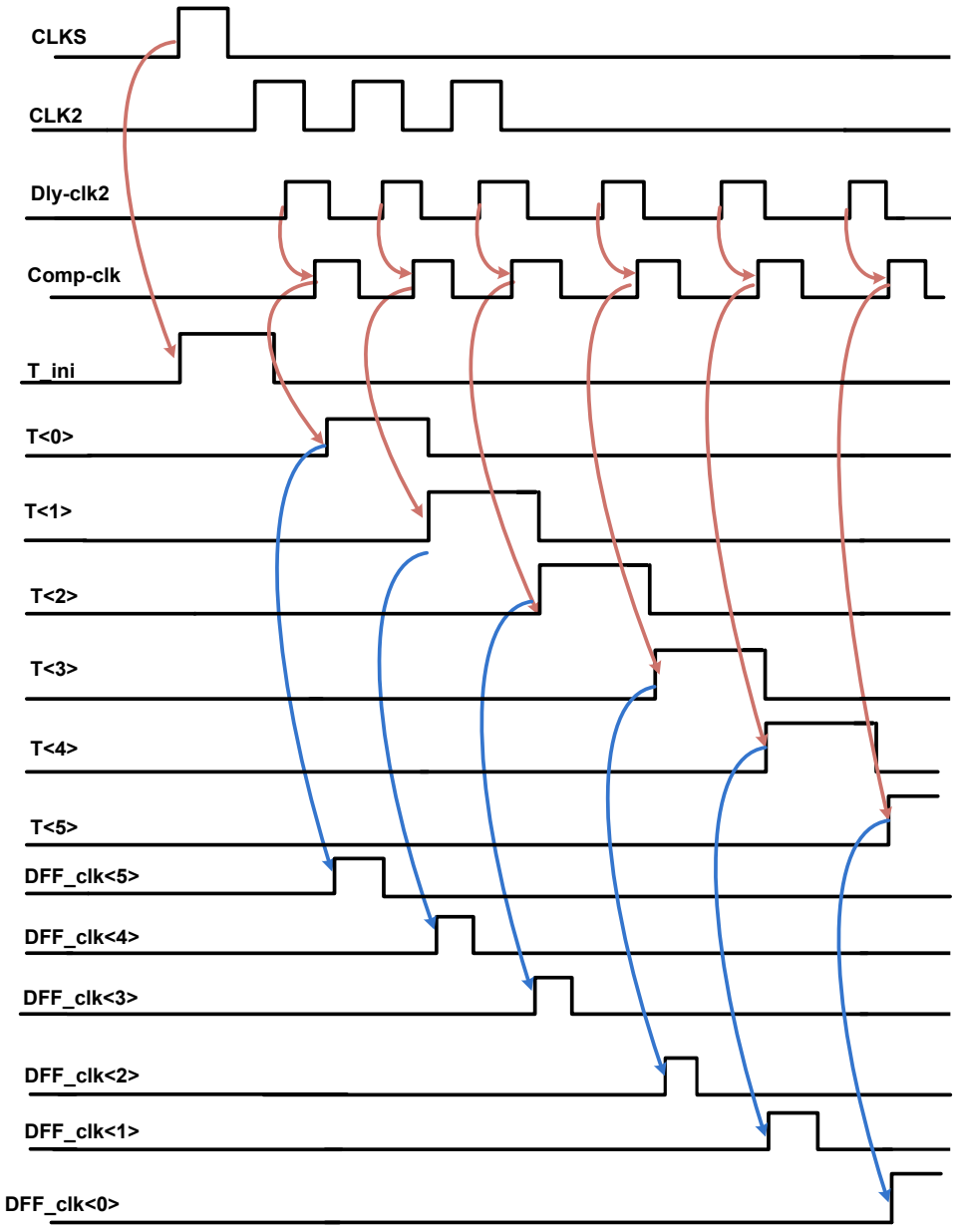


Figure 2.25: Clock generation timing diagram for 6-bit shift register.

mux transmits $FLOP\_out$ to the output and $Dout$ becomes low. When, comparator clock $Comp\_CLK$ is high, the comparator output will change and it will make

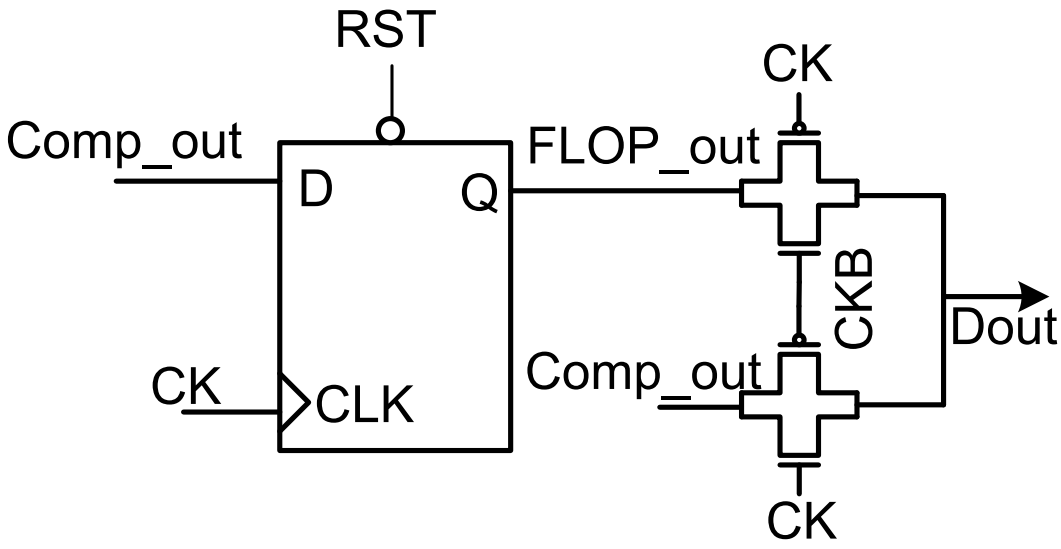


Figure 2.26: MUX circuit for radix-3 data out.

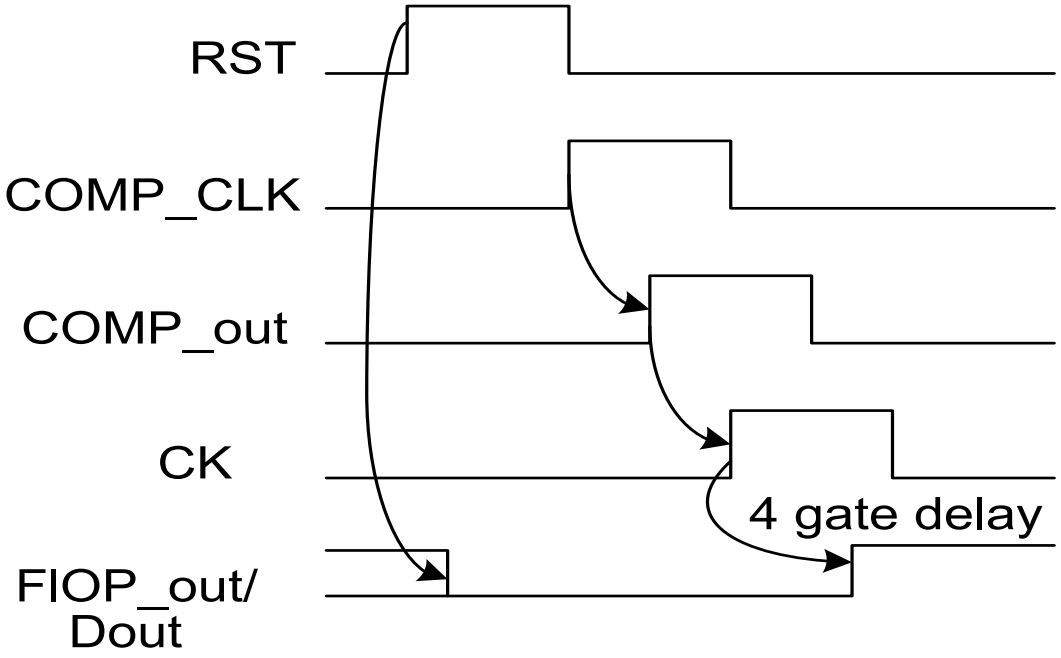


Figure 2.27: Clock to Dout delay with MUX.

CK high. When CK is high, the 2:1 mux will pass $COMP\_out$ and after the data has been latched to the DFF, CK will go low and the mux will pass $FLOP\_out$. So, from $COMP\_out$ to $Dout$ the delay is only one transmission gate. The detail timing diagram is shown on Fig.2.27. If there was no mux, the delay from $Comp\_out$ to $Dout$ is the flop delay which is 3-4 logic gates, depending on the design as shown on Fig.2.28. Simulation shows that a DFF with MUX logic becomes 40pS faster than a regular DFF.

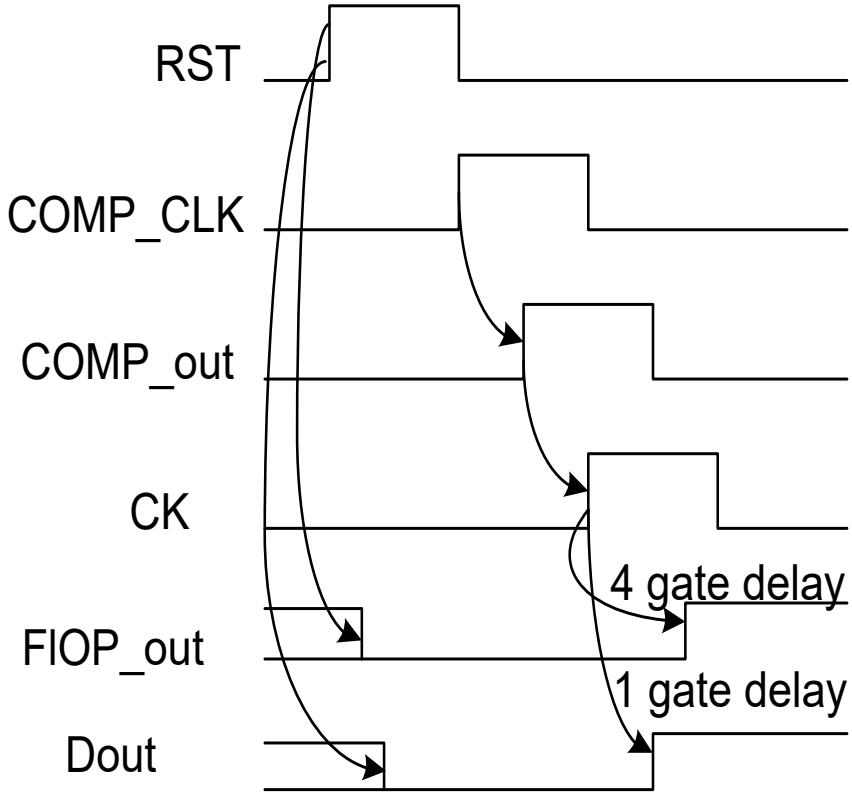


Figure 2.28: Clock to Dout delay without MUX.

2.6.4 Sample and Hold Circuit

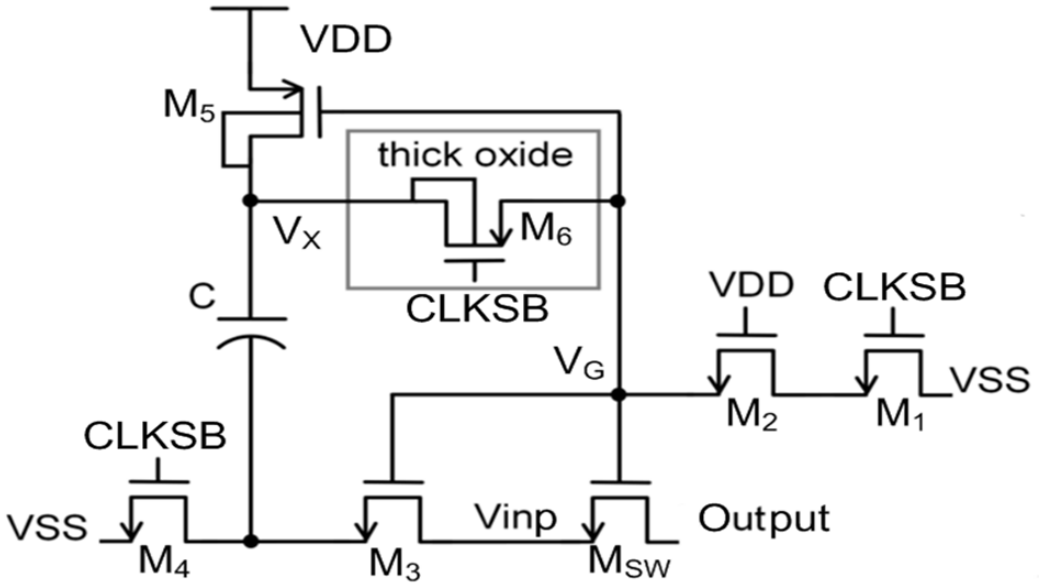


Figure 2.29: Schematic of bootstrapped sampling switch.

The input sampling switches are bootstrapped with the circuit shown in Fig.2.29 [Siragusa and Galton [2004]]. Bootstrapped switches are employed in the sampling circuit in order to achieve both smaller on-resistance and minimal signal-dependent sampling distortion. It is simple and does not require two complementary clock phases [Jiang et al. [2012]]. When the sampling clock $CLKSB$ is high, the switch M_4 is shorted to ground and the capacitor C is charged to near the supply voltage. When $CLKSB$ is low, the large voltage difference across the capacitor will be added to the input signal V_{inp} and then applied to the gate of the pass switch, making the gate-source voltage of the M_{sw} close to that high voltage constantly. In order to reduce the on-resistance of the bootstrapped switch such that the track and hold circuit can meet the hard timing requirement, the external supply

voltage connection is thoroughly considered during the layout. This circuit is carefully designed so that no voltage difference between any two nodes of a single MOS transistor is larger than the nominal supply voltage. But for safety purpose, a thick-oxide device, M_6, is used to tolerate a potential voltage higher than the nominal supply voltage. A more detailed description of designing and sizing the transistors is presented in next chapter.

2.6.5 Capacitor Switching Circuit

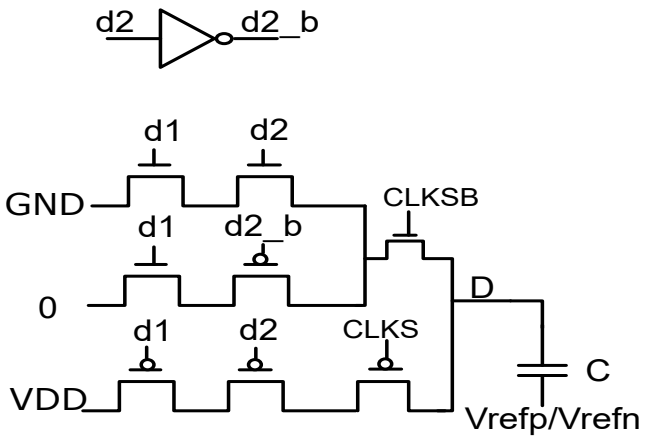


Figure 2.30: Capacitor switching circuit with transmission gate.

During radix-3 search, MSB capacitors need to be connected to V_{cm} and the rest of the capacitors should be connected to VDD. Also, depending on the comparator outputs, the capacitors can be connected to VDD, GND or V_{cm}. The traditional way to switch the capacitors is to use a transmission gate as shown in Fig.2.30 since logic gates (i.e. NAND or INVERTER) can only switch between VDD and GND. When $CLKS$ is high ($CLKSB$ is low), the switching circuit is disabled and no DATA is passed through the transmission gate. At the same time,

the boostrap switch will be activated and the sampled input voltage will be passed through the capacitors. When $CLKS$ is low ($CLKSB$ is high), the switching circuit is activated and at the same time, the boostrap switch will be deactivated. So, DATA will be transferred through the transmission gate and the capacitors will be connected to the required voltage level depending on the comparators' decisions.

2.6.6 Comparator Design and Offset Calibration

Fig.2.31 shows the dynamic comparator with offset calibration. By designing the comparator with low input referred offset compared to 1LSB voltage, we have eliminated the preamplifier in our design. It is a strong-ARM latch based design. Two variable MOS capacitors are added at the drain of input transistors $M11$ and $M12$ for calibration purpose. Comparator offset and decision time are two key parameters in this design.

All comparators have offsets and their offset mismatches degrade the ADC linearity. Thus, it is desirable to design a comparator with small offset and fast decision time. One important factor that influences both offset and decision time is the comparator input common-mode voltage V_{cm} [Wicht et al. [2004]]. A small V_{cm} is preferred to reduce the offset. The reason is that the pre-amplification gain is larger at small V_{cm}, which suppresses the offset contribution from the latch. A large V_{cm} helps reduce the pre-amplification time but the time duration of the latch regeneration phase is longer due to the reduction in the pre-amplification gain [Wicht et al. [2004]]. There exists an optimized V_{cm} for decision time.

Note that V_{cm} decreases slightly when the comparators are fired due to the

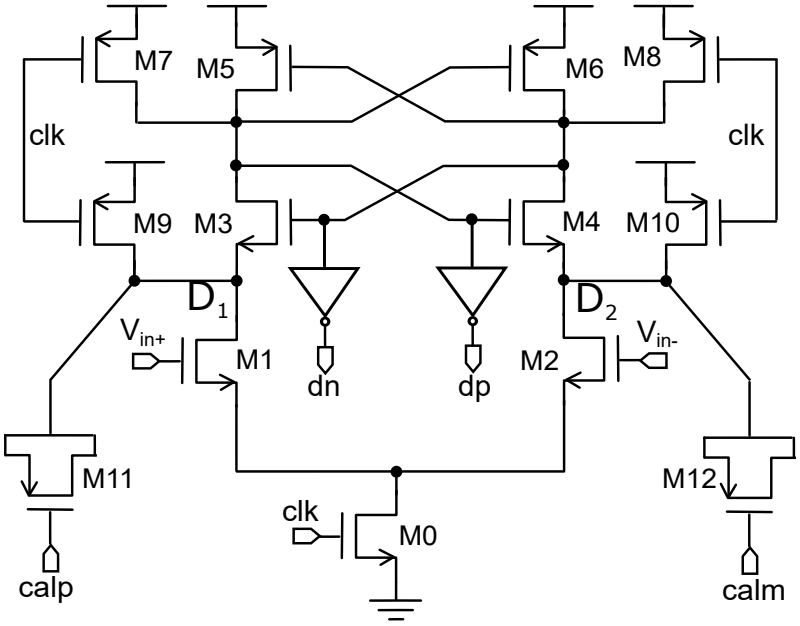


Figure 2.31: Dynamic comparator with varactor loading.

comparator kick-back noise. The kick-back noise is a common-mode noise to the first order, which does not disturb the settling of the comparator differential mode voltage. Thus, the kick-back noise does not degrade the linearity.

In the prototype ADC, the optimized comparator 1σ offset is $\sim$5mV. A 1000-point Monte-carlo simulation result is shown in Fig.2.32, with a mean of -684μV and 1σ of 4.76mV. To avoid linearity degradation due to offset mismatch, a V_{cm}-adaptive offset calibration technique is proposed.

As is shown in Fig.2.31, the proposed calibration block consists of a dynamic comparator, varactor and control pins. The control pins $calp$ and $calm$ are used to to change the voltage added to the gate of the calibration-MOS capacitor. The different feedback voltage on the gates of the load MOS would result in differ-

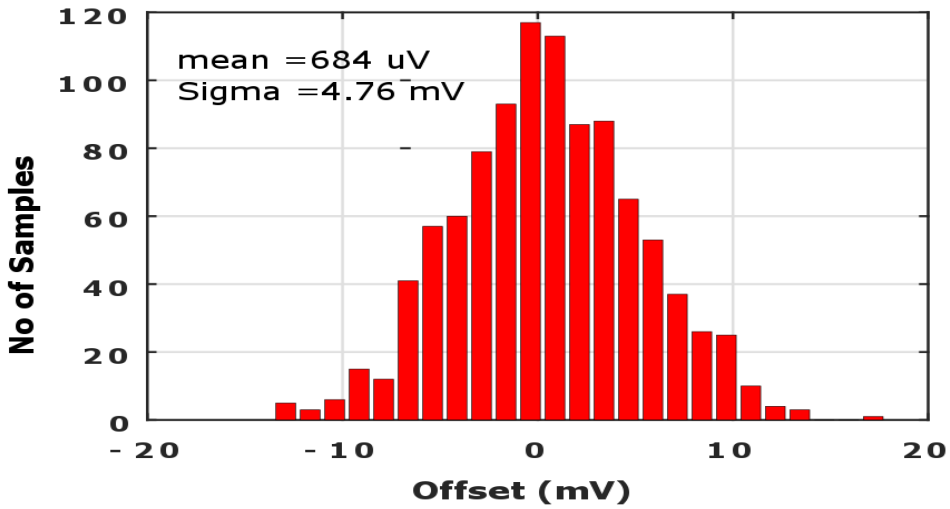


Figure 2.32: 1000-point Monte-carlo simulation for input referred offset of comparator.

ent capacitance values. By adjusting the output loads attached to the comparator, the offset would be compensated.

Fig.2.31 shows the proposed comparator with real-time calibration. Two NMOS varactors M_{11} and M_{12} are attached to the internal nodes D_1 and D_2.

The calibration technique works as follows. When the ADC is in the calibration mode, the calibration signal ($OFFSET\_CALIBRATION$=1) is assigned from external control. That keeps the signal $CLKSE$ high during the whole calibration period and positive and negative terminals of the comparators are connected to V_{cm} (see Fig.2.33) and hence, a zero differential input voltage is applied to the inputs of comparators. For simplicity of design, we do not need any external clock or extra circuitry for this calibration procedure. As our design is fully synchronous, we just slow down the external clock to give the comparators enough time so that its dif-

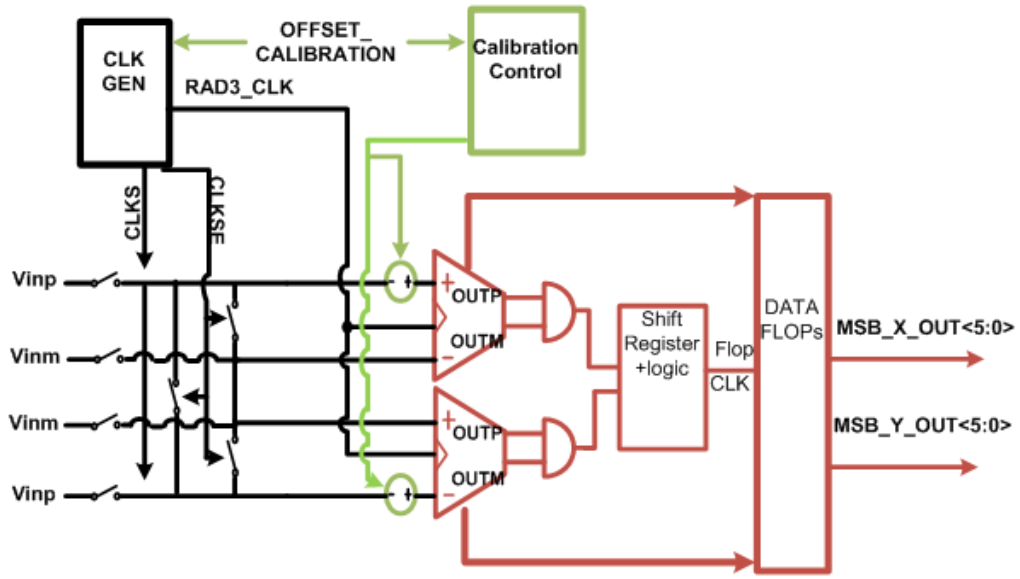


Figure 2.33: Comparator calibration scheme in proposed radix-3 SAR ADC.

ferential inputs settle well and stay close to zero. Fig.2.34 shows the timing diagram of calibration. $CLKS$ turns on for one clock cycle as usual convergence operation, but does not affect the input voltage of the comparators. $CLKS$ needs to be high to reset all the DATA flops and shift registers in each conversion time. $RAD3\_CLK$ toggles 6 times as usual operation, but at a much slower frequency as described earlier. As a result, comparators will toggle and their outputs will be latched at the output flops. Radix-3 comparators provide outputs $MSB\_X\_OUT < 5:0 >$ and $MSB\_Y\_OUT < 5:0 >$.

If there is no offset, each comparator's output jumps between "1" and "0" due to thermal noise. Comparator thermal noise in the design is about 400μV, which is much smaller than the offset. When a large offset is present, the comparator's

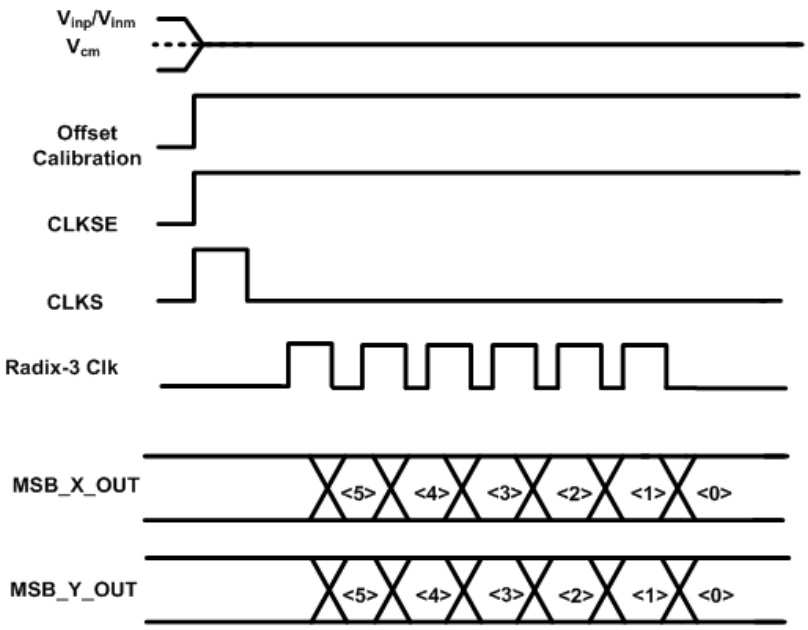


Figure 2.34: Timing waveform for calibration of comparator offset.

output keeps staying at either "1" or "0" as shown in Fig.2.35. The offset can be calibrated by tuning the MOSFET based varactors shown in Fig.2.31, whose values are controlled by its gate voltage $calp/calm$. Supposing that node D_1 is discharged faster than node D_2 caused mainly due to the mismatch of input transistors M_1, M_2 according to [Harpe et al. [2014]], it means that the comparator output d_p would reach GND and d_n would reach VDD even if the differential input signal is zero (V_{in+}=V_{in-}).

To compensate for this offset, the gate voltage of M_{11} is reduced with external potentiometer control knob in the calibration unit. By doing this, the capacitance of M_{11} connected to node D_1 will be increased according to the curve shown

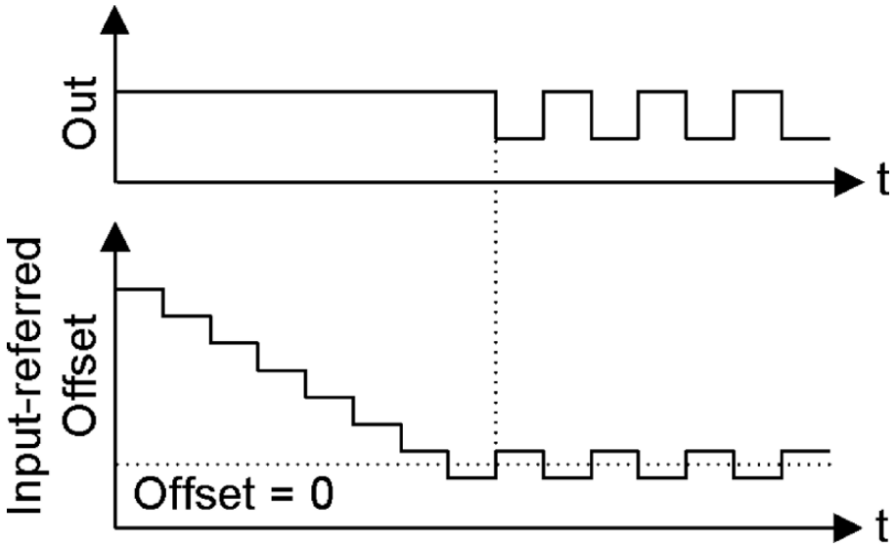


Figure 2.35: Timing waveform of change of input offset of comparator.

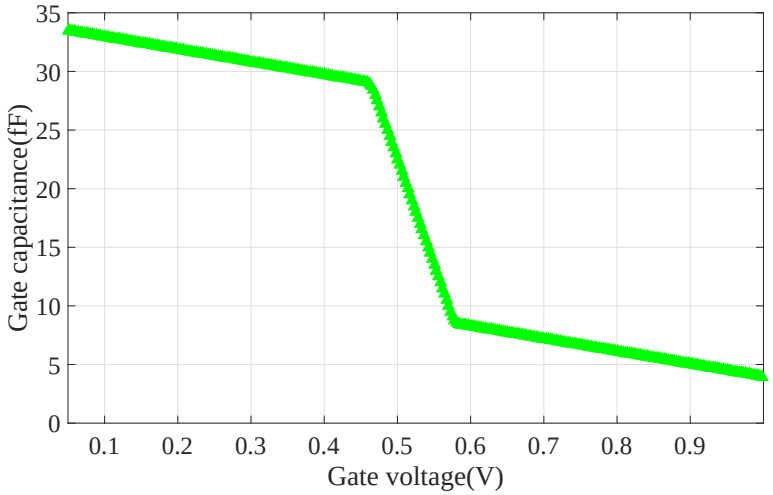


Figure 2.36: MOSFET gate capacitance variation vs control voltage.

in Fig.2.36. The larger capacitance load of node D_1 apparently will cause its discharging speed to be slower during the next cycle. Similarly, the complementary

voltage to the gate of M_{12} will be changed in the opposite way. At last, the mismatch of the discharging speed of nodes D_1 and D_2 will be reduced to minimal. The offset caused by device mismatch will be calibrated. The calibration range is designed to be 20mV which is 3 times the simulated 1σ offset. By observing the comparator's output, we can tell whether the comparator offset has been calibrated or not. The calibration is finished when the comparator output is evenly distributed between "1" and "0" (Fig.2.35).

2.7 SPICE Simulation Results

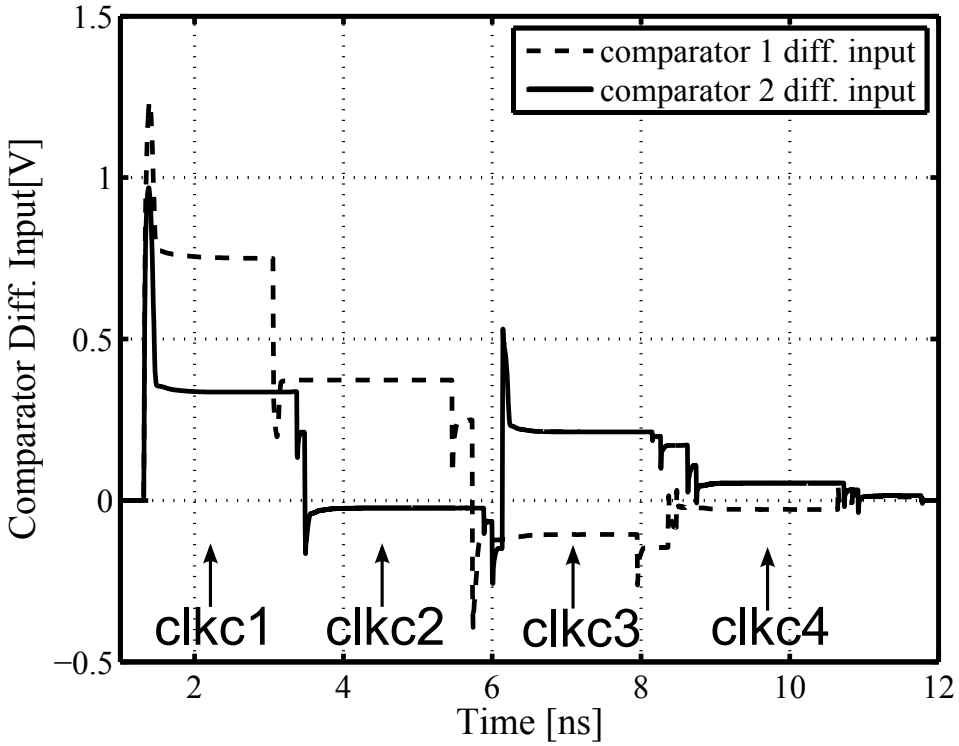


Figure 2.37: Residue voltage of 4-ternary-bit radix-3 SAR ADC.

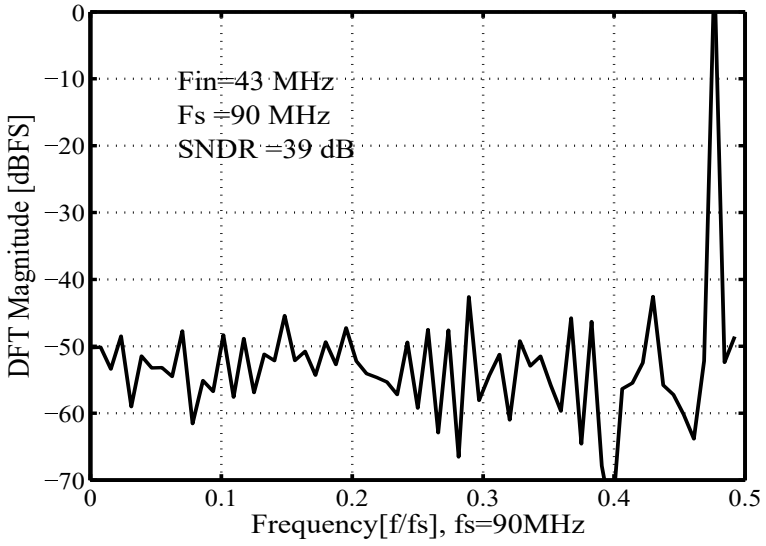
To verify our idea, a 4-ternary-bit radix-3 SAR ADC is designed in 180nm CMOS technology with a 1.8V power supply. At the beginning of the design, during the SPICE simulation, the capacitive DAC mismatch and the comparator offset mismatch are not considered.

An example of $V_{in} = -0.225$V, which corresponds to the digital input $-0.225/0.9 = -1/4$ of Fig.2.6, is given as the input signal to the radix-3 SAR ADC. Since we use 0V to indicate logic '-1' and use 1.8V to indicate logic '1', $D_{out} = -20/81$ represents the analog input: $-20/81 \times 0.9V = -0.22$V. The quantization error is -0.225V$-(-0.22)$V$= -0.005$V which meets the 4 ternary bits accuracy. Fig.2.37 shows the SPICE simulation result of the differential input $V_{resp} - V_{resn}$ of the two comparators. The comparator differential input reduces every comparison cycle and is within 1 LSB at the end of *clkc4*.

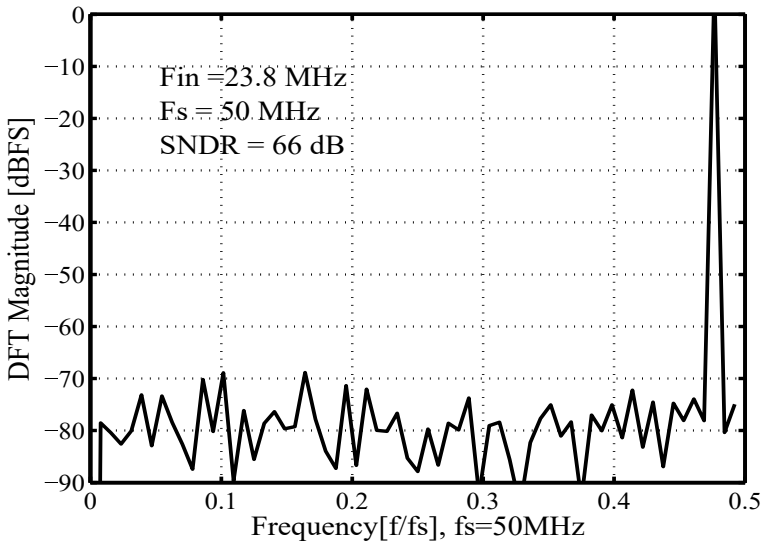
The 128 point FFT plot of the 4-ternary-bit radix-3 SAR ADC simulated with $(61/64)\times 45$MHz input and 90MHz sampling frequency is shown in Fig.2.38(a). The SNDR is 39 dB which is about 6.2 binary bits.

Another 128 point FFT plot of the 7-ternary-bit SAR ADC simulated with $(61/64) \times 25$MHz input and 50MHz sampling frequency is shown in Fig.2.38(b). The SNDR is 66 dB which corresponds to 10.7 binary bits. The results match well with the theoretical analysis.

To verify the calibration algorithm, the calibration of a 7-bit radix-3 SAR ADC is also designed in 180nm CMOS technology with 1.8V power supply. Capacitance mismatch is modeled by the standard deviation. The amplitude of the sine



(a)



(b)

Figure 2.38: FFT plots of (a) 4-ternary-bit (b) 7-ternary-bit radix-3 SAR ADC.

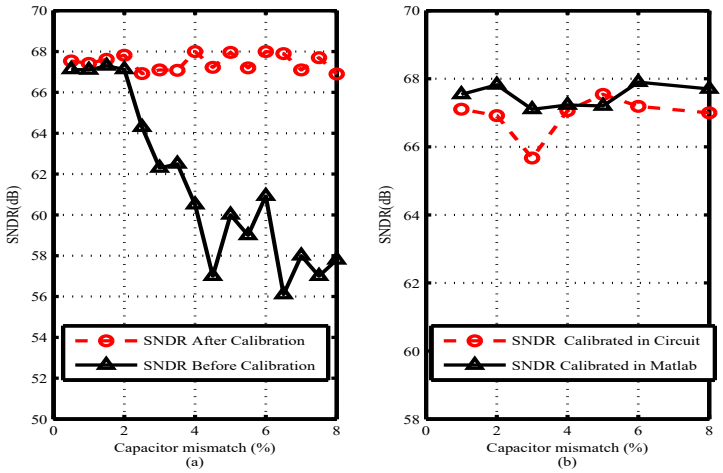


Figure 2.39: (a) SNDR of radix-3 SAR before and after calibration. (b) comparison of calibration results based on SPICE and MATLAB.

wave input signal is 1.7 V peak. The capacitor ratio error was varied from 0.5% to 8% and each time the SNDR was calculated. Fig.2.39(a) shows SNDR of raidx-3 before and after calibration from MATLAB based simulation. With the increment of statistical variation of capacitors, SNDR falls sharply without calibration, but with calibration, the SNDR is held around 67 dB.

The SNDR found from circuit based SPICE simulation and the SNDR from MATLAB based simulation are plotted in Fig.2.39(b). The plot in Fig.2.39(b) shows that circuit based result closely follows Matlab simulation result and verifies the calibration idea, when a standard DAC capacitance deviation is taken up to 8%.

The 128 point FFT plot of a 7-ternary-bit SAR ADC simulating with sampling frequency 25 MHz and with a 5% mismatch is shown in Fig.2.40. The SNDR

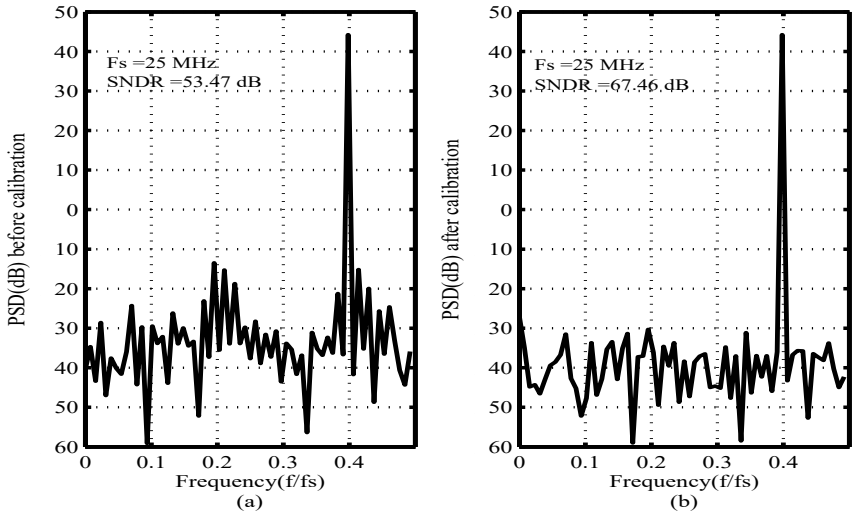


Figure 2.40: FFT of radix-3 SAR with 5% mismatch (a) before calibration (b) after calibration.

is 53.47 dB before calibration and 67.46 dB after calibration. From the circuit, with up to 10% mismatch, a SNDR of around 67dB was found which verifies the proposed calibration algorithm. The proposed calibration performance is compared with other techniques in Table 2.3. The main advantage of this work is that it does not require any extra capacitor DAC and can help achieve ENOB which will be close to resolution.

Table 2.3: Comparison of calibration of ADCs.

ADC	SAR Arch	Tech (nm)	Sample (MS/s)	SNDR (dB)	Extra DAC	Reso-lution	ENOB
Kuramochi et al. [2007]	Conventional	180	1	51.2	Yes	10	8.2
Yanfei et al. [2010]	Split Cap	65	50	45.8	Yes	8	7.3
Yoshioka et al. [2010]	Split Cap	130	50	56.63	Yes	10	9.1
Li et al. [2012]	Conventional	N/A	0.01	60.8	Yes	10	9.8
Xu et al. [2012]	Conventional	180	0.768	61.1	None	10	9.83
This Work	Radix-3	180	25	67.46	None	11.2	11.01

2.8 Conclusion

In this chapter, we introduced an efficiently controlled radix-3 SAR ADC. We also characterized the ADC and proposed a simple calibration technique for the input referred offset of the comparator. Comparator calibration does not require any circuit overhead and can be easily controlled with two external pins. A digital calibration technique is also presented for the radix-3 SAR ADC. The main advantage of this architecture is that it does not need any extra capacitor DAC array and the calibration circuit is programmable for any size of DAC array with a small digital circuit overhead. Theoretical analysis and circuit based simulation also verified the proposed idea.

Chapter 3

Radix-3/Radix-2 Based Hybrid SAR ADC

This chapter presents a fast converging hybrid successive approximation register (SAR) analog-to-digital converter (ADC) based on the radix-3 and radix-2 search approach. The radix-3 approach achieves 1.6 bits/cycle. It offers significant speed gain over a traditional radix-2 SAR ADC, but it comes at the cost of more DAC power, control switch power and flipflop powers. Also, due to the architecture, it uses two comparators simultaneously and as a result, it burns more comparator power than a radix-2 SAR ADC and the mismatch between comparator offsets can limit the resolution of the radix-3 SAR ADC. The radix-2 approach mitigates the effect of comparator offset and improves the accuracy of the ADC. Also, incorporating monotonic switching of [Sanyal and Sun [2014]], the radix-2 approach can lower the DAC power and the power of switching-control circuit, as it reduces the required capacitance in the DAC by 4 times for the same resolution.

Again, incorporating clock gating of the comparators and efficient switching of capacitors, the proposed hybrid ADC demonstrates a promising balance be-

[1]This chapter is a partial reprint of the publication: Manzur Rahman, Arindam Sanyal, and Nan Sun, "A novel hybrid radix-3/radix-2 SAR ADC with fast convergence and low hardware complexity," *IEEE* Transactions on Circuits and Systems II: Express Briefs (*TCAS-II*), vol. 62, no. 5, pp.426-430, May 2015. I did the modeling, design, and testing of the prototype. I also thank other co-authors for their valuable advice.

tween hardware complexity and speed and can achieve equivalent signal-to-noise-and-distortion-ratio (SNDR) with less capacitors compared to a radix-3 SAR ADC. Behavioral simulation based results verify the operation and merit of the proposed architecture. A 9.5-bit radix-3/radix-2 hybrid SAR ADC was designed in a 40nm CMOS process to prove the concept.

This chapter is organized as follows: an introduction of existing high speed SAR ADC design techniques is first presented in the literature review section. The proposed SAR ADC architecture is shown next. Then we present the characterization of the proposed hybrid SAR ADC. Next, we propose the calibration algorithm of capacitor mismatch in DAC. Finally, the prototype ADC implementation and calibration of comparator offset are presented.

3.1 Literature Review

High-speed low-resolution analog-to-digital converters (ADCs) are required by many demanding applications, such as high speed serial link transceivers and communication systems. Compared with pipelined and $\Delta\Sigma$ ADCs, SAR ADCs are more power efficient and scaling friendly due to their mostly digital architecture. Several techniques have been developed to increase the speed of SAR ADCs [Chen et al. [2013]; Chen and Brodersen [2006]; Hong et al. [2015]; Kull et al. [2013]; Lin et al. [2010]; Tai et al. [2014.]; Verbruggen et al. [2012]; Wei et al. [2012]; Yang et al. [2010]], and [Jiang et al. [2012]]. To have different time durations of each comparison cycle, the first asynchronous SAR ADC was proposed in [Chen and Brodersen [2006]]. To save comparator reset time, using alternate comparators

was proposed in [Kull et al. [2013]]. Other effective high-speed techniques in SAR ADCs such as pipelining two-stage SAR ADCs was proposed in [Tai et al. [2014.]]. Recently, several works arrange multiple comparators to further increase the speed [Chen et al. [2013]; Lin et al. [2010]; Verbruggen et al. [2012]], and [Jiang et al. [2012]]. A binary-search ADC was proposed in [Lin et al. [2010]], which describes a transitional structure between flash and SAR ADCs. However, the hardware cost is high in [Lin et al. [2010]] as this technique requires additional switching networks and $2N-1$ comparators for an N-bit design. The loop-unrolled architecture of [Verbruggen et al. [2012]], and [Jiang et al. [2012]] employs a dedicated comparator for each comparison cycle. The comparison result is stored directly at the comparator output. As a result, the SAR logic is greatly simplified, leading to reduced power and delay. Although more comparators are used compared to the conventional SAR architecture, the total comparator power does not increase since each of them is fired only once during the whole conversion. Nevertheless, the comparator common-mode voltage V_{cm} varies significantly and eventually goes to V_{DD} in [Verbruggen et al. [2012]], and [Jiang et al. [2012]], resulting in large comparator offsets and reduced linearity. Both [Verbruggen et al. [2012]] and [Jiang et al. [2012]] require complicated calibrations for comparators' offset mismatches, which increase both the power consumption and the design complexity.

The SAR ADC speed can also be improved by using multi-bit-per-cycle architectures to reduce the number of comparisons, however at the cost of increased hardware complexity. [Thirunakkarasu and Bakkaloglu [2010]] introduced a radix-3 SAR ADC which resolves 1.6 bits/cycle. For N ternary bits, the number of capac-

itors is 4×3^N. Due to complexity of control, it is not applicable for high resolution applications. No calibration of capacitor mismatch was done, which also limits the resolution. [Cao et al. [2009]] proposed a radix-4 SAR ADC which produces 2 bits per step. For N binary bits, the number of capacitors is 6×2^N. It requires three differential DACs. It's power hungry architecture also limits the resolution. [Hong et al. [2012]] presents a 2 bits per cycle SAR ADC with a new design approach, but it produces 1.75 binary bits/cycle on average. It also requires an extra reference DAC. Three comparators/cycle are used for this architecture. Also, lots of extra digital circuits are required for post processing. [Hong et al. [2013]] presents another efficient 2 bits per cycle SAR ADC, but it produces 1.5 binary bits/cycle on average due to redundancy. It also requires an extra reference DAC as well. On average 2.5 comparators/cycle (maximum 3 comparators/cycle) are used for this architecture. Also, lots of extra digital circuits are required for post processing. [Hong et al. [2015]] presents another efficient 2.6 bits per cycle SAR ADC, but it produces 1.25 binary bits/cycle on average. It also requires two extra reference DACs as well. On average 3 comparators/cycle (maximum 5 comparators/cycle) are used for this architecture. Also, lots of extra digital circuits are required for post processing. [Wei et al. [2012]] also proposes a 2 bits per cycle architecture, but it requires five comparators, a power hungry resistive DAC and lots of post processing and calibration of the DAC and comparators.

This work proposes a novel fast converging hybrid successive approximation register (SAR) analog-to-digital converter (ADC) based on a combined radix-3 and radix-2 search approach. The Radix-3 approach allows multi-bit per cycle with

the expense of one extra comparator and same number of DACs as we will be using in a single ended structure for the radix-2 search. During the radix-2 approach, we use a differential structure and one single comparator and we incorporate a very power efficient monotonic switching scheme. The radix-2 approach mitigates the effect of comparator offset and improves the accuracy of the ADC and lowers the overall conversion power. Also, to further improve the linearity, a novel offset calibration technique is proposed to calibrate the comparators' offset mismatch. The proposed calibration technique has very low hardware complexity. It can calibrate the comparator offset at its operating V_{cm} following the proposed switching procedure. A prototype ADC is designed in 40nm CMOS process. SPICE simulation shows that it can achieve 58.1 dB SNDR at a sampling rate of 200 MS/s, while consuming only 1.4mW of power from a 1.1V supply.

3.2 Proposed SAR ADC Architecture

3.2.1 Comparison Levels

An in depth review of comparison levels is important to understand the architecture of any ADC. For that purpose, Fig.3.1 presents the comparison levels of the proposed hybrid SAR ADC containing 2 ternary and 2 binary bits. As it is known, the radix-3 architecture will always compare with $1/3$ and $2/3$ of input range and radix-2 architecture will always compare with $1/2$ of the input range. Assuming the input voltage $V_{in} \in [-1, 1]$, in first cycle it is compared against $1/3$ and $-1/3$ and one ternary bit is resolved in cycle1. In cycle2, the comparison levels can be $(-7/9, -5/9)$ or $(-1/9, 1/9)$ or $(5/9, 7/9)$ and another ternary bit will be

resolved. In cycle3, the radix-2 search algorithm will be applied and the comparison level will be the half of the residue voltage. For example, if the $V_{in} \in [1, 7/9]$, then the comparison level is $8/9$ and so on. So, in cycle3 and cycle4, two binary bits are resolved. Hence, total $(2 \times 1.6 + 2 \times 1) = 5.2$ binary bits are achieved from 4 cycles.

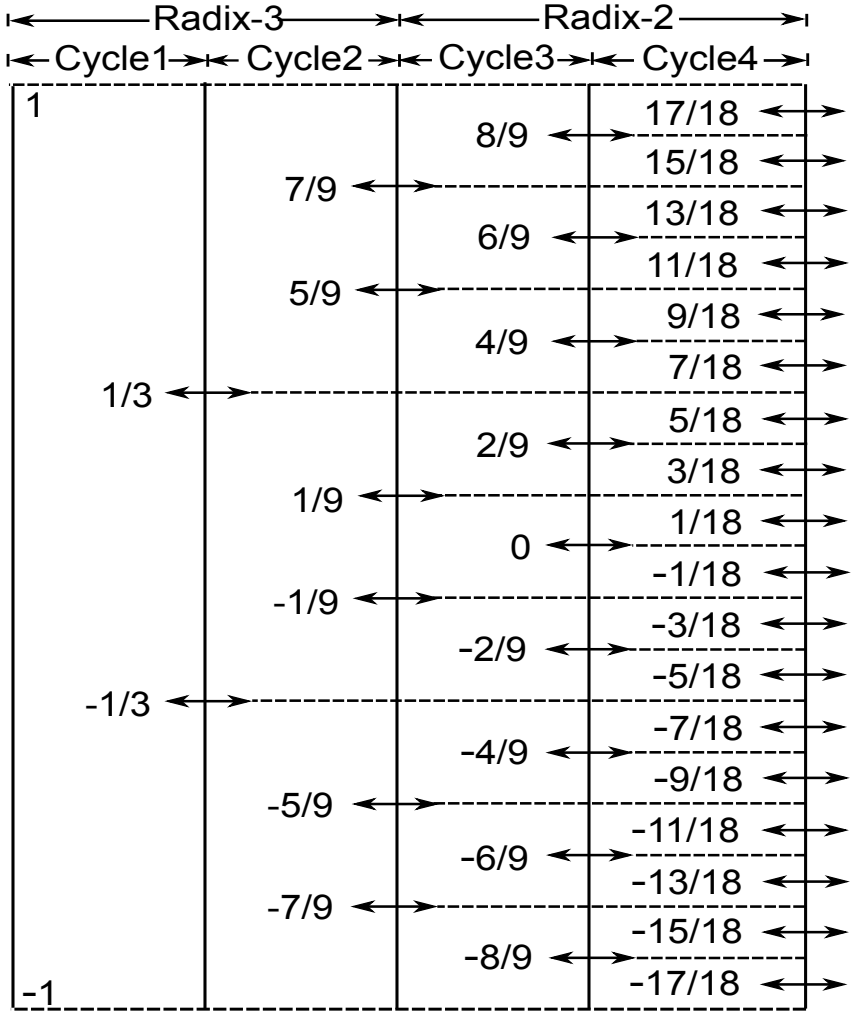


Figure 3.1: Reference voltage levels of the proposed hybrid ADC architecture.

3.2.2 Circuit Architecture and Operation

In this subsection, we explain the circuit architecture of the hybrid SAR ADC. As the architecture is derived from the radix-3 and the radix-2 SAR architecture, we revisit those two architectures first. A conventional 5-ternary bit radix-3 ADC circuit implementation is shown in Fig.3.2. In this ADC, two comparators $\text{Comp}_{1,2}$ and four capacitor DACs, $\text{DAC}_{1,2,3,4}$ are used to perform the differential ternary search. Hence, a total of 5 cycles are required to produce $(5 \times 1.6) = 8$ binary bits. As we discussed in previous chapter, the value of capacitors in the capacitor array are:

$$C_n = \begin{cases} 2 \cdot 3^{n-2} C_{unit} & \text{if } n > 1 \\ C_{unit} & \text{if } n = 1 \end{cases} \tag{3.1}$$

where C_{unit} is the unit capacitor.

Fig.3.3 shows the proposed hybrid SAR ADC containing 3-ternary-bits and 3-binary-bits with $\sim 78\%$ less capacitance of the radix-3 SAR ADC. In the proposed ADC, two comparators $\text{Comp}_{1,2}$ and two capacitor DACs, $\text{DAC}_{1,2}$, are used to perform the single ended ternary search. During radix-3 search, capacitors C, C and $2C$ of $\text{DAC}_{3,4}$ act as a single LSB capacitor of $4C$ for $\text{DAC}_{1,2}$. So, the values of capacitors of $\text{DAC}_{1,2}$ are $72C, 24C, 8C, 4C$ and produce 4.8 binary bits in 3 comparison cycles. Also, $\text{DAC}_{3,4}$ and Comp_3 are used to perform a differential radix-2 search. Hence, a total of 6 cycles are required to achieve 7.8 binary bits.

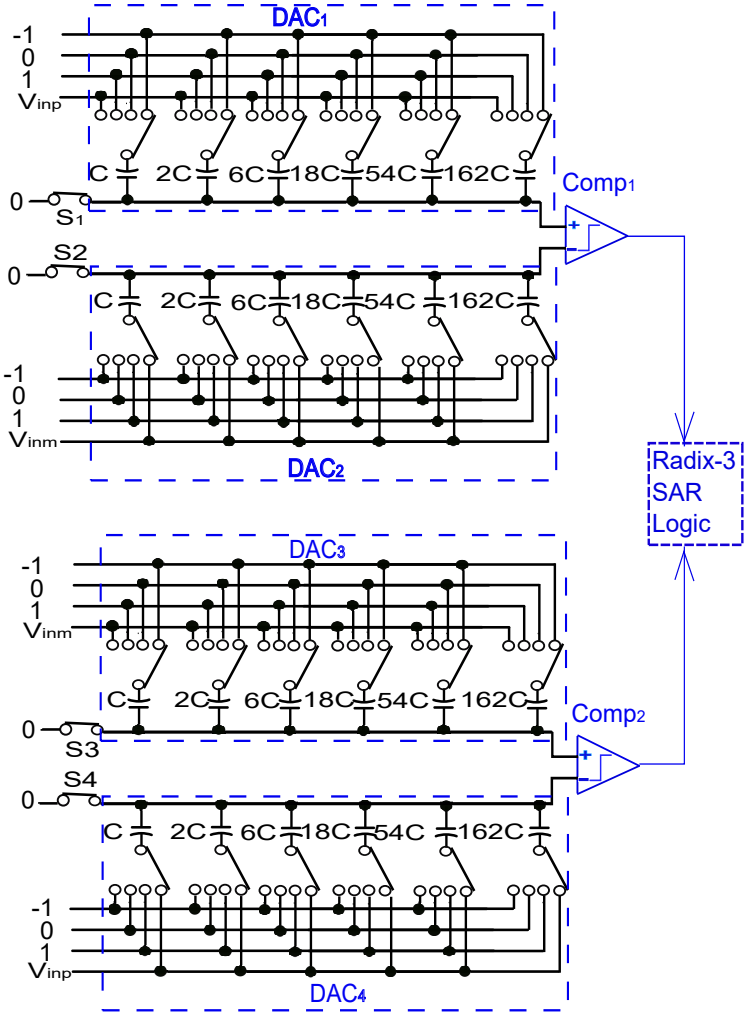


Figure 3.2: Conventional radix-3 SAR ADC.

To illustrate the circuit level operation, it is assumed that an input voltage '$\frac{55}{108}$' is sampled across the DACs. In the first comparison cycle, ϕ_1, capacitor 72C of $DAC_{1,2}$ are connected to '0' and rest of the capacitors are connected to '1' which generate two reference levels '$\frac{1}{3}$' and '$-\frac{1}{3}$'. Comparators outputs (d_1, d_2) become $(-1, -1)$ and a simple logic circuit converts that to single control inputs D_1 and D'_1

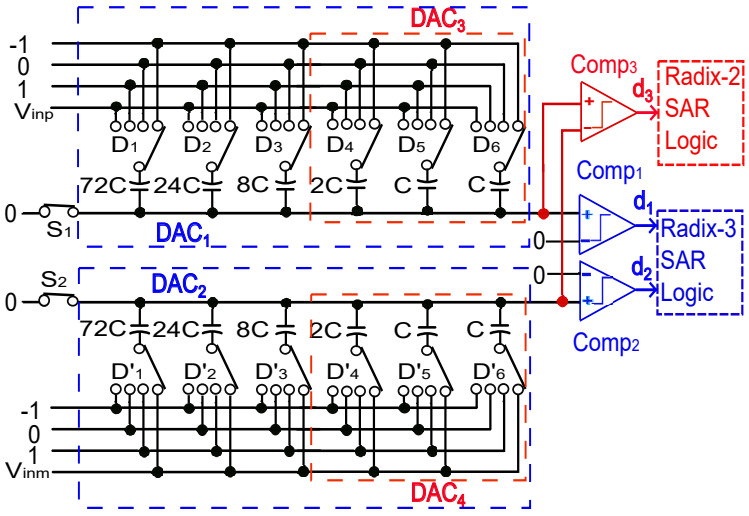


Figure 3.3: Proposed radix-3/radix-2 based hybrid SAR ADC.

for the MSB capacitors of DAC_1 and DAC_2 respectively. Thus the first 1.6 bits are obtained in cycle ϕ_1. In a similar manner, 3.2 binary bits are obtained in $\phi_2 - \phi_3$. In $\phi_4 - \phi_6$, a radix-2 search is completed using the monotonic switching scheme of [Sanyal and Sun [2014]] and 3 binary bits are obtained. The detail conversion steps including the comparison levels are illustrated in Fig.3.4.

Fig.3.3 can be expanded for a $(N + M)$-bit hybrid SAR ADC containing N-ternary-bits and M-binary-bits. Defining C_u as sum of all capacitors of $\text{DAC}_{3,4}$ and also as unit capacitor of $\text{DAC}_{1,2}$ and C_i as the value of i-th individual capacitor of DACs, we have:

$$C_u = \sum_{l=1}^{M} C_l \tag{3.2}$$

$$C_i = \begin{cases} 2 \cdot 3^{i-M-1} C_u & \text{if } M+1 \leq i \leq N+M \\ \frac{2^{i-2}}{2^{M-1}} C_u & \text{if } 1 < i \leq M \\ \frac{1}{2^{M-1}} C_u & \text{if } i = 1 \end{cases} \tag{3.3}$$

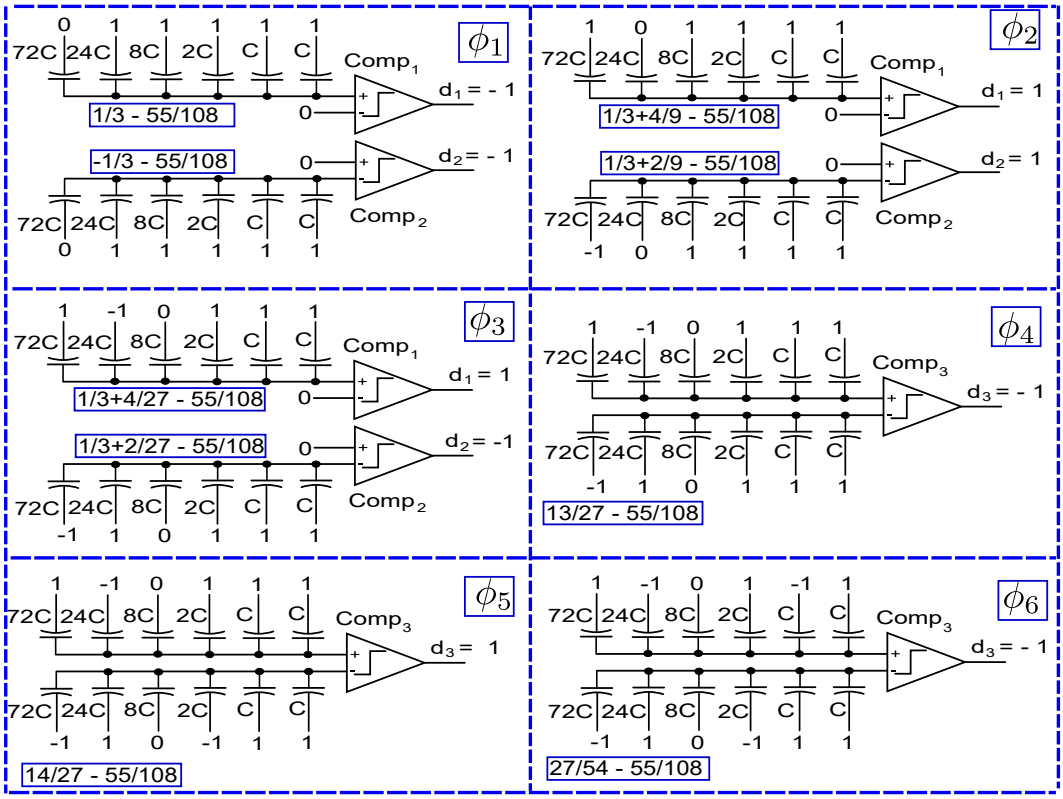


Figure 3.4: Proposed hybrid ADC's conversion steps for input voltage of '55/108'.

Fig.3.5 explains the residual voltages of the proposed ADC. In the first comparison cycle, $V_{in} \in [1/3, 1]$ range and (d_1, d_2) become $(-1, -1)$ and SAR digital codes (D_1, D'_1) according to Table 3.1 become $(1, -1)$.

In the second comparison cycle, $V_{in} \in [5/9, 1/3]$ which is $[-1, -1/3]$ of residue voltage range and (d_1, d_2) become $(1, 1)$ and SAR digital codes (D_2, D'_2) according to Table 3.1 become $(-1, 1)$.

In the third comparison cycle, $V_{in} \in [15/27, 11/27]$ which is $[-1/3, 1/3]$ of

Table 3.1: Binary codes from radix-3 comparators' output.

d_1	d_2	*Region*	D_i
0	1	$V_{in} \in [1/3,\ 1]$	1
1	1	$V_{in} \in [-1/3,\ 1/3]$	0
1	0	$V_{in} \in [-1, -1/3]$	-1
0	0	*not Possible*	–

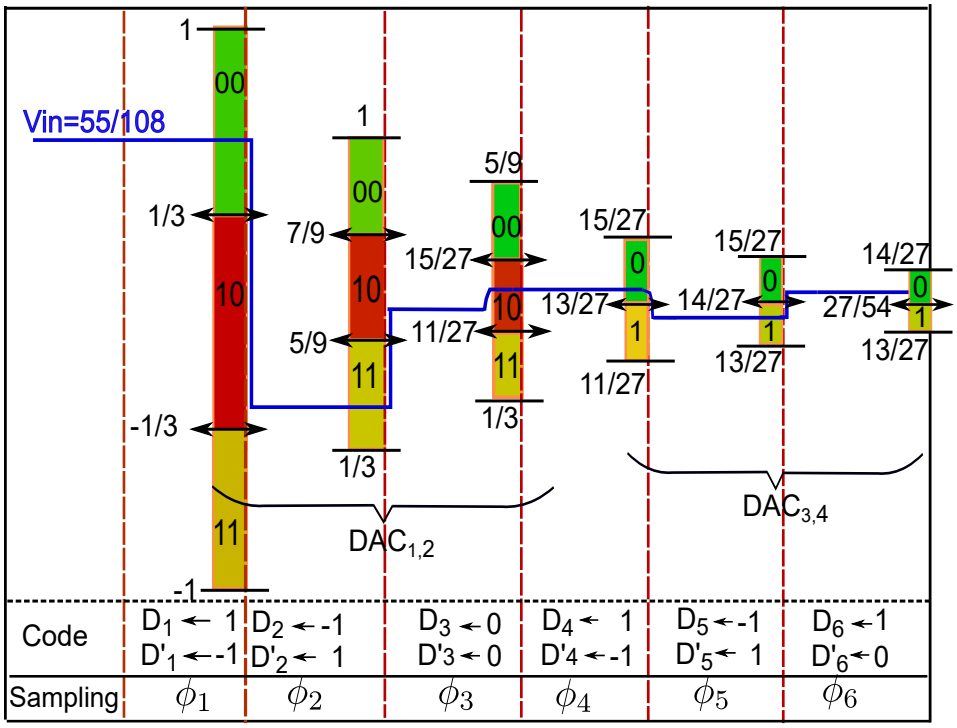


Figure 3.5: Sampling and comparison phases for (3+3) bit hybrid SAR ADC.

residue voltage range and (d_1, d_2) become $(1, -1)$ and SAR digital codes (D_3, D'$_3$) according to Table 3.1 become $(0, 0)$.

In the fourth comparison cycle, $V_{in} < 13/27$ which is $1/2$ of residue voltage range and d_3 becomes -1 and SAR digital codes (D_4, D'$_4$) become $(1, -1)$.

In the fifth comparison cycle, $V_{in} > 14/27$ which is $1/2$ of residue voltage range and d_3 becomes 1 and SAR digital codes (D_5, D'$_5$) become $(-1, 1)$.

In the sixth comparison cycle, $V_{in} > 27/54$ which is $1/2$ of residue voltage range and d_3 becomes -1 and SAR digital codes (D_6, D'$_6$) become $(1, -1)$.

Thus after all the comparisons, we have 3 ternary bits D_1 to D_3 and 3 binary bits D_4 to D_6. In total we have, $3 \times 1.6 + 3 \times 1 = 7.8$ binary bits from 6 comparison cycles.

Fig.3.6 shows the flow diagram of the conversion steps of an $(N + M)$-bit hybrid SAR ADC containing N ternary and M binary bits. The convergence starts at the MSB bit which is the $N + M$-th bit and the radix-3 search continues until the $N + M - 1$-th bit. Each bit, before convergence, is assigned $'0'$ and rest of the bits are assigned $'1'$. As shown in Fig.3.2, two comparators will be used in radix-3 search. After the comparator decision, digital codes (D_i, D_i') are generated based on Table 3.1 values. After N conversion cycles, from M-th bit to the LSB bit, the radix-2 monotonic switching search is applied. One more improvement compared to [Sanyal et al. [2015]] is that we do not switch any of the radix-2 capacitors during the radix-2 comparison. After the comparison is done by the radix-2 comparator, the output codes are generated as shown in the flow diagram.

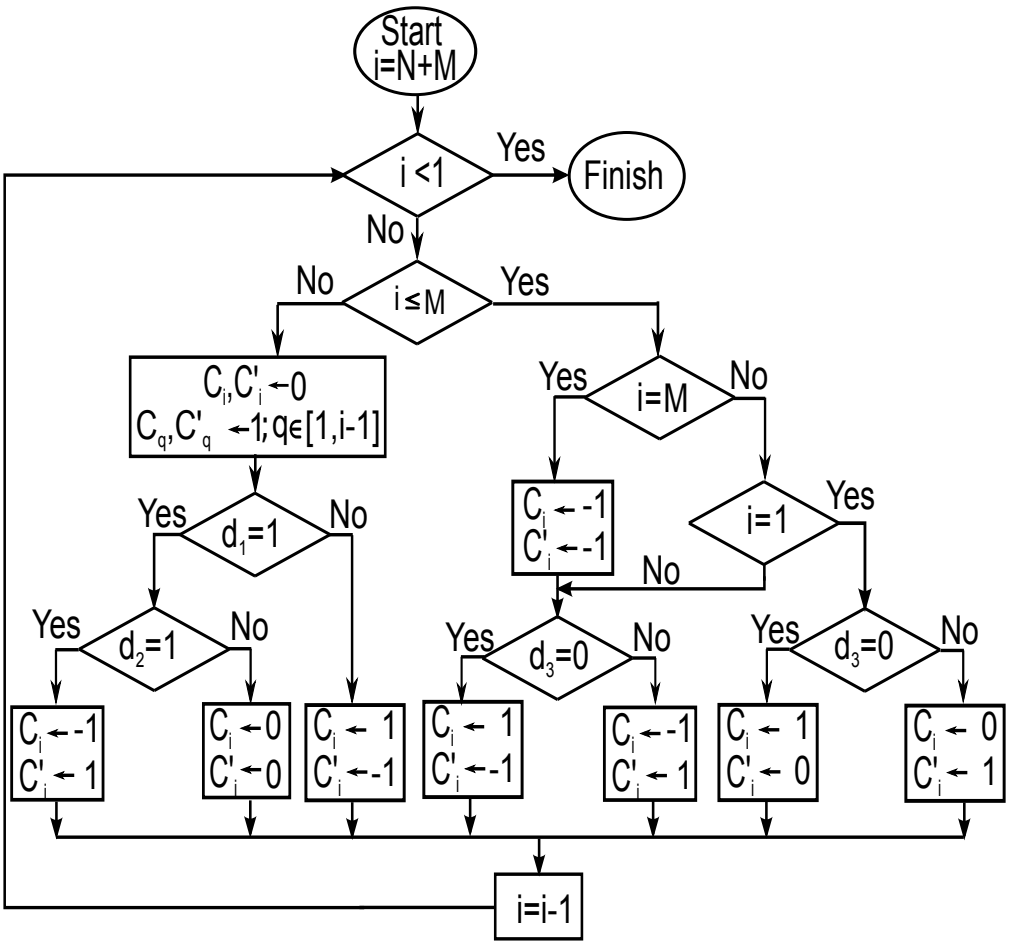


Figure 3.6: Conversion flow diagram of the propsed hybrid SAR ADC.

The design complexity of the hybrid SAR ADC including three ternary bits and one binary bit was estimated and compared with other multi bits/cycle SAR ADCs with close to 6-binary bits resolution in Table 3.2. It can be seen from Table 3.2 that, because of the architecture, the proposed ADC requires fewer DAC arrays and capacitors than the other ADCs. Also, the switching between low and high power comparators in the proposed hybrid ADC helps to achieve less comparator power than [Cao et al. [2009]; Chen et al. [2013]; Thirunakkarasu and Bakkaloglu

[2010]], and [Rahman et al. [2014]]. Thus, the hybrid ADC benefits from the high convergence rate with simpler circuitry compared to other ADCs.

Table 3.2: Comparison of hardware complexity of multi bits/step ADCs.

ADC	SAR Arch	Average comparator /cycle	No. of Array	Total unit cap	Control (Switch)	Mux /extra logic
[Cao '09]	2b/cycle	3	6	378	42	Yes
[Shankar '10]	1.6b/cycle	2	4	324	324	No
[Rahman '14]	1.6b/cycle	2	4	324	72	No
Proposed	hybrid	1.5	2	54	38	No

3.3 Hybrid ADC Characterization

3.3.1 Effect of Comparator Offset

The LSB of a hybrid SAR ADC with N ternary bits and M binary bits is $2V_{ref}/2^{(1.6N+M)}$. During the radix-3 search, the comparator offset should be less than $V_{ref}/2^{1.6N}$ which is $2^{(M-1)}$ times larger than the LSB and though two comparators are used simultaneously, the offset mismatch between the comparators should not affect the linearity as long as it does not cross the over range limit set by redundancy capacitor [Chang et al. [2013]], which is 9 LSB in our design. During the radix-2 search of the hybrid ADC, a single comparator is used and its offset should not affect the overall linearity. In the radix-3 SAR ADC, the linearity is affected by the comparator offset mismatch as two comparators are used simultaneously during all the conversion steps. The variation of comparator offset is modeled by a Gaussian random variable with standard deviation. In Fig.3.7, the SNDR is plotted based on the result of 10000-sample Monte Carlo simulations for a (5+5) bit

hybrid ADC with redundancy. As explained earlier, the hybrid SAR ADC shows consistent SNDR over the whole range of variation while the radix-3 ADC's linearity degrades significantly. Similarly, the input common mode voltage variation of the two different single-ended DACs is equivalent to the comparator offset mismatch and it will not affect the hybrid ADC's performacne as long as the variation is within the over range limit.

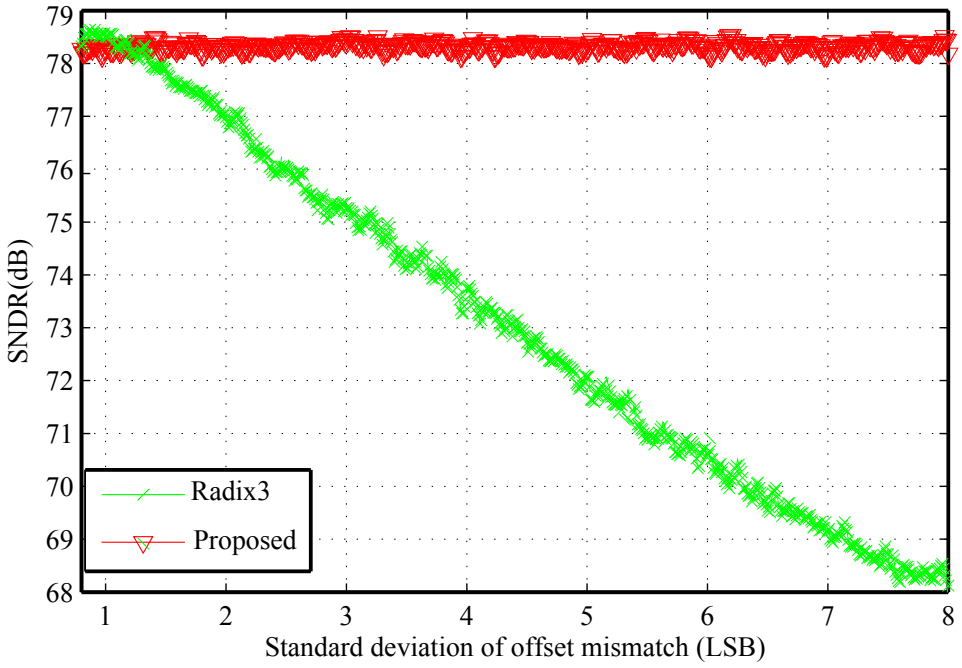


Figure 3.7: Monte-Carlo simulation to compare the effect of comparator offset.

3.3.2 Comparison of Speed

The proposed ADC exploits the conversion speed of the radix-3 search and converges faster than a radix-2 SAR ADC. To achieve an equivalent of K binary bits of resolution, a hybrid ADC with M binary bits takes $(M + \frac{K-M}{1.6})$ cycles

and a radix-3 ADC requires $\frac{K}{1.6}$ cycles. Depending on the value of M, Table 3.3 shows the comparison between number of conversion cycles of hybrid ADCs, T_{hyb} and that of radix-2 ADCs, T_{conv} and that of radix-3 ADCs, T_{rd3}. Depending on the configuration, the proposed ADC can achieve a maximum speed gain of 37.5% over a radix-2 ADC, but can have a worst case speed loss of 25% compared to a radix-3 ADC. Fig.3.8 shows the comparison of total comparison cycles among radix-2, radix-3, and hybrid SAR ADC with $M = 3$. It follows the result in Table 3.3.

Table 3.3: Speed gain of the hybrid ADC over radix-2 and radix-3 SAR ADCs.

Resolution	$(T_{conv}\text{-}T_{hyb})/T_{conv}$ (%)			$(T_{hyb}\text{-}T_{rd3})/T_{rd3}$ (%)		
K (bits)	M=2	M=3	M=4	M=2	M=3	M=4
6	16.7	33	16.7	0	−25	−25
7	28.6	22	14.3	−20	−20	−20
8	25	37.5	12.5	−20	−20	−20
9	22.2	22.2	22.2	−16.2	−16.2	−16.2
10	30	30	20	0	0	−16
11	27.3	27.3	27.3	−14.3	−14	−14
12	33.3	25	25	−12.5	−25	−25

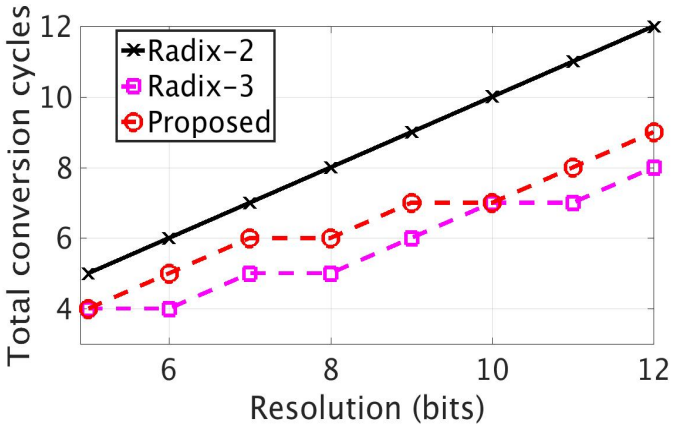


Figure 3.8: Comparison of total conversion cycles.

3.4 Comparison of Power

3.4.1 DAC Energy:

One of the major contributors to the power consumption in ADC is the capacitor DAC. To achieve N binary bits, a radix-2 ADC requires a total of 2×2^N unit capacitors. For the same binary resolution, a radix-3 ADC requires $\frac{N}{1.6}$ ternary bits and a total of $4 \times 3^{\frac{N}{1.6}}$ unit capacitors. Assuming the hybrid ADC contains equivalent ternary and binary bits, it will require a total of $2 \times (2^{\frac{N}{2.6}-1}3^{\frac{N}{2.6}})$ unit capacitors. Fig.3.9 shows the required total capacitor value for radix-2, radix-3 and hybrid SAR ADCs for different number of resolutions. It shows that, to have same resolution, the hybrid SAR ADC requires fewer capacitors than the others.

During a radix-3 conversion, the converging capacitors are first connected to V_{cm}. If the input voltage levels are within the $[-1/3, 1/3]$ region of V_{ref}, then none of the capacitors will be switching and energy will be zero. If input voltage levels are within the $[1/3, 1]$ region of V_{ref}, then one of the capacitor of the DACs

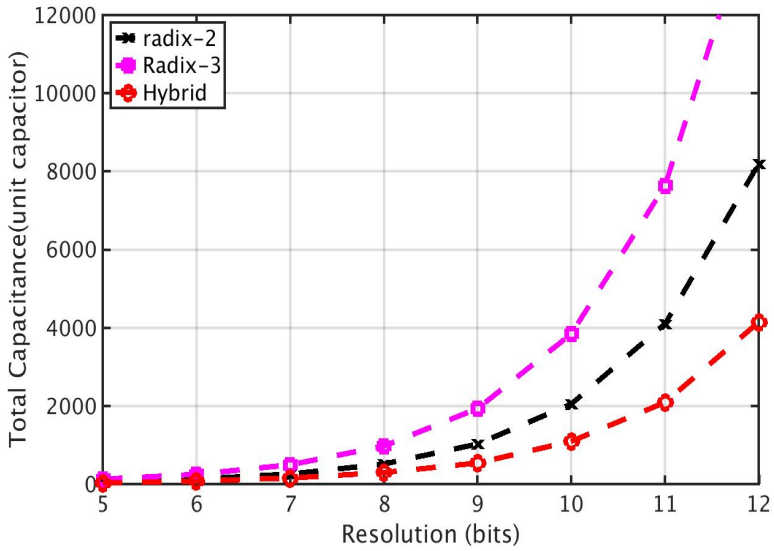


Figure 3.9: Comparison of total number of capacitors.

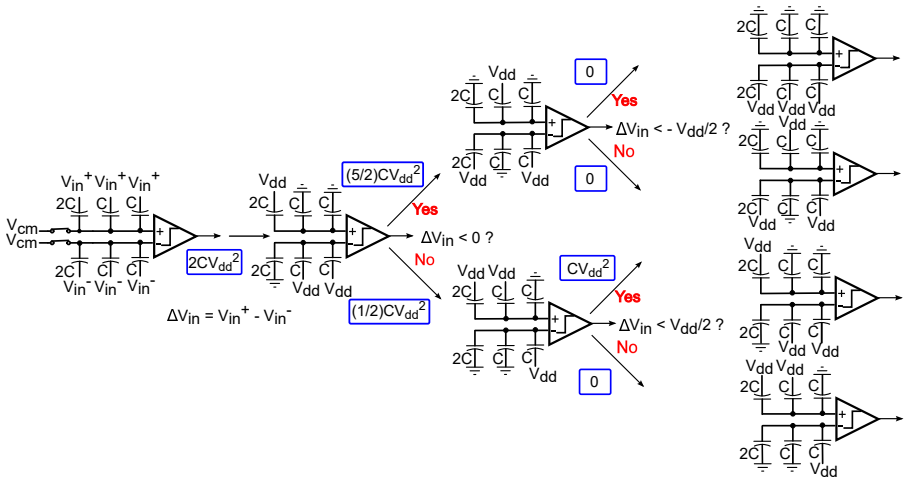
will be switching. If input voltage levels are within the $[-1, 1/3]$ region of V_{ref}, then both capacitors of the DACs will be switching. So, in each conversion, either two capacitors or one capacitor or none will switch depending on the input value. Also, in the radix-2 search, the proposed switching scheme ensures much less switching energy in the first two conversion cycles and only one capacitor is switched in each comparison cycle, which also reduces the energy. The SAR used in the proposed technique adopts the novel low-power switching technique of [Sanyal and Sun [2014]] in which only one-side of the differential DAC array needs to be switched every cycle. The proposed technique is compared with the conventional switching technique in Fig.3.10 with a 2-bit example. Switching the LSB capacitor between $(0, V_{cm})$ instead of $(0, V_{dd})$ allows the proposed technique to generate a zero-mean residue for the 2-bit ADC with only 4C capacitance. If a zero-mean

residue is not required, the proposed technique can give 3-bit resolution with the same 4C capacitance [Sanyal and Sun [2014]]. Thus, the proposed switching technique achieves a 4X capacitance reduction compared to the conventional technique and this holds true for an ADC with any resolution. Bottom-plate switching is used to ensure linearity of the ADC.

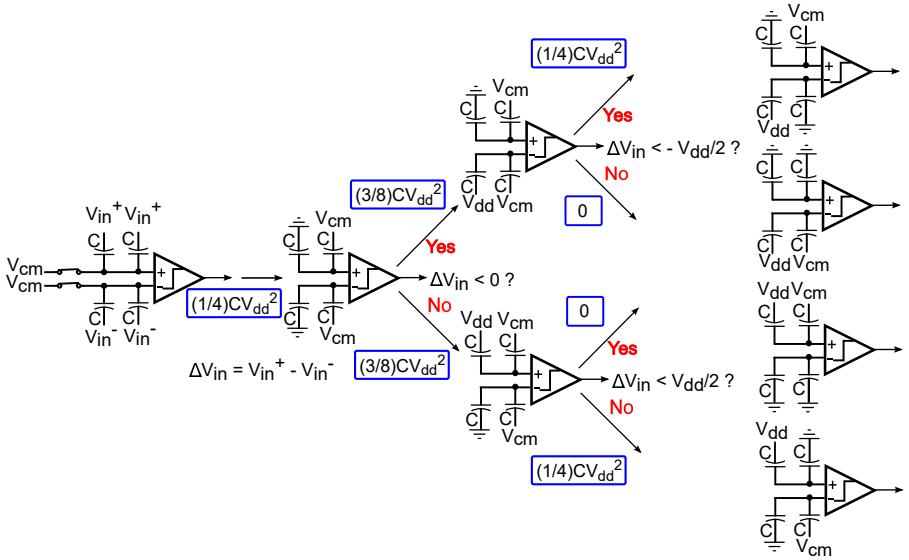
The hybrid SAR ADC benefits from the radix-3 and radix-2 switching approach and also from the capacitor values. Fig.3.11 shows a comparison of E_{ref} for the different techniques for a 10-bit SAR ADC. As can be seen, the proposed scheme has a significantly lower E_{ref} than the other techniques in all the conversion cycles.

3.4.2 Comparator Power:

The LSB of an N_1+M-bit hybrid SAR ADC is $2V_{ref}/2^{1.6N_1+M}$. During the radix-3 search, the comparator offset should be less than $V_{ref}/2^{1.6N_1}$ which is 2^{M-1} times larger than the LSB. So, during radix-3 search, we use a low power high noise comparator. Since, the LSB value during the radix-3 search is much higher, we can use the minimum size for the input differential pairs of comparators which will give a high input referred offset. As a result, the comparator switching power during radix-3 search operation is reduced. But during radix-2 search, the low power comparators are switched off and we use high-power, but low noise comparator. This way, we can save comparator power and the total comparator power would be comparable to standard radix-2 ADC. The radix-3 ADC has to use two high power low noise comparators during all the cycles for accuracy purposes



(a)



(b)

Figure 3.10: Switching technique for 2-bit (a) conventional SAR, and (b) proposed SAR ADC.

and comparator power becomes higher than the radix-2 and the hybrid SAR ADC.

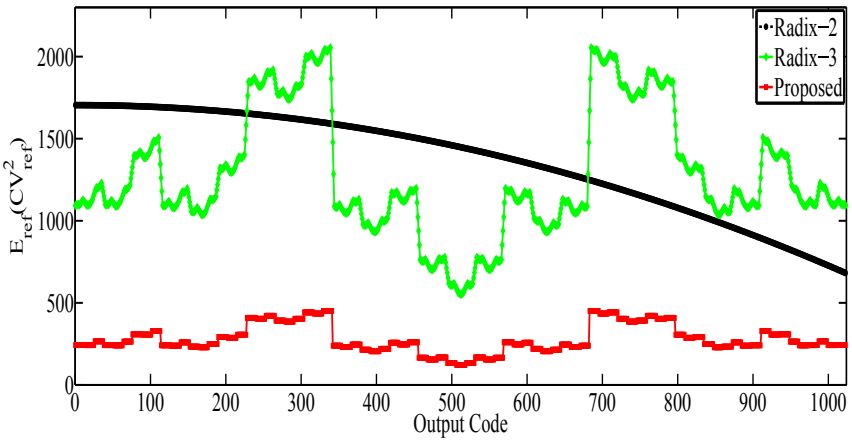


Figure 3.11: Comparison of DAC energy.

3.4.3 SAR Logic Power:

The major contributors to logic power are flip flops and logic circuits that connect the capacitors to correct voltage levels. For N binary bit resolution, a radix-2 ADC requires $(N+1)$ DFFs to latch the data for the capacitor DAC, where a radix-3 ADC requires $(\frac{2N}{1.6}+1)$. Similarly, required control circuits (MOSFETS) for capacitor DACs for the radix-2 ADC is $\sim (2N+2)$, and for the radix-3 ADC, it is $\sim (\frac{6(N+1)}{1.6})$. Fig.3.12 shows the comparison of total DFFs and control circuits.

Considering above facts, it shows that hybrid ADC offers lower DAC energy than the conventional radix-2 ADC, equivalent comparator power and more power in logic circuits than the radix-2 ADC. Also, it offers lower power than the radix-3 ADC as discussed above. Considering the speed gain over the radix-2 ADC and the accuracy gain over the radix-3 ADC, hybrid ADC proves itself to be a good candidate for low power and high speed data conversion.

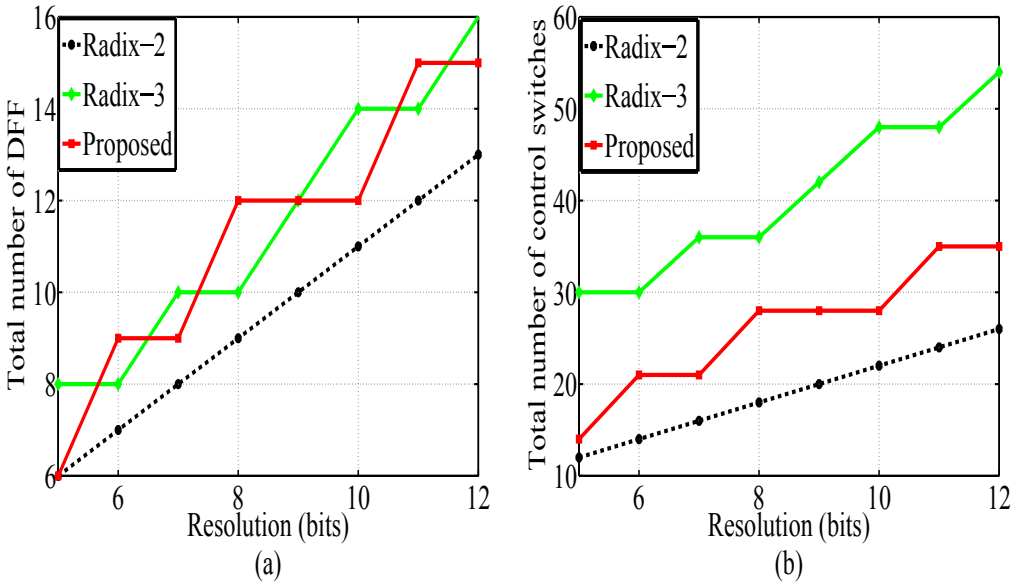


Figure 3.12: Comparison of (a) total number of DFFs (b) total number of control circuits.

3.5 Capacitor Mismatch Calibration

Fig.3.13 is a simplified version of $(N + M)$-bit hybrid SAR ADC. Due to process variation, it has been assumed that each capacitor has varied by a proportion of ϵ [Lee et al. [1984]]. The capacitor values in terms of the unit capacitor of a radix-2 DAC, C_u are as following:

$$C_n = \begin{cases} 2 \cdot 3^{n-M-1} C_u(1+\epsilon_n) & \text{if M+1}\leq\text{n}\leq\text{N+M} \\ \frac{2^{n-2}}{2^{M-1}} C_u(1+\epsilon_n) & \text{if 1<n}\leq\text{M} \\ \frac{1}{2^{M-1}} C_u(1+\epsilon_1) & \text{if } n = 1 \end{cases} \tag{3.4}$$

A redundant capacitor C_r is required for calibration purposes. If number of LSB capacitors used for calibration is Q, then C_r can be defined in terms of the unit capacitor of $\text{DAC}_{1,2}$, C_u as:

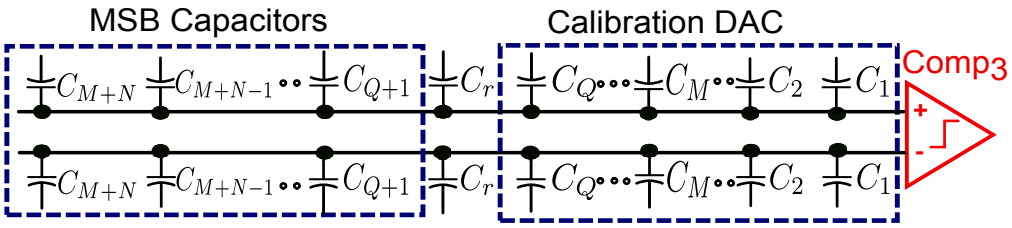


Figure 3.13: Simplified DAC of the hybrid SAR ADC.

$$C_r = 3^{Q-M-1}C_u(1+\epsilon_r)$$

For example: Let us assume that we have a (4+3) bit hybrid SAR ADC. So, $N = 4$, $M = 3$.

So, the capacitor values are, 216, 72, 24, 8, 2, 1, 1.

Unit capacitor of $\text{DAC}_{1,2}$, $C_u = 1 + 1 + 2 = 4$.

We assume that 6 capacitors will be used for calibration including the redundancy capacitor. So, $Q = 6$.

So, the redundancy value is, $C_r = 3^{Q-M-1} \times C_u = 3^{6-3-1} \times 4 = 36$.

For ideal case, total capacitors of $\text{DAC}_{1,2}$, $C_{total} = 2^{M-1}(3^N + 3^{Q-M-1})$.

So, the unit capacitor of $\text{DAC}_{1,2}$, C_u can be redefined as:

$$C_u = C_u \times \frac{C_{total}}{2^{M-1}(3^N + 3^{Q-M-1})} \tag{3.5}$$

Taking the capacitor mismatch into consideration,

$$C_u = \frac{C_u((2^M \sum_{i=M+1}^{M+N} 3^{i-M-1} + \sum_{i=1}^{M} 2^{i-1})(1+\epsilon_i) + (1+\epsilon_1) + 3^{Q-M-1}2^{M-1}(1+\epsilon_r))}{2^{M-1}(3^N + 3^{Q-M-1})} \tag{3.6}$$

Defining $3^{Q-M-1}2^{M-1}$ as A, $2^M \sum_{i=M+1}^{M+N} 3^{i-M-1}$ as X_i, $\sum_{i=1}^{M} 2^{i-1}$ as Y_i:

$$C_u = \frac{C_u((X_i + Y_i)(1+\epsilon_i) + (1+\epsilon_1) + A(1+\epsilon_r))}{2^{M-1}(3^N + 3^{Q-M-1})} \tag{3.7}$$

$$\Rightarrow C_u = \frac{C_u(X_i + Y_i + 1 + A)}{2^{M-1}(3^N + 3^{Q-M-1})} + \frac{C_u((X_i + Y_i)\epsilon_i + \epsilon_1 + A\epsilon_r)}{2^{M-1}(3^N + 3^{Q-M-1})} \tag{3.8}$$

$$\Rightarrow C_u = C_u + \frac{C_u((X_i + Y_i)\epsilon_i + \epsilon_1 + A\epsilon_r)}{2^{M-1}(3^N + 3^{Q-M-1})} \tag{3.9}$$

As C_u can not be 0, it is implied from (3.9):

$$(X_i + Y_i)\epsilon_i + \epsilon_1 + A\epsilon_r = 0 \tag{3.10}$$

The output voltage, V_o can be found in terms of the digital output code D_i, where $i \in [1, M+N]$ and the code for redundancy capacitor, D_r:

$$V_o = \frac{\sum_{i=1}^{N+M} C_i D_i + C_r D_r}{C_{total}} \tag{3.11}$$

$$V_o = \frac{(X_i + Y_i)(1+\epsilon_i)D_i + A(1+\epsilon_r)D_r + (1+\epsilon_1)D_1}{2^{M-1}(3^N + 3^{Q-M-1})} \tag{3.12}$$

if there is no mismatch, i.e $\epsilon_i = \epsilon_r = 0$, then the ideal output:

$$V_{ideal} = \frac{(X_i + Y_i)D_i + AD_r + D_1}{2^{M-1}(3^N + 3^{Q-M-1})} \tag{3.13}$$

Defining the error voltage for the n-th capacitor as $V_{\epsilon n}$ and the total error voltage as V_{error}:

$$V_{\epsilon n} = \begin{cases} \frac{2 \cdot 3^{i-M-1}\epsilon_n}{(3^N + 3^{Q-M-1})} & \text{if } M+1 \le n \le N+M \\ \frac{2^{i-M}\epsilon_n}{(3^N + 3^{Q-M-1})} & \text{if } 1 < n \le M \\ \frac{2^{1-M}\epsilon_n}{(3^N + 3^{Q-M-1})} & \text{if } n = 1 \\ \frac{3^{Q-M-1}\epsilon_n}{(3^N + 3^{Q-M-1})} & \text{if } n = r \end{cases} \tag{3.14}$$

$$V_{error} = V_o - V_{ideal} = \sum_{i=1}^{N+M} V_{\epsilon i} D_i + V_{\epsilon r} D_r \tag{3.15}$$

In the current ADC architecture, LSB capacitors C_i, $i \in [1, Q]$ do not require calibration as their mismatch error is negligible [Lee et al. [1984]]. So, calibration is performed on MSB capacitors C_i, $i \in [Q+1, M+N]$. Calibration is started by finding the mismatch of the $M+N$-th MSB capacitor. '1' is sampled across C_{M+N} and rest of the capacitors (including top pates) are connected to '0'. Then '1' is sampled on the bottom plate of all the capacitors except C_{M+N} and C_i, $i \in [1, Q]$ which will be connected to '-1'. So, the residual charge at the top plate of the capacitors is:

$$Chg_{M+N} = 2 \cdot C_u (3^{N-1}\epsilon_N - \sum_{i=Q+1}^{N+M-1} 3^{i-M-1}\epsilon_i - A\epsilon_r) \tag{3.16}$$

From (3.14) and (3.16), the residual voltage is:

$$V_{xM+N} = \frac{Chg_{M+N}}{C_{total}} = \frac{3}{2} V_{\epsilon_{M+N}} \tag{3.17}$$

Similarly, the error voltage $V_{\epsilon n}$, $n \in [Q+1, N+M-1]$ is:

$$V_{\epsilon n} = \frac{2}{3}(V_{xn} - \sum_{i=n+1}^{M+N} V_{\epsilon i}) \tag{3.18}$$

After quantizing the error, digitized error voltages DV_{ϵ_q} and quantized residue voltage, DV_{xq} are:

$$DV_{\epsilon q} = \begin{cases} \frac{2}{3} DV_{xq} & \text{if } q = N+M \\ \frac{2}{3}(DV_{xq} - \sum_{i=Q+1}^{N+M} DV_{\epsilon i}) & \text{if } N+M > q \geq Q+1 \end{cases} \tag{3.19}$$

If the i-th bit is assigned as 1, 0 or -1, then the corresponding error voltage $DV_{\epsilon i}$ will be $DV_{\epsilon i}$, $(1/2)DV_{\epsilon i}$ or 0 respectively. C_i, $i \in [1, Q]$ can be used for digitizing the error terms. During normal conversion cycles, the calibration logic is de-activated and the converter works in the same way as the proposed hybrid SAR ADC. Finally the error correction voltages are added based on the DAC digital output codes of the first $N + M - Q$ capacitors.

3.6 Key Circuit Building Blocks

3.6.1 Choice of Architecture

Table 3.4: Selection of hybrid SAR ADC architecture.

# Radix-3	# Radix-2	i(Total) (uA)	Expected ENOB	# Cycles	Fs (MHz)	FOM (fJ/Conv)
2	7	1396	9.1	10	200	13.99
3	6	1397	9.5	10	200	10.61
4	4	1615	9.3	9	222	12.68
5	3	1630	9.4	9	222	11.94

In the hybrid SAR ADC, it is very imperative to decide on the combination of number of radix-3 bits and number of radix-2 bits. We need to consider all the possible combinations and the trade-offs among power, speed and performance. Increasing the number of radix-3 bits will help achieve higher convergence speed, but we also need to consider the dynamic comparator power, DAC power and overall ADC power depending on the architecture. Also, the comparator offset mismatch is a concern for the radix-3 ADC as we have to use two comparators in each radix-3 conversion cycle. To begin with, a 2-bit-radix-3 + 7-bit-radix-2 based

hybrid SAR ADC was designed in a 40nm CMOS process. We achieved the target performance from it and then estimated the performance of the other possible combinations based on simulated values as shown in Table 3.4.

From the above table, it is clear that the 3-radix-3-bit+6-radix-2-bit combination offers second highest convergence speed, lowest power and lowest FOM. So, we picked this combination for our proposed hybrid SAR ADC.

3.6.2 SAR Logic and Control

In this subsection, we discuss the logic design of the hybrid SAR ADC. We are going to design a 9.5 bit hybrid SAR ADC including a 3-bit radix-3 SAR ADC and a 6-bit radix-2 SAR ADC. Fig.3.14 shows the top level schematic of the proposed hybrid ADC. Two distinct colors have been used to distinguish between radix-3 and radix-2 circuits. The ADC consists of two capacitor arrays. As discussed before, for the radix-3 search, we will be using a single ended DAC array to reduce the DAC power. The DACs shown in Fig.3.14 are used as single ended during the radix-3 search and act as a differential DAC during the radix-2 search. The capacitor arrays are driven by logic circuits which include buffers and flipflops. The data are driven to the flops by the comparators.

The ADC uses three comparators. Two of them, are high power, high speed and low resolution for radix-3 convergence. For the radix-2 converter, we have used a high speed and high resolution comparator. The comparators generate the clocks for the data-flops. As the radix-3 comparators will be used as single ended manner, the negative terminal of $Comp_1$ and positive terminal of $Comp_2$ are connected

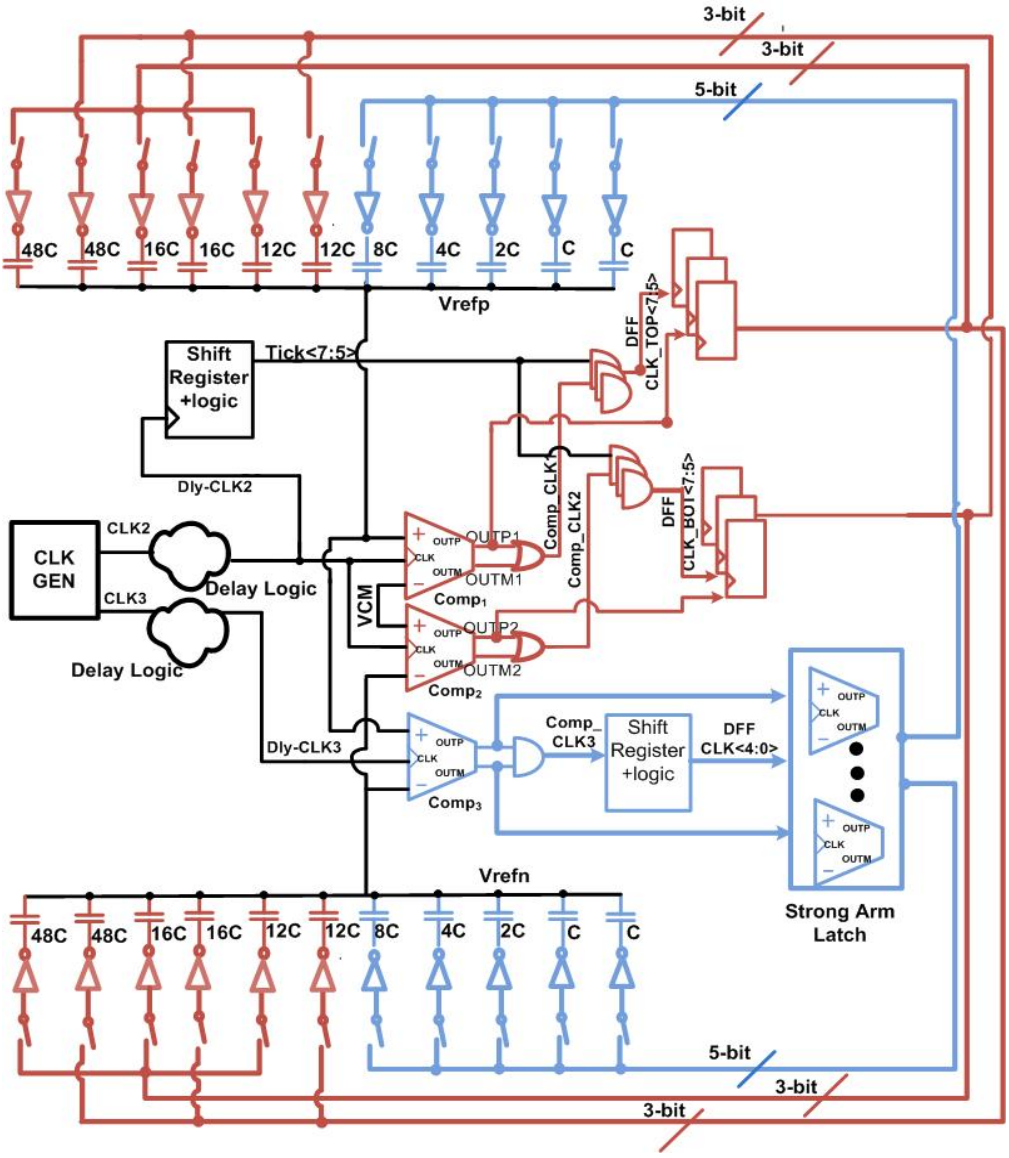


Figure 3.14: Top level circuit diagram of the proposed hybrid SAR ADC.

to VCM (Fig.3.14). All the digital logic for radix-3 and radix-2 convergence are synchronous. The logic and other circuits will be discussed in the following sub-sections.

3.6.3 Clock Generation Logic

In this design, we will have 1 clock cycle CLKS for sampling, and 9 clock cycles for the comparison and convergence of the SAR ADC. We don't need an extra clock cycle to send the data to the output PAD. Fig.3.15 shows the timing diagram for the clock generation logic.

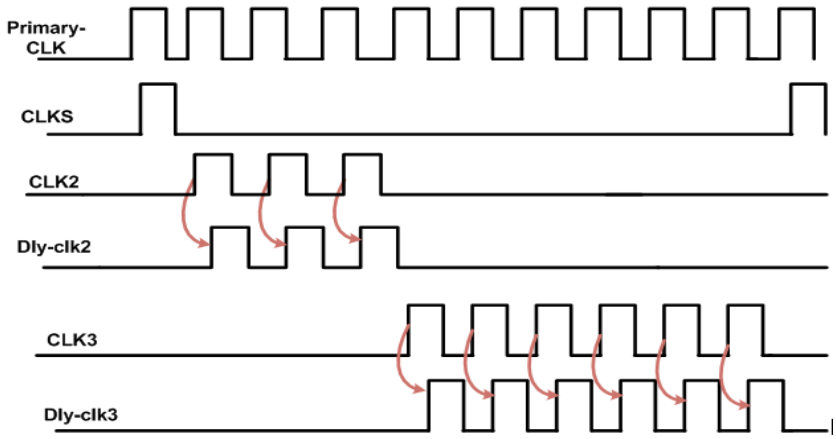


Figure 3.15: Timing diagram of the clock generation.

Primary-CLK is the external clock input. It goes through a 4-bit counter and generates the radix-3 comparator clock "CLK2" and the radix-2 comparator clock "CLK3". Both CLK2 and CLK3 go through a delay cell to generate Dly-clk2 and Dly-clk3, respectively for the radix-3 and the radix-2 SAR logics. It needs to be noted that Dly-clk2 and Dly-clk3 are completely non-overlapping and Dly-clk2 does not toggle any more when Dly-clk3 starts toggling to avoid unnecessary kick-back noise from the radix-3 comparators during the radix-2 search and also to reduce the radix-3 comparators' power.

Fig.3.16 shows conventional circuits for clock generation for the data flops to latch the data of the radix-3 comparison. Sampling clock CLKS sets/resets the flops of the shift register. The clocks to the flops of the shift register are generated by outputs of the radix-3 comparators.

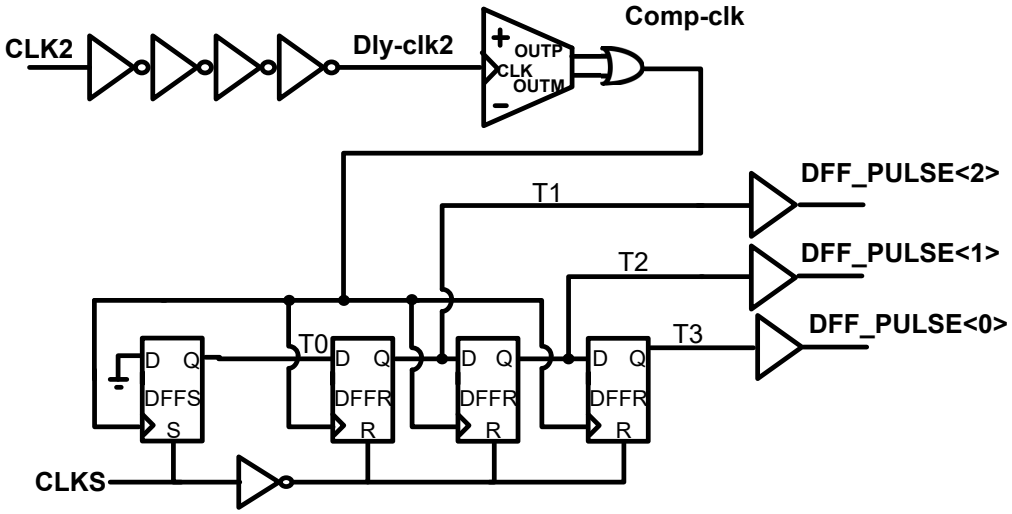


Figure 3.16: Conventional clock generation circuit for the radix-3 data flops.

Fig.3.17 shows the timing diagram for the conventional clock generation for the data flops to latch data for the radix-3 comparisons. While CLKS is high, T0 is high and T1, T2, T3 become low. Dly-clk2 is generated from CLK2 signals after a few buffer delays shown on Fig.3.17. Dly-clk2 acts as a comparator clock and in each cycle, one of the comparator outputs will be high which generates the signal Comp-clk. Comp-clk acts as the clock to the flops of the shift registers and generates DFF_PULSE$< 2 : 0 >$. So, the delay from comparator output to DFF_PULSE is:

OR-gate-delay+ FLOP clk-to-q delay + Buffer-delay.

Fig.3.18 shows improved and faster circuits for clock generation for the data

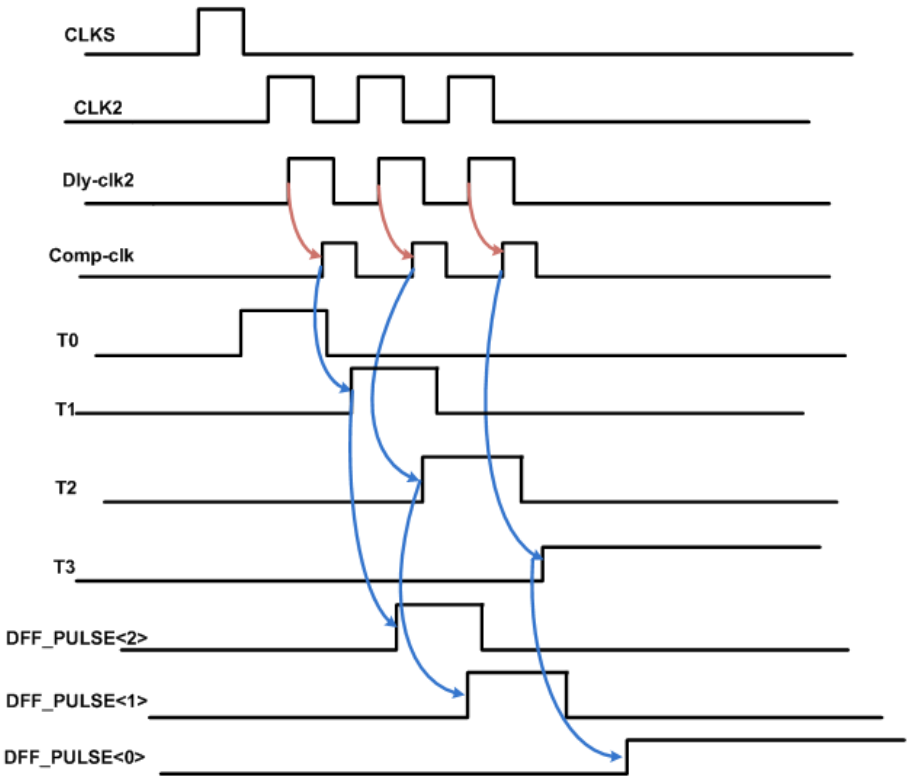


Figure 3.17: Conventional clock generation timing for the radix-3 data flops.

flops to latch data of radix-3 comparison. The sampling clock $CLKS$ sets/resets the flops same as original circuit. The clock to the flops of shift register is the same clock as the comparator clock. So, the overall comparator output data to flop output delay gets reduced.

Fig.3.19 shows the improved timing diagram for the control signals of proposed SAR ADC. While CLKS is high, T0 is high and T1, T2, T3 becomes low. Dly-clk2 is generated from CLK2 signals after few buffer delays as shown on Fig.3.19. Dly-clk2 acts as the comparator clock and in each cycle, one of the com-

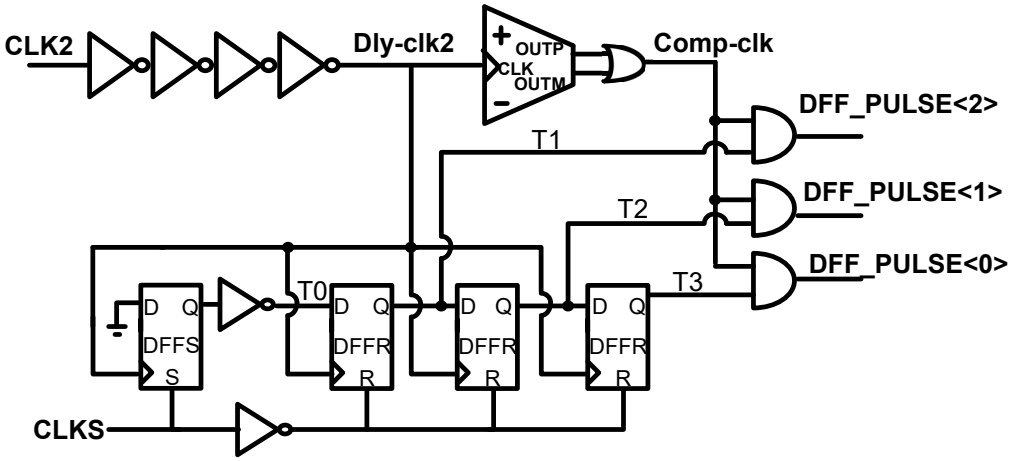


Figure 3.18: Improved clock generation circuit for the radix-3 data flops.

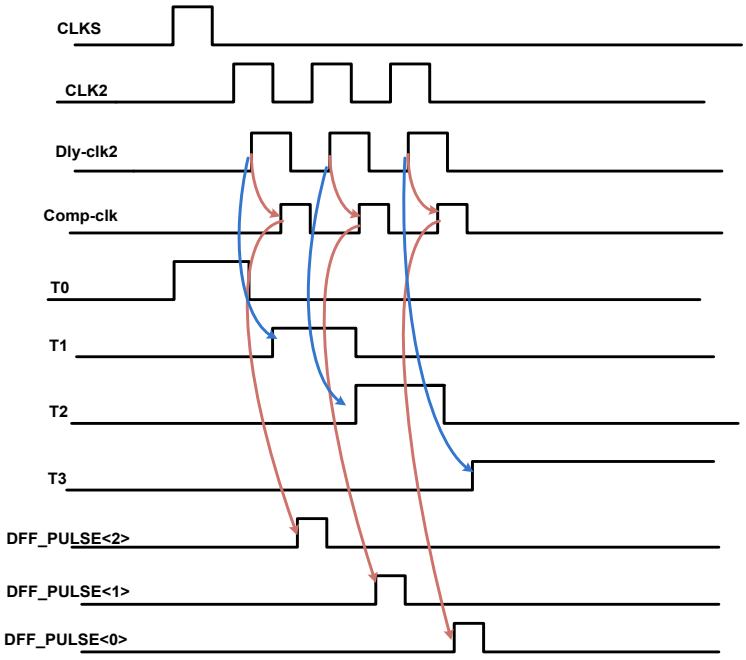


Figure 3.19: Improved clock generation timing for the radix-3 data flops.

parator outputs will be high which generates the signal Comp-clk. Also, Dly-clk2 acts as the clock to the shift register flops. It needs to be noted that T1, T2, T3 become high for the whole cycle of Dly-clk2 and Comp-clk remains high only for the partial cycle of Dly-clk2. As T1-T3 are ANDed with Comp-clk to generate DFF_PULSE$< 2 : 0 >$, it is guaranteed that there will be no glitch in the pulse signals. So, the delay from comparator output to DFF_PULSE is:

OR-gate-delay+AND-gate-delay.

It needs to be noted that, we save the FLOP-clock-to-q dealy which is equivalent to 4-single gate delays (INVERTER delay). Thus, the overall comparator output data to flop output delay is improved. Fig.3.20 shows that the modified scheme is 100ps faster than conventional timing generation scheme.

3.6.4 Sample and Hold Circuit

The input sampling switches are bootstrapped switches with the circuit shown in Fig.3.21. Bootstrapped switches are employed in the sampling circuit in order to achieve both smaller on-resistance and minimal signal-dependent sampling distortion [Siragusa and Galton [2004]]. It is simple and does not require two complementary clock phases [Jiang et al. [2012]]. Fig.3.22 shows the timing diagram of the proposed sample and hold circuit. When the sampling clock $CLKSB$ is high, the switch M_4 is shorted to ground and the capacitor C is charged to near the supply voltage. When $CLKSB$ is low, the large voltage difference across the capacitor will be added to the input signal V_{inp} and then applied to the gate of the pass switch M_{sw}, making the gate-source voltage of the NMOS close to that high voltage

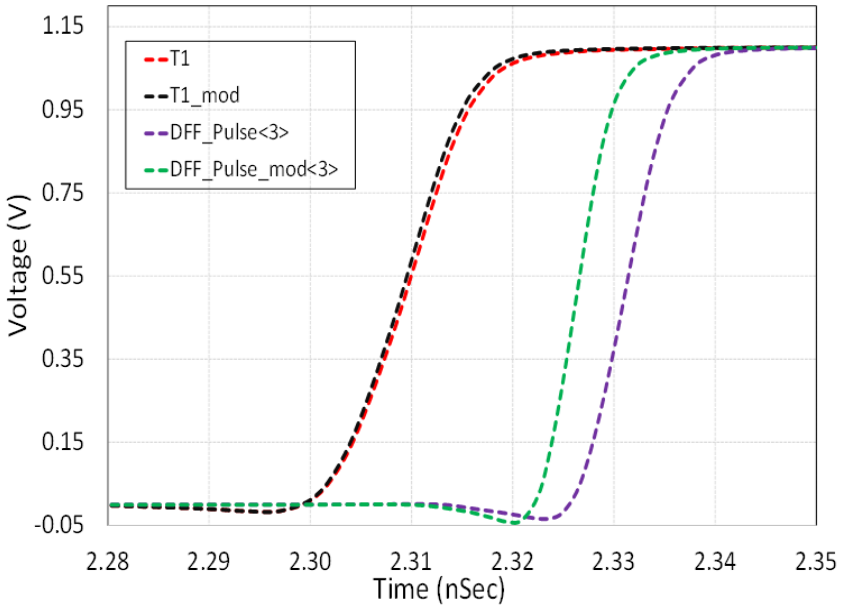


Figure 3.20: Comparison of timing between proposed and conventional scheme.

constantly. In order to reduce the on-resistance of the bootstrapped switch such that the track and hold circuit can meet the hard timing requirement, the external supply voltage connection is thoroughly considered during the layout.

Design considerations for bootstrapped switch are as follows: 10-bit linearity with 200 MHz sampling frequency allows M_{sw} to have $\sim 60\Omega$ on-resistance. Fig.3.23 shows the simulated on-resistance of the sampling switch M_{sw}. The gate of M_5 is controlled by V_G as V_X can be greater than VDD. For the same reason, bodies of M_6, M_5 are connected to V_X. The gate of M_3 is controlled by V_G as V_{inp} can be equal to VDD. M_2 is added to reduce the breakdown stress on M_1 when V_G is

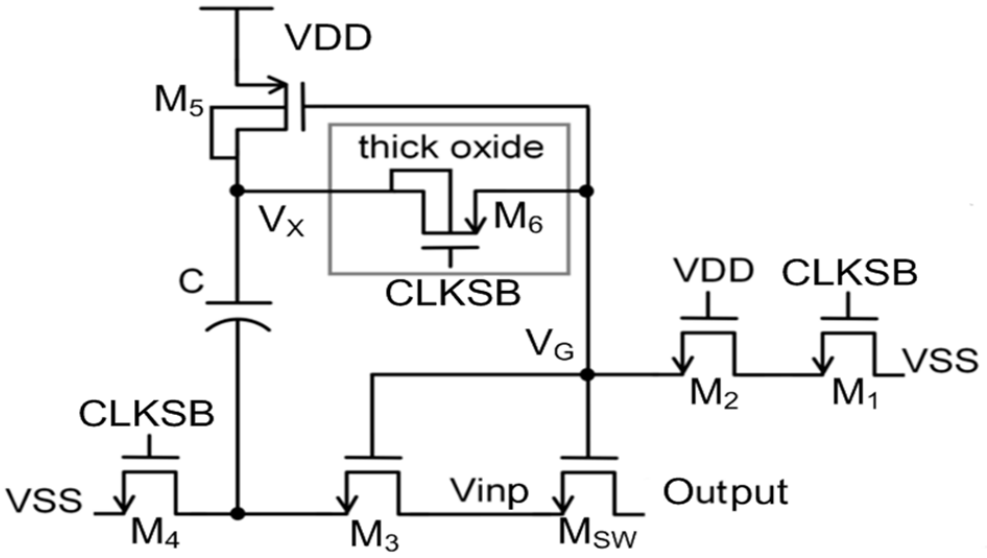


Figure 3.21: Schematic of bootstrapped sampling switch.

greater than VDD. M_6 is chosen to be a thick oxide device to reduce the breakdown stress when the drain-gate voltage is greater than VDD. Fig.3.24 shows 200-point monte-carlo simulation of the bootstrapped switch. The switch has SNDR with a mean of 71.69 dB and a sigma of 2.4 dB. Fig.3.25 shows a 1024-point FFT plot of the bootstrapped switch output at sampling frequency of 200 MHz which has 71.6 dB SNDR and is completely in accordance with the design requirement.

3.6.5 Capacitor Switching Circuit

During the radix-3 search, MSB capacitors need to be connected to V_{cm} and the rest of the capacitors should be connected to VDD. The traditional way to switch the capacitors is to use transmission gates as shown in Fig.3.26 as logic gates (i.e NAND or INVERTER) can only switch between VDD and GND. Also, in our

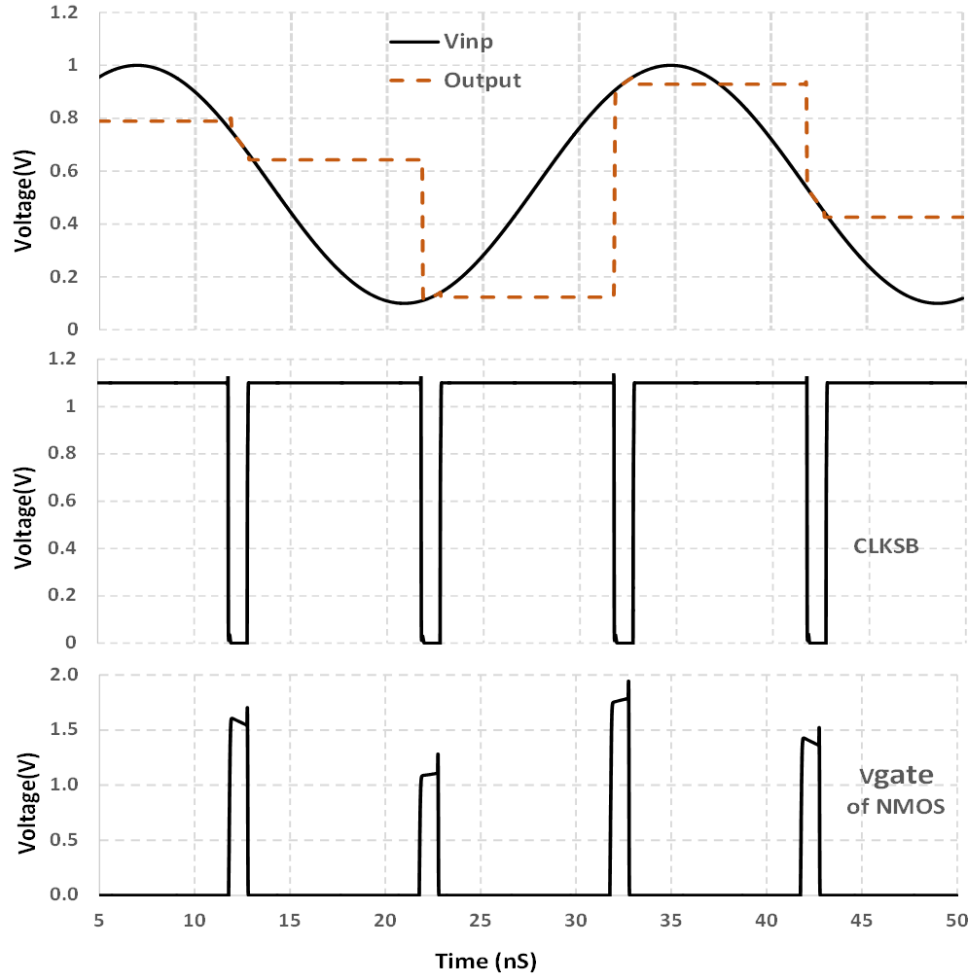


Figure 3.22: Timing diagram of bootstrapped sampling switch.

chip, V_{cm} is an external supply voltage and it accumulates supply noise. To avoid that noise, we divide the radix-3 capacitors into two equal segments. For example, in our 10-bit DAC, capacitor values are $C, C, 2C, 4C, 8C, 24C, 32C$ and $96C$.

Out of these capacitors, $24C, 32C, 96C$ are radix-3 capacitors. So, we divide them as $12C, 12C, 16C, 16C, 48C, 48C$ and these 6 capacitors represent 3-

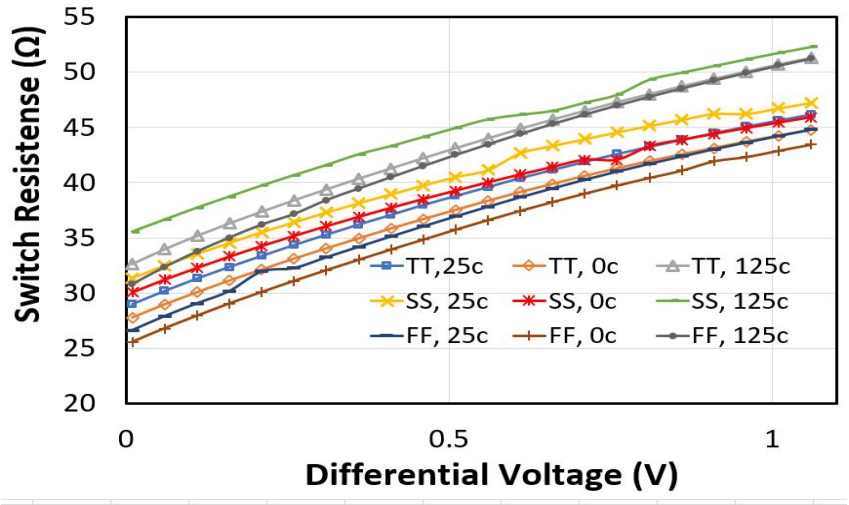


Figure 3.23: Simulated on-resistance of M_{sw}.

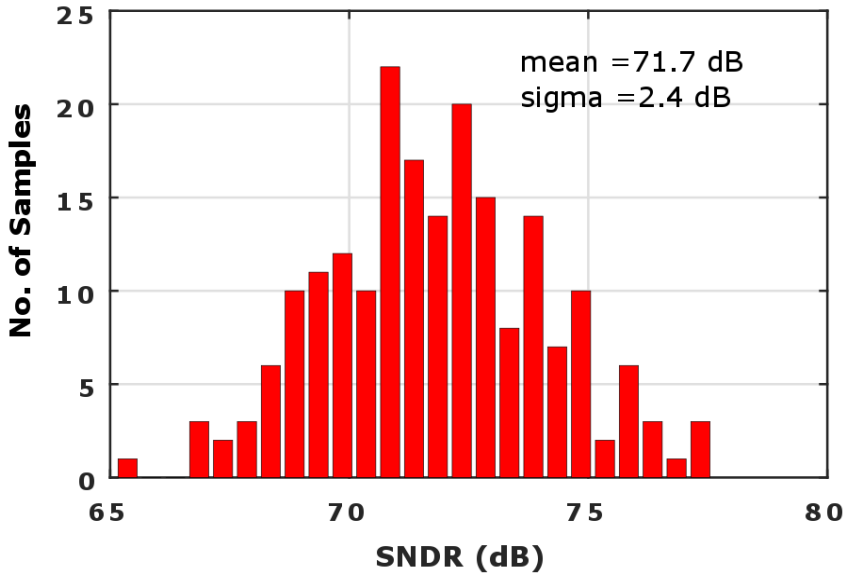


Figure 3.24: 200-point monte-carlo simulation of the bootstrapped switch frequency response.

radix-3 bit. So, when any radix-3 bit needs to be connected to V_{cm}, one of the two equally segmented capacitors will be connected to VDD and another one will be

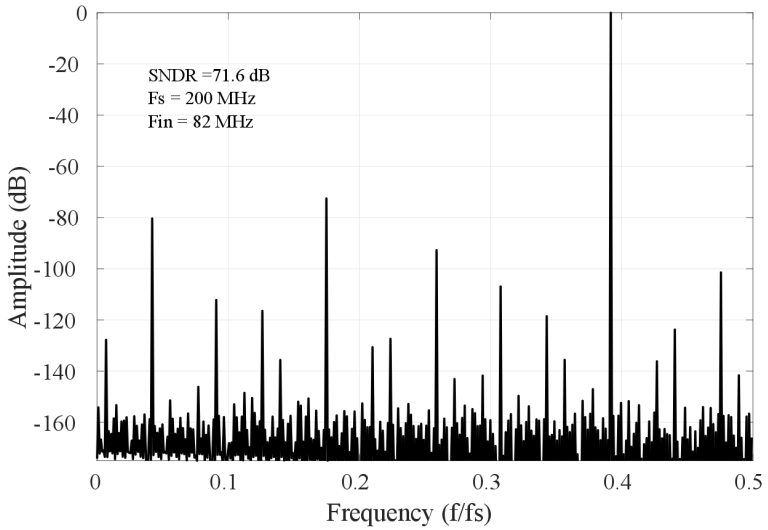


Figure 3.25: 1024-point FFT plot of the bootstrapped switch output.

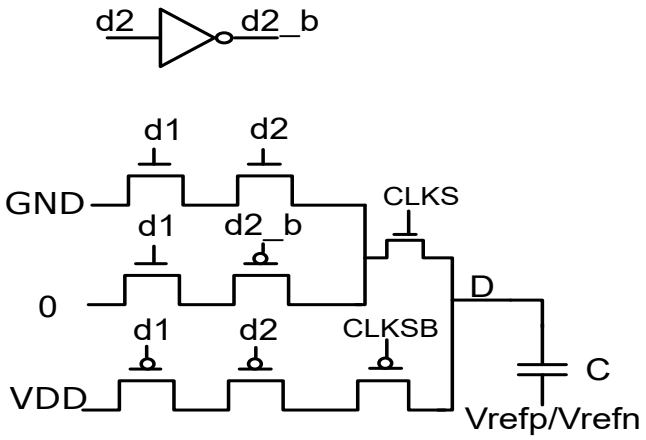


Figure 3.26: Capacitor switching with transmission gate.

connected to GND. As a result, we do not need to use transmission gates as shown on Fig.3.26. Transmission gates are slower because of output loading and series MOSFETs and capacitors take longer time to settle. Fig.3.27 shows the switching circuit with equally divided capacitors. This switch acts as inverters as CLKS and

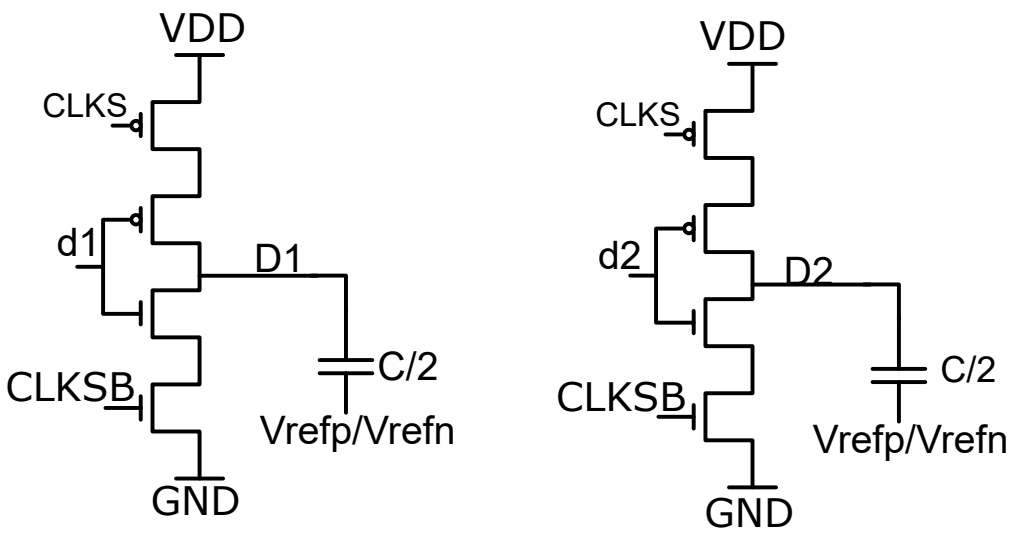


Figure 3.27: Capacitor switching with improved logic inverters.

CLKSB will be at VDD and GND during conversion and the capacitors will settle to required voltage level much faster than transmission gates.

Table 3.5: Comparison of switching scheme.

	Conventional	Proposed
D to Q (ps)	70	40
Power (uW)	42.3	38.5
No of Gates	10	8
No. Power Supply	3	2

Fig.3.28 shows the timing diagram of the proposed and conventional capacitor driver circuits. Table 3.5 shows the performance comparison. The proposed switching circuit consumes 10% less power than the conventional one and is 30pS (43%) faster than the conventional switch.

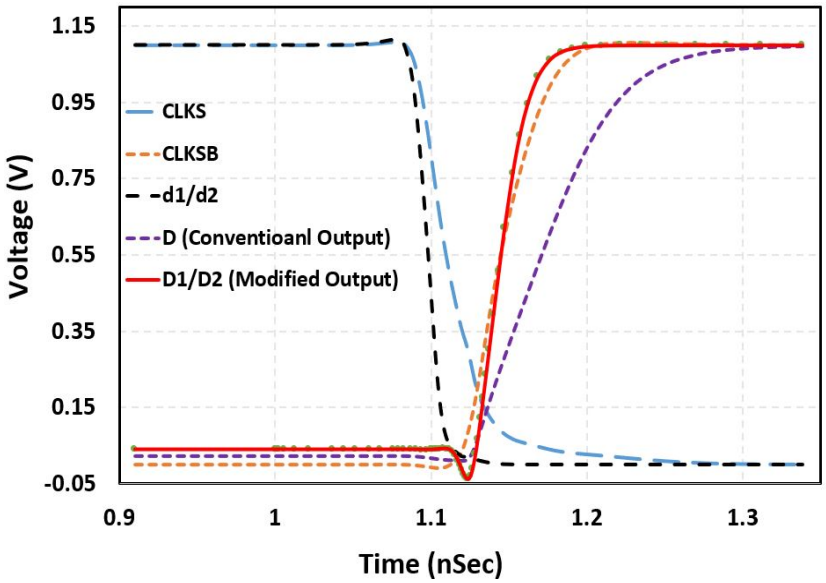


Figure 3.28: Timing diagram of the capacitor driver circuits.

3.6.6 Capacitor Array

The capacitive DAC is designed using metal-oxide-metal (MOM) capacitors. Even though the MOM capacitors have more parasitic capacitance and worse matching compared to metal-insulator-metal (MIM) capacitors, they are compatible with any standard digital process without any specialized process options. The layout of the capacitive array is shown in Fig.3.29.

Common centroid practice is used for top three MSB bits. Even though the calibration algorithm can be used to remove the mismatch due to manufacturing variation, it is still a good practice to try to minimize the variation as much as possible. As discussed in the previous section, although calibration can remove mismatch, larger mismatch between capacitors requires more redundancy. Since the amount of redundancy is pre-configured in the design and cannot be changed after

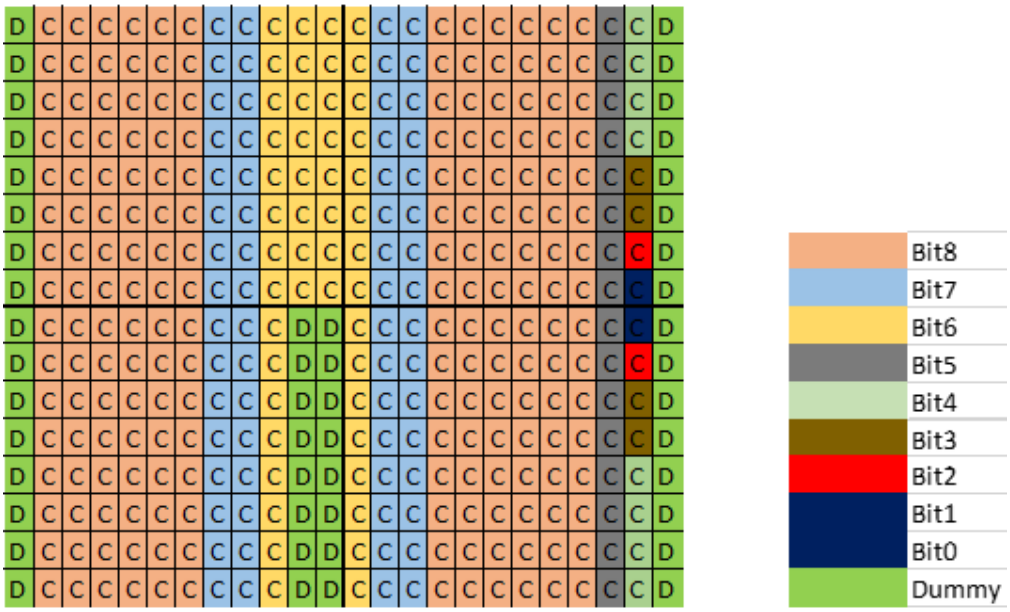


Figure 3.29: Placement of capacitor array.

the chip is fabricated, if too much variation occurs after fabrication exceeding the capability of the redundancy, calibration may not able to completely correct the mismatch. In our 10-bit DAC, the capacitor values are $2C, 2C, 4C, 8C, 16C, 48C, 64C$ and $192C$, where C is the unit capacitor and our design has a value of $1.86fF$ for the unit capacitor. So, we have 16 capacitors in each column and the MSB bit requires 12 columns in common centroid form. Similarly, the MSB-1 bit requires four columns in common centroid form. The MSB-2 bit is a redundancy bit and due its unique value, we used four columns in common centroid form with dummy capacitors in them. The rest of the bits are placed on the right hand side to improve the routing.

Table 3.6 shows the comparison of layout extracted capacitor values with

Table 3.6: Comparison of layout extracted and ideal capacitor values.

Bit	Extracted Cap (fF)	Ideal Cap (fF)	Error (%)	Error (LSB)
Bit0	1.8984	1.8984	0.0	0.0
Bit1	1.8937	1.8984	−0.2	−0.002
Bit2	3.8152	3.7968	0.5	0.010
Bit3	7.58	7.5936	−0.2	−0.006
Bit4	14.99	15.18	−1.3	−0.104
Bit5	30.36	30.374	0.0	−0.008
Bit6	45.48	45.56	−0.2	−0.039
Bit6a	45.49	45.56	−0.1	−0.034
Bit7	60.746	60.748	0	−0.001
Bit7a	60.766	60.748	0.0	0.009
Bit8	182.288	182.246	0.0	0.022
Bit8a	182.264	182.246	0.0	0.009

ideal values. It shows the variation of capacitor value is well controlled and much smaller than $1/2$ LSB value of the DAC.

3.6.7 Comparator Design and Offset Calibration

Fig.3.30 shows the dynamic comparator with offset calibration. By designing the comparator with a low input referred offset compared to a single LSB voltage, we have eliminated the requirement of a preamplifier in our design. It is a strong-ARM latch based design. Two variable MOS capacitors are added at the drain of input transistors M_1 and M_2 for calibration purpose. Comparator offset and decision time are two key parameters in this design. All comparators have offsets and their offset mismatches degrade the ADC linearity. Thus, it is desirable to de-

sign a comparator with small offset and fast decision time. One important factor that influences both offset and decision time is the comparator input common-mode voltage V_{cm} [Wicht et al. [2004]]. A small V_{cm} is preferred to reduce the offset. The reason is that the pre-amplification gain is larger at small V_{cm}, which suppresses the offset contribution from the latch. A large V_{cm} helps reduce the pre-amplification time, but the time duration of the latch regeneration phase is longer due to the reduction in the pre-amplification gain [Wicht et al. [2004]]. There exists an optimized V_{cm} for the decision time. The simulated residue voltage and comparator V_{cm} is shown in Fig.3.31. The transient simulation shows that V_{cm} converges to VDD/2, which is 550 mV in this case.

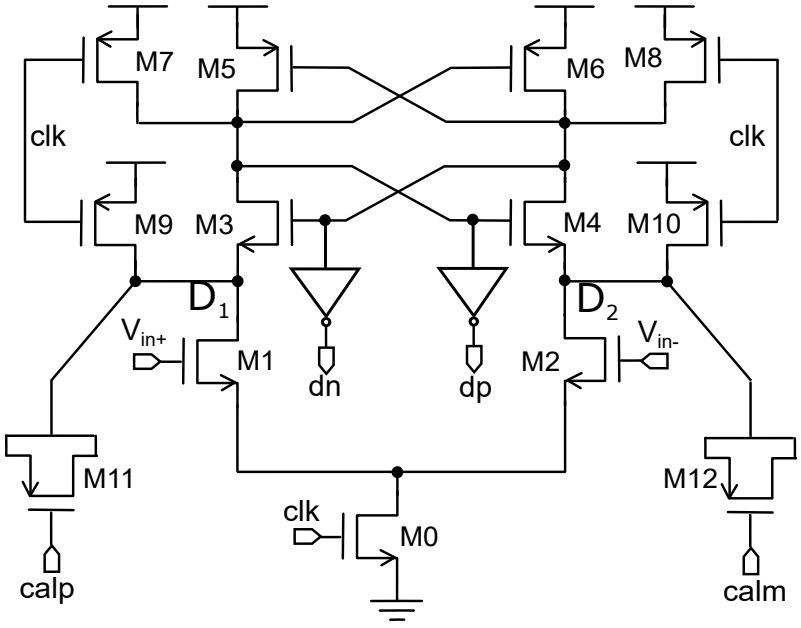


Figure 3.30: Dynamic comparator with varactor loading.

Fig.3.32 shows simulated values of comparator input referred offset sigma

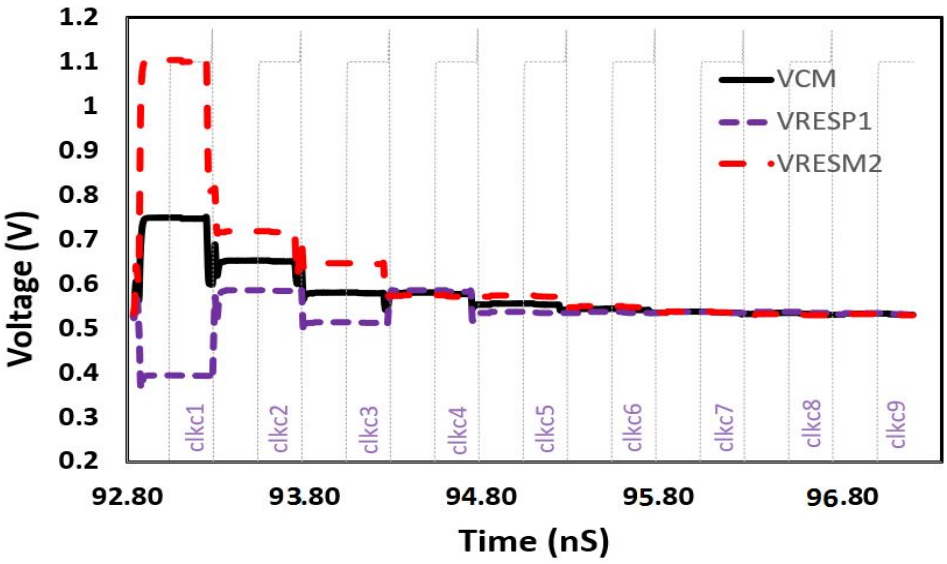


Figure 3.31: Comparator input voltage convergence and value of V_{cm} at different cycles.

σ_{os} w.r.t V_{cm}. At the expected V_{cm}, the radix-3 comparator is expected to have σ_{os} of $\sim$ 7.5 mV and the radix-2 comparator is expected to have σ_{os} of $\sim$ 4.5 mV. In the prototype ADC, the full-scale differential input swing is 1.1V and 1 LSB size for the radix-3 SAR ADC is about 8mV. The optimized comparator 1σ offset is 7mV, which is comparable to the LSB size. A 1000-point Monte-carlo simulation result is shown in Fig.3.33, with a mean of -984μV and a 1σ offset is 7.07mV.

In the prototype ADC, the 1 LSB size for radix-2 SAR ADC is about 5mV. The optimized comparator 1σ offset is 4.8mV, which is comparable to the LSB size. A 1000-point Monte-carlo simulation result is shown in Fig.3.34, with a mean of -684μV and a 1σ is 4.76mV.

Fig.3.35 shows the simulated power of the radix-2 and the radix-3 compara-

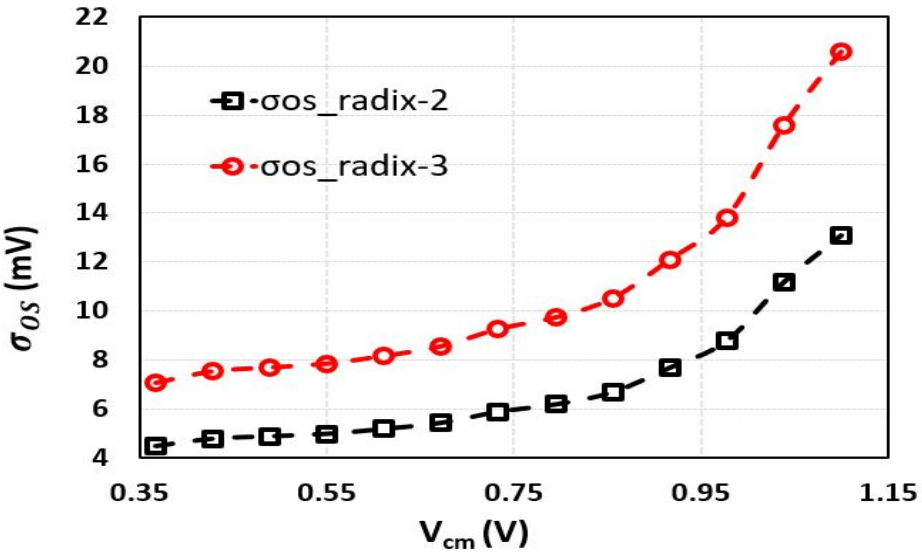


Figure 3.32: Simulated comparator offset σ at different V_{cm}.

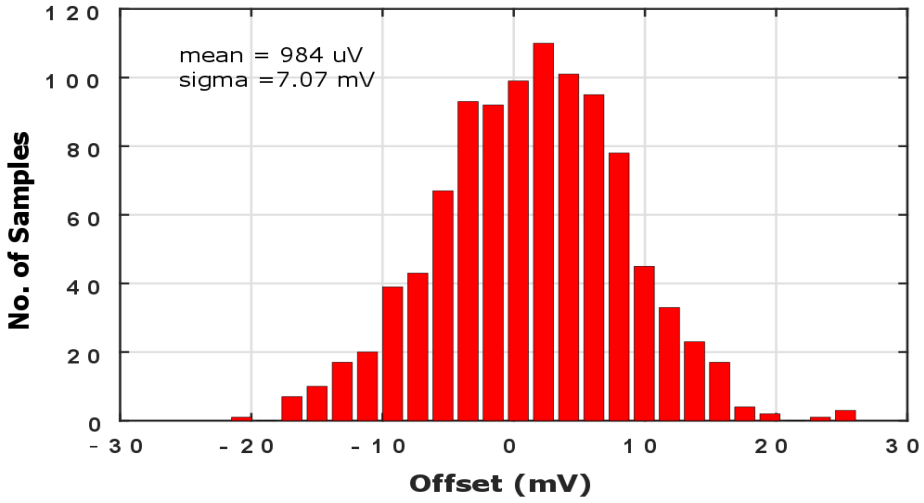


Figure 3.33: 1000-point Monte-carlo simulation for input referred offset of the radix-3 comparator.

tor. Depending on the V_{cm}, the radix-3 comparator power varies from 15 μW to 30 μW and the radix-2 comparator power varies from 30 μW to 45 μW.

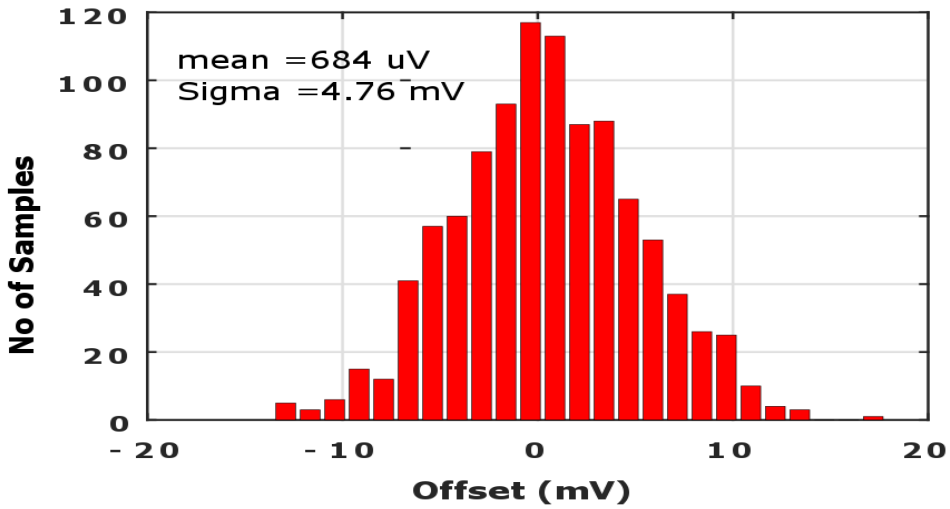


Figure 3.34: 1000-point Monte-carlo simulation for input referred offset of the radix-2 comparator.

Fig.3.36 shows the simulated clk-to-q delay of the radix-2 and the radix-3 comparators. Depending on V_{cm}, the radix-3 comparator might take 100 pS to 290 pS and radix-2 comparator might 88 pS to 240 pS.

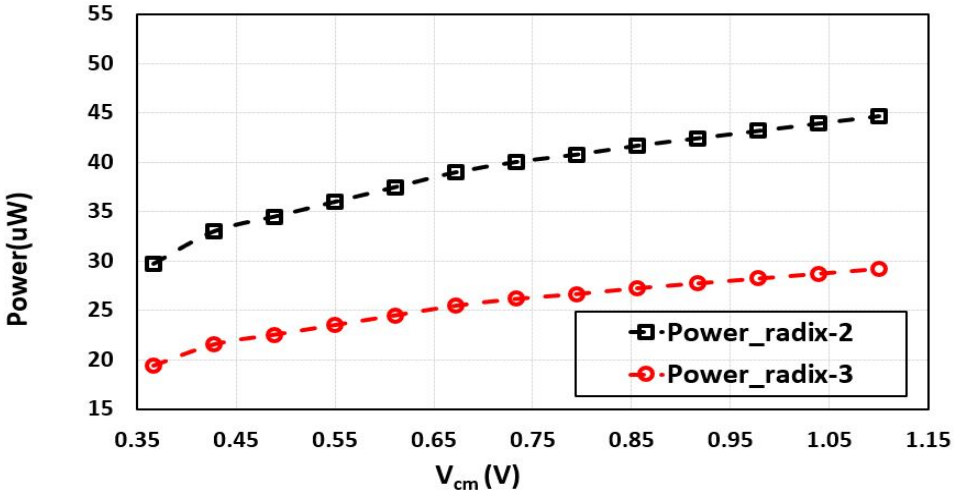


Figure 3.35: Simulated comparator power at different V_{cm}.

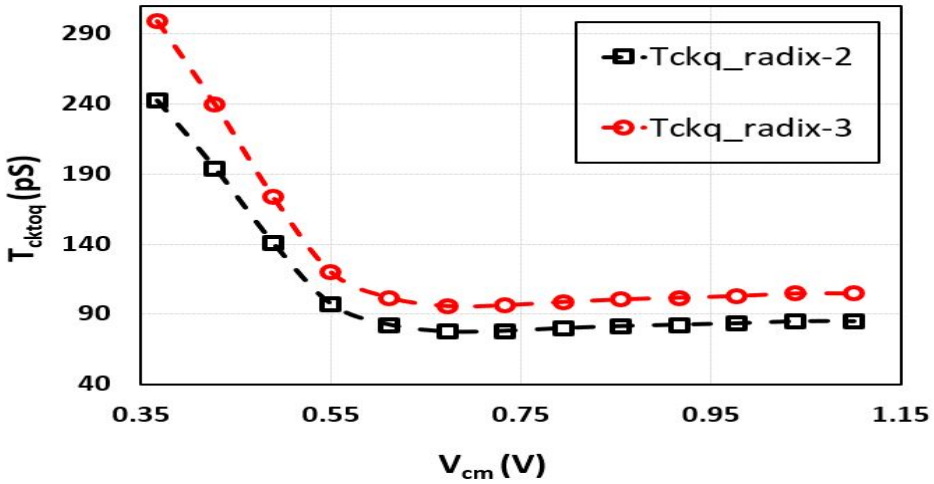


Figure 3.36: Simulated comparator clk-to-q delay at different V_{cm}.

To avoid linearity degradation due to offset mismatch, a V_{cm}-adaptive offset calibration technique is proposed. As is shown in Fig.3.37, the proposed calibration block consists of a dynamic comparator, a varactor and control pins. The control pins $calp$ and $calm$ are used to to change the voltage added to the gate of the M_{11} and M_{12} (Fig.3.30). The different feedback voltage on the gates of load MOS would result in different capacitance values. By adjusting the output loads attached to the comparator, the offset would be compensated.

The calibration technique works as follows: when the ADC is in the calibration mode, the calibration signal (OFFSET_CALIBRATION=1) is assigned from external control. That keeps the signal CLKSE high during whole calibration period and switches S0, S1 and S2 are turned on and they connect the positive and negative terminals of the comparators to V_{cm} (see Fig.3.37) and hence, a zero differential input voltage is applied to the inputs of the comparators. For simplicity

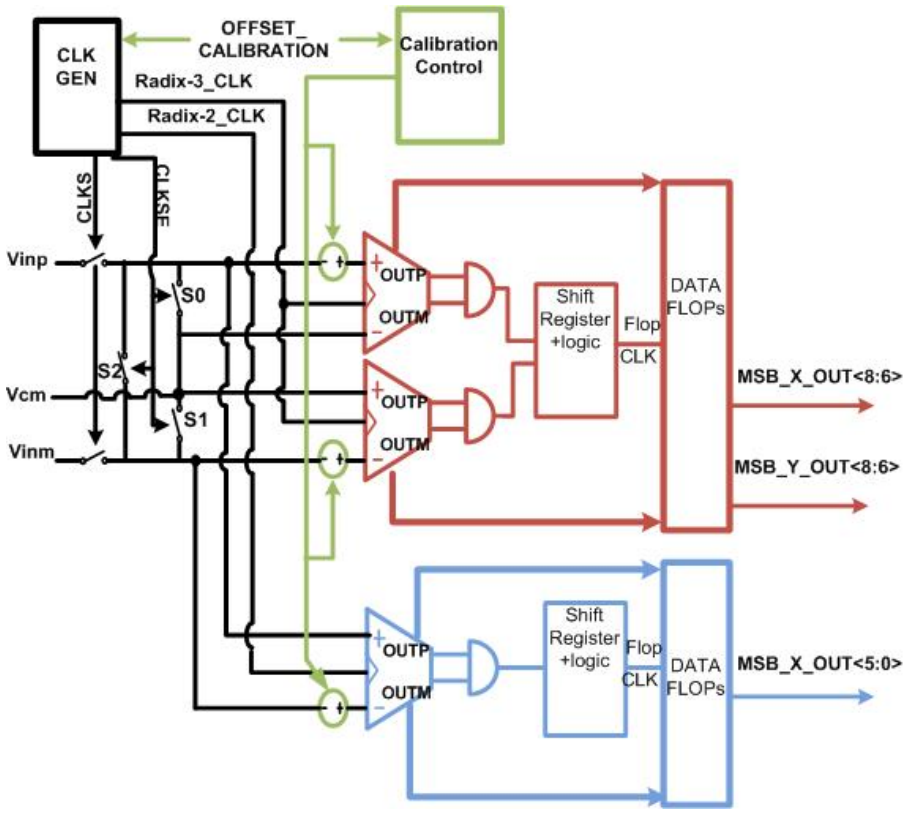


Figure 3.37: Comparator calibration scheme in proposed hybrid SAR ADC.

of design, we do not need any external clock or extra circuitry for this calibration procedure. As our design is fully synchronous, we just slow down the external clock to give the comparators enough time so that their differential inputs settle well and stay close to zero. Fig.3.38 shows the timing diagram of calibration. CLKS turns on for one clock cycle as usual convergence operation, but does not affect the input voltage of the comparators. CLKS needs to be high to reset all the DATA flops and shift registers in each conversion time. Radix-2_CLK and Radix-3_CLK toggles 6 and 3 times respectively as usual operation, but at a much

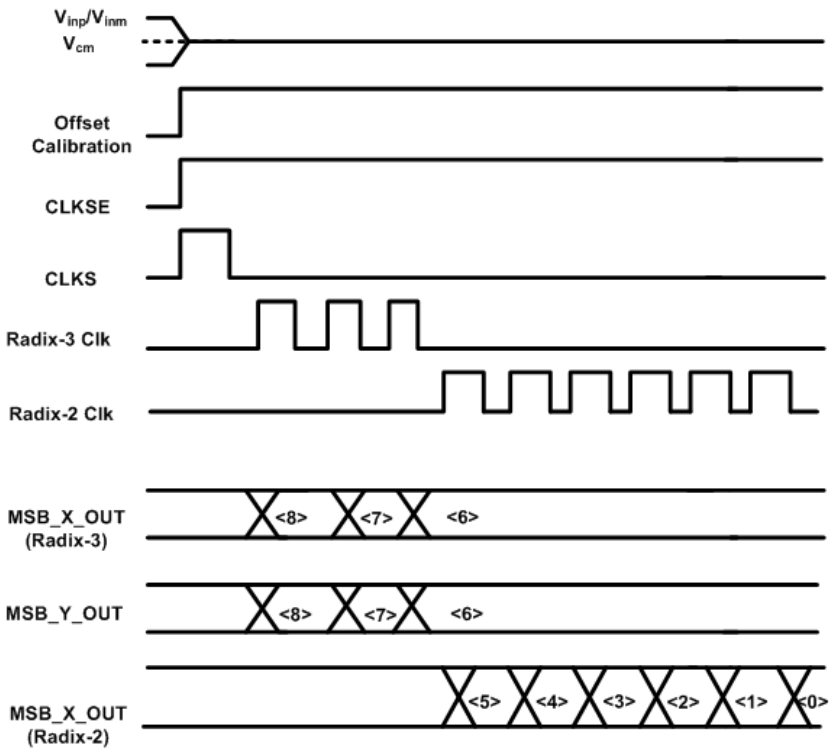


Figure 3.38: Timing diagram of comparator calibration.

slower frequency as described earlier. As a result, comparators will toggle and their outputs will be latched at the output flops. Radix-3 comparators provide outputs MSB_X_OUT$< 8 : 6 >$ and MSB_Y_OUT$< 8 : 6 >$. Radix-2 comparator provides outputs MSB_X_OUT$< 5 : 0 >$.

If there is no offset, each comparator's output jumps between "1" and "0" due to thermal noise. Comparator thermal noise in the design is about 400μV, which is much smaller than the offset. When a large offset in present, the comparator's output keeps staying at either "1" or "0" as shown in Fig.3.39. The offset can be

calibrated by tuning the MOSFET based varactors shown in Fig.3.30, whose values are controlled by its gate voltage $calp/calm$. Suppose that node D_1 is discharged faster than node D_2, mainly due to the mismatch of input transistors M_1, M_2 according to [Harpe et al. [2014]]. It means that the comparator output d_p would reach GND and d_n would reach VDD even though the differential input signal is zero (V_{in+}=V_{in-}).

To compensate for this offset, the gate voltage of M_{11} is reduced with an external potentiometer control knob in the calibration unit. By doing this, the capacitance of M_{11} connected to the node D_1 will be increased. The larger capacitance load of node D_1 apparently will cause its discharging speed to be slower during the next cycle. Similarly, the complementary voltage to the gate of M_{12} will be changed in the opposite way. At last, the mismatch of the discharging speed of nodes D_1 and D_2 will be reduced to minimal. The offset caused by device mismatch will be calibrated.

The calibration range is designed to be 20mV which is 3 times the simulated 1σ offset. By observing the comparator's output, we can tell whether the comparator offset has been calibrated or not. The calibration is finished when the comparator output is evenly distributed between "1" and "0" (Fig.3.39). 1024 ADC outputs are captured by a logic analyzer during the calibration. The comparator offset is removed when the probability that its output code equals to "1" is around 50%. The measured probability of the comparators outputs being "1" versus its calibration voltage $calm$ for the radix-2 comparator is plotted in Fig.3.40. The proposed calibration is simple and it does not require special DAC patterns to generate

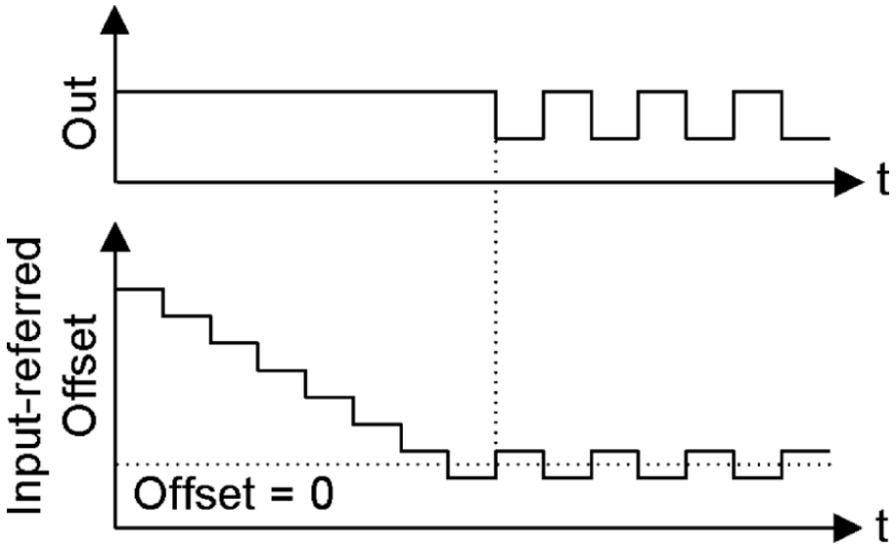


Figure 3.39: Change of input referred offset of comparators with calibration.

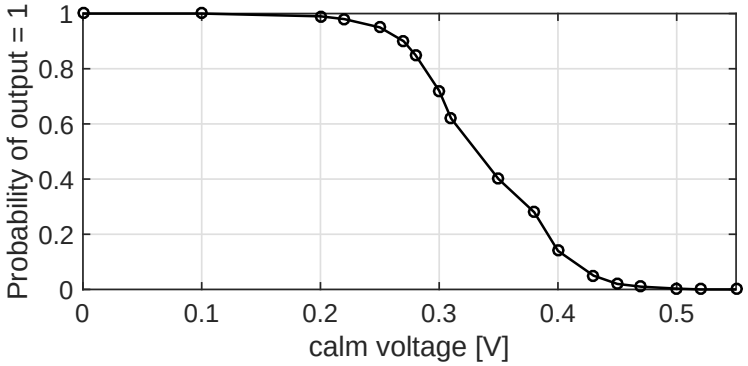


Figure 3.40: Probability of radix-2 comparator output being '1' versus its $calm$ with $calp$ fixed at 1.1V.

the operating V_{cm} in [Verbruggen et al. [2012]] or special input voltages that cause metastability at different comparators in [Jiang et al. [2012]]. Furthermore, since the same DAC switching procedure happens during calibration, each comparator offset is calibrated at the same V_{cm} as that of the normal ADC operation. This is

necessary in our modified monotonic switching technique since V_{cm} varies in each comparison cycle and the comparator offset depends strongly on V_{cm} [Chen et al. [2014]; Wicht et al. [2004]].

3.7 Simulation Results

A prototype (3+6)-bit hybrid ADC, a 6-bit radix-3 and a 10-bit radix-2 ADC were designed in a 40nm CMOS process with $1.86fF$ minimum capacitor value, 1.1 V supply and simulated in SPICE with an input sine wave of amplitude of 1.1 V and with varying sampling frequency. To verify our proposed architecture, we ran transient simulation and captured the data from ADC output and found out the frequency response of the ADC.

Table 3.7: Comparison of performance.

ADC	i(Total) (uA)	No of Cycle	No of Bits	Sampling Freq(MHz)	FOM (fJ/Conv)
Radix-3	2552	8	9.6	250	14.47
Radix-2	1996	12	10	167	12.92
Hybrid	1397	10	9.5	200	10.61

The SNDR values are plotted in Fig.3.41. It can be seen that, to achieve the desired SNDR, the radix-2 ADC can operate at maximum speed of 167 MHz whereas the hybrid and radix-3 ADCs can operate at 200 MHz and 250 MHz, respectively. The simulation result closely follows the data of Table 3.3. Table 3.7 shows the comparison among the radix-2, radix-3 and hybrid SAR ADCs.

The radix-3/radix-2 based hybrid SAR ADC saves 30% power compared to the conventional radix-2 SAR ADC and 45% power compared to the radix-3

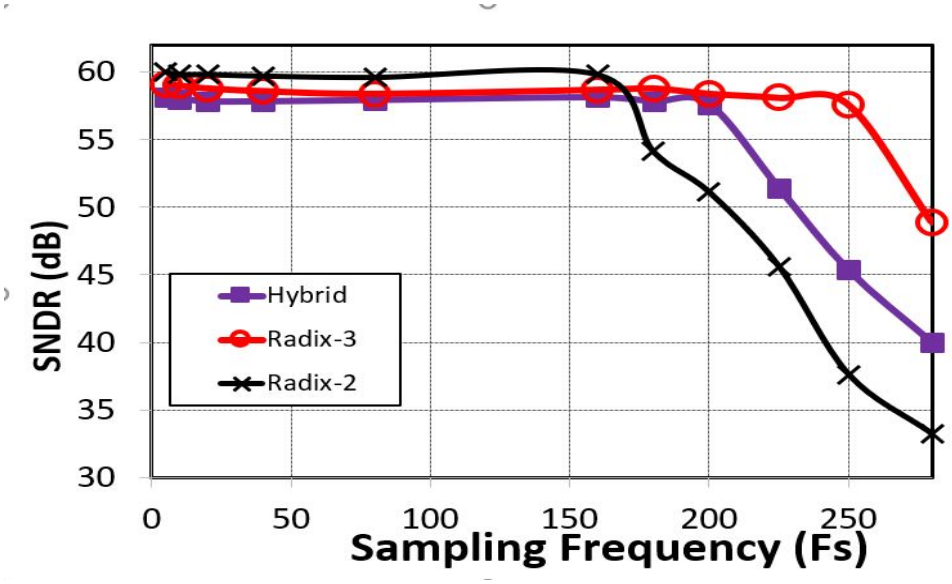


Figure 3.41: Comparison of maximum speed

SAR ADC. It sacrifices 25% sampling frequency compared to the radix-3 SAR and it gains 16.67% sampling frequency compared to the conventional radix-2 SAR ADC. It achieves 36% performance (FOM) compared to the radix-3 SAR and it gains 21.8% performance compared to the conventional radix-2 SAR ADC.

The transient simulation plot is presented in Fig.3.42. Sampling clock, CLKS, is high for one cycle for sampling the input voltage. The radix-3 comparator clock, Radix-3 CLK, toggles three times and the radix-2 comparator clock, Radix-2 CLK, toggles six times. DAC output voltages (VRESP and VRESM) converge to V_{cm} after nine cycles of convergence. The 1024 point FFT plot of the hybrid ADC simulated with a sampling frequency of 200 MHz is shown in Fig.3.43. The SNDR is 58.1 dB which verifies the proposed ADC architecture idea.

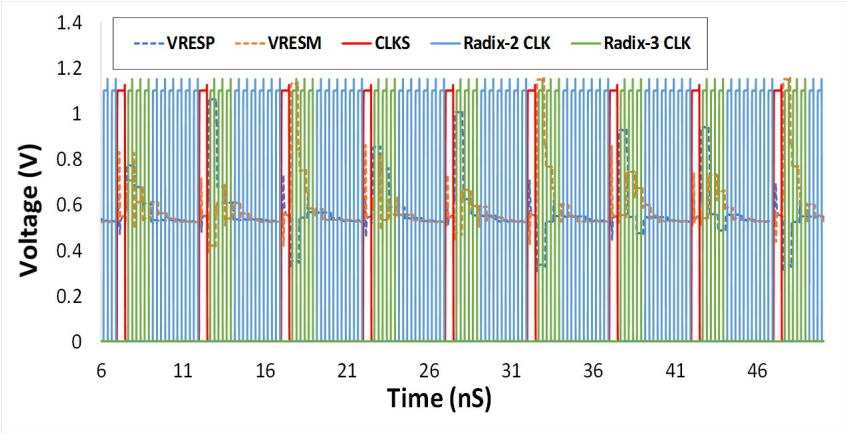


Figure 3.42: Transient simulation of the hybrid SAR ADC.

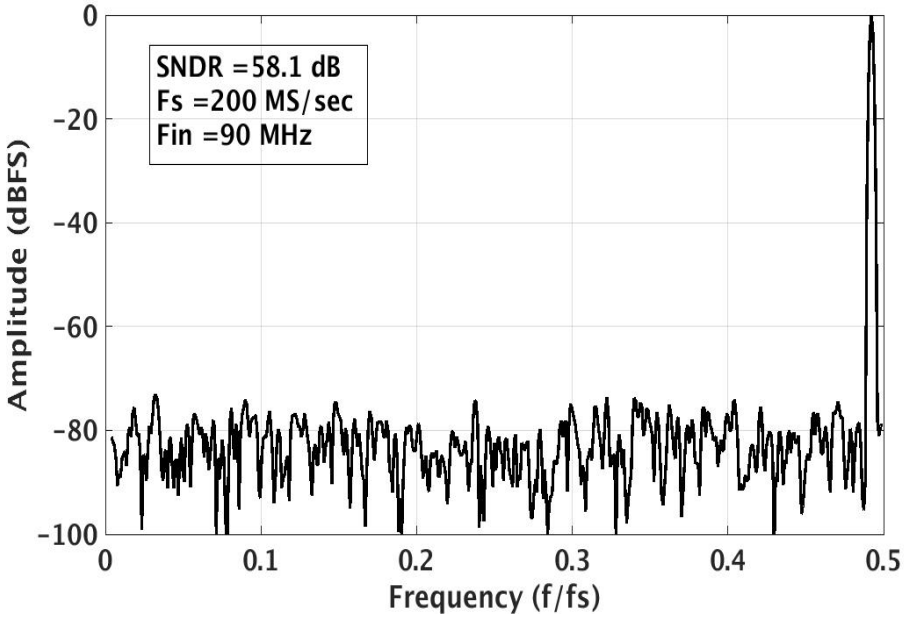


Figure 3.43: 1024 point FFT plot of the hybrid SAR ADC.

3.8 Conclusion

In this chapter, a novel hybrid SAR ADC based on a radix-3/radix-2 search approach has been introduced and designed and characterized. Also, a calibration technique to reduce capacitor mismatch and input referred offset of dynamic comparators has been proposed. The main advantage of this architecture is that it does not need any extra capacitor DAC arrays and the calibration circuit is programmable for any size of DAC array with a small digital circuit overhead. Theoretical analysis and circuit based simulation also verified the proposed idea.

Chapter 4

Packaging, Testing and Measurement

In this chapter, we focus on the silicon implementation and testing of the proposed radix-3/radix-2 based hybrid SAR ADC. The chapter is organized as follows: first we discuss the floor planning and the placement of the I/O pins to minimize the amount of signal feed through and noise coupling to achieve target accuracy. Then we focus on the setup of the testing environment. It includes discussion of the testing equipment, the making of the printed circuit board (PCB), and the testing flow. Finally, in the last part of this chapter, we discuss the measurement results of our fabricated chip.

4.1 Packaging

Common causes of noise issues during the testing of SAR ADCs are due to presence of analog and digital components onto a single system. Therefore, it is important to consider the potential noise sources at the design stage to prevent degradation in accuracy and difficulties during chip debugging.

To understand the sources of noise, we ran conservative extraction of the layout and simulation was also very conservative to include as much of the existing parasitic capacitance and inductance effects as possible. However, due to long sim-

ulation time and complexity, it is very unlikely to detect all the off chip sources of errors. During our tapeout, we followed some guidelines to determine the pin placements, power/ground decoupling capacitors, interconnect coupling and the design of our printed circuit board (PCB) in order to create a robust system against noise.

At high frequencies, inductances associated with bond wires play a vital role for the stability of the internal power and ground. A primary solution to reduce the total impedance is to add more parallel power/ground pins. Also, it is highly recommended to separate the digital and analog power supplies to improve the isolation between the noisy digital switching and quieter analog switching.

Separate PADs for analog and digital power supplies and grounds are used to have quieter analog. Also, to avoid noise coupling through the substrate, the noisy circuit should be placed as far from the quiet analog blocks as possible.

To further reduce the power supply noise, decoupling capacitors between the power and ground nodes should be used. On-chip decoupling capacitors are needed to reduce this high-frequency noise. Empty areas on the die can be filled with decoupling capacitors. The capacitors are built by putting layers of MOM capacitors (using all metal layers) and MOSCAP in parallel.

Combining the techniques, introduced previously, help provide significant filtering that enables lower impedance and cleaner supplies for the analog circuits on the die.

Fig.4.1 shows the top level GDS of the fabricated chip. The analog portion was placed on the left side. Dynamic comparators and other digital circuits were

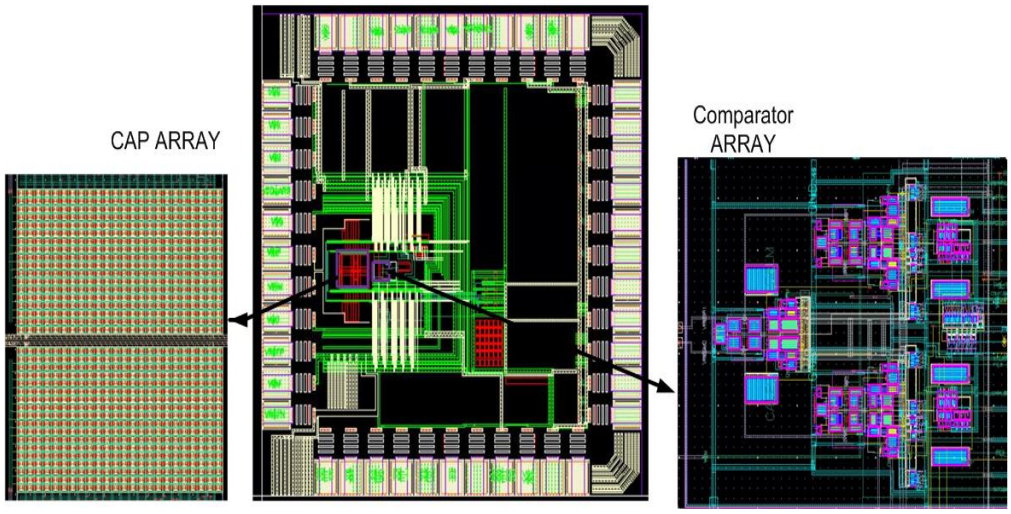


Figure 4.1: Top level GDS of the fabricated chip.

placed on the right side in a separate power domain. Long analog signal routing is avoided to prevent potential noise coupling. Digital and analog parts of the circuit are kept as far away from each other as possible. For the cases where analog and digital wiring cannot be separated, shielding is used to reduce noise coupling.

The same theory can be applied to the I/O pin placement. Analog output pins should be separated from the digital output pins, preferably on the opposite side of the chip. Neighboring analog output pins are also isolated by quiet ground pins. The bonding diagram and the location of the I/O pad placement are shown in Fig.4.2. The die has a total of 41 output pins and the TQFP package has a total of 44 output pins. The design follows the general guideline introduced previously. As shown in the diagram, all of the sensitive analog signals including analog power supply (V_{analog}) and the reference voltages ($V_{reference}$, and V_{cm}) are placed on the left side of the die, the noisy digital output pins along with digital power supply

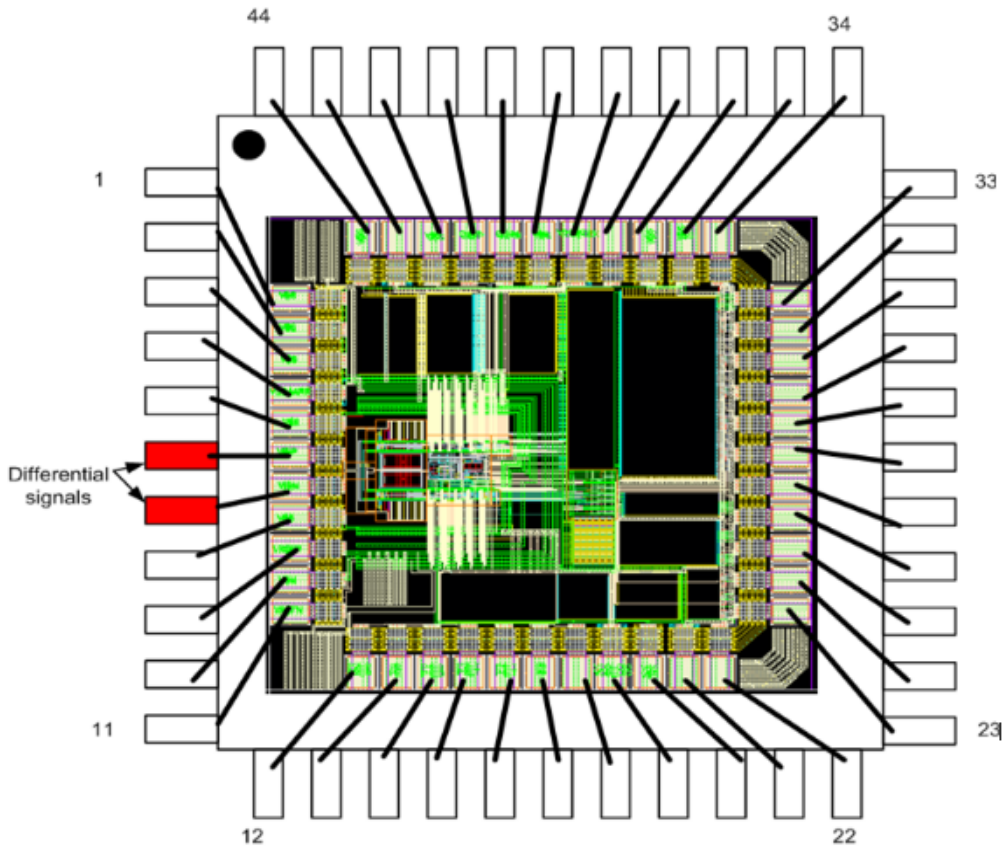


Figure 4.2: Bonding diagram of the fabricated chip.

(V_{out_buf}) are placed on the right side of the die. All the calibration pins and digital power supply ($V_{digital}$) are placed on the top of the die and all the clock generation pins with clock power supply are placed on the bottom of the die.

4.2 Test Setup

The ADC test setup is an important part of the design in order to obtain accurate measurement results. After the design comes back, the first step is to choose

a suitable package for the die. We used the TQFP package. The second step is to design a printed circuit board (PCB) that can be used as an interface between the packaged die and the external test equipment. Off-chip capacitors have a maximum frequency at which they behave as a capacitor, because capacitors also have a series inductance. At certain frequencies, the impedance begins to look more inductive than capacitive. Large capacitors have lower self-resonance frequencies. As a result, to maintain capacitive characteristic even at high frequencies, it is important to put capacitors with different values in parallel. To achieve better results, off-chip capacitors should be placed as close to the packaged chip as possible.

The test board in shown in Fig.4.3. Linear regulators with low dropout voltage (LT3021) are used on the PCB to supply clean power and reference voltages. Separate linear regulators are used for different supplies and references. As a result, there are a total of five regulators on the PCB in order to generate V_{analog}, $V_{reference}$, V_{cm}, $V_{digital}$ and V_{out_buf}. The separation of analog power supply, digital power supply and reference voltage ensures low noise coupling between them.

A single ended sine wave signal is generated using a signal generator. A band pass filter is used at the output of the signal generator to improve the purity of the input signal. This input signal is then transformed into a differential signal using two transformers made by mini-circuit. The use of two transformers helps reduce the second order distortion caused by the transformers. The CMOS clock is generated by a synthesized clock generator.

The digital output data is collected by a logic analyzer. The probes of the logic analyzer add a small capacitive load to the output drivers of the die.

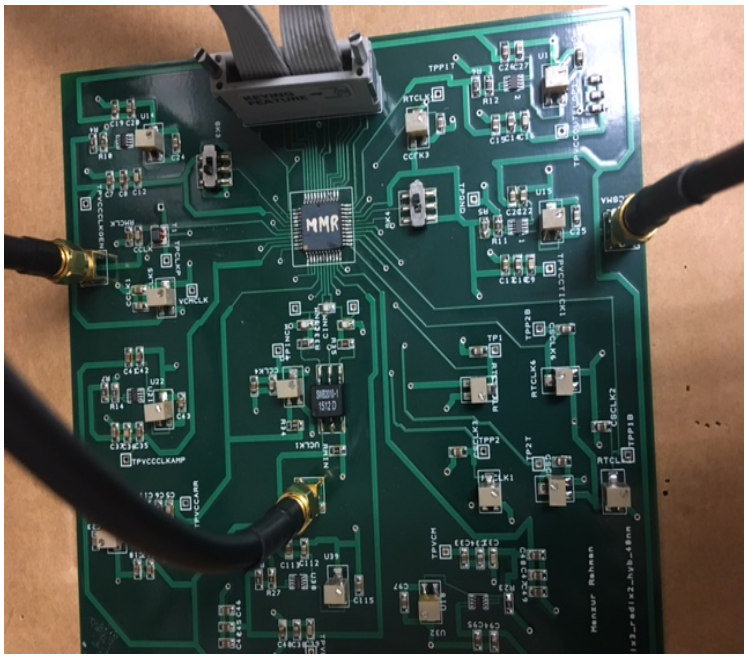


Figure 4.3: PCB setup of fabricated chip in TSMC 40nm technology.

4.3 Measurement Results

The prototype ADC is fabricated in standard TSMC 1P8M 40nm low-power CMOS technology with 1.1V supply voltage. The active area is roughly $0.0412mm^2$. The DAC is implemented with standard MOM capacitors from metal 3 to metal 5 with a unit capacitance of $1.86fF$. Several chips are measured and all measurements are performed at room temperature. Fig.4.4 shows the die photo of the fabricated chip in TSMC 40nm technology.

Fig.4.5 shows the measured frequency spectrum of the chip. The proposed comparator calibration was done on chip. With a sampling frequency of 30 MHz and an input frequency of 1.5 MHz, the ADC can achieve an SNDR of 56.9 dB and

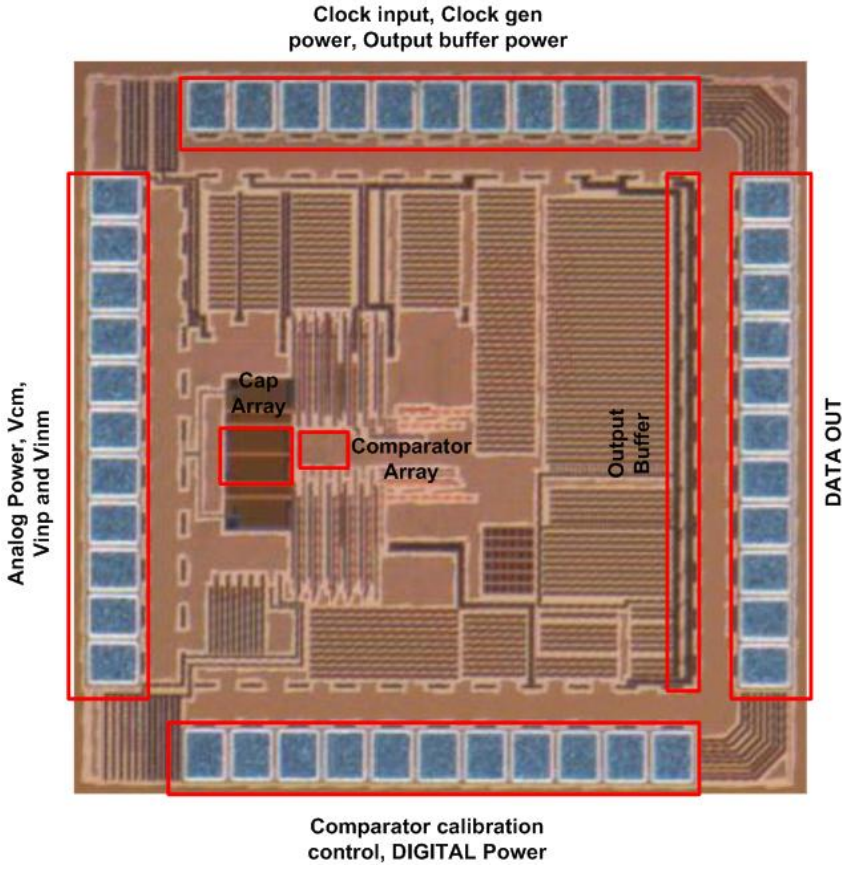


Figure 4.4: Die micrograph of the fabricated chip in TSMC 40nm technology.

an SFDR of 67.5 dB. Keeping the same sampling frequency, at input frequency of 12 MHz, the ADC can achieve an SNDR of 53.4 dB and an SFDR of 63.5 dB.

Fig.4.6(a) presents the measured SNDR under different sampling frequencies with a 7.5 MHz input. It shows that ADC gives $\sim$ 56 dB SNDR over the whole range. Fig.4.6(b) presents the measured SNDR under different input frequencies with a 30 MS/s sampling rate. The ADC was able to maintain consistent performance over the whole range. Fig.4.7 presents the linearity of the designed hybrid

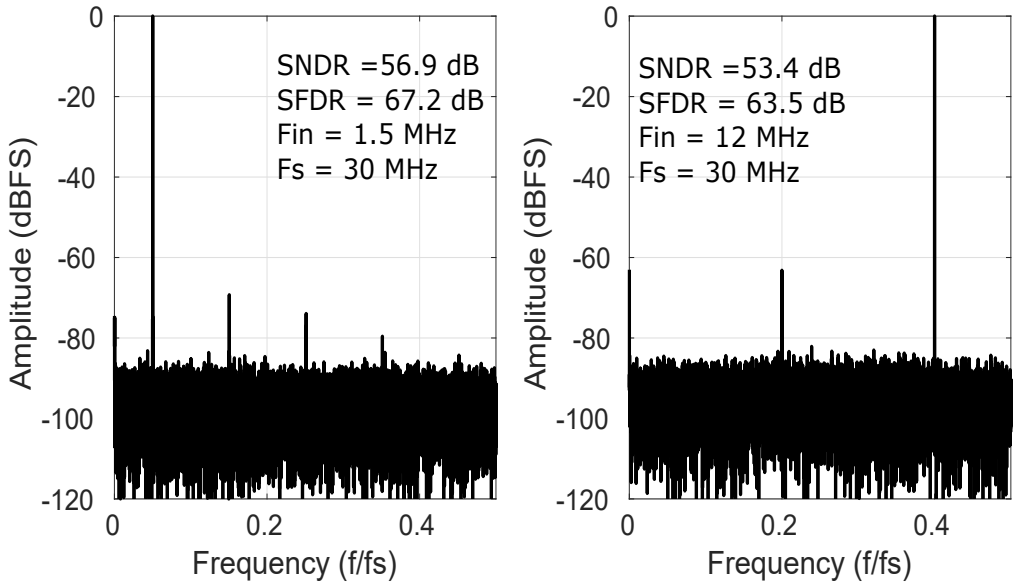
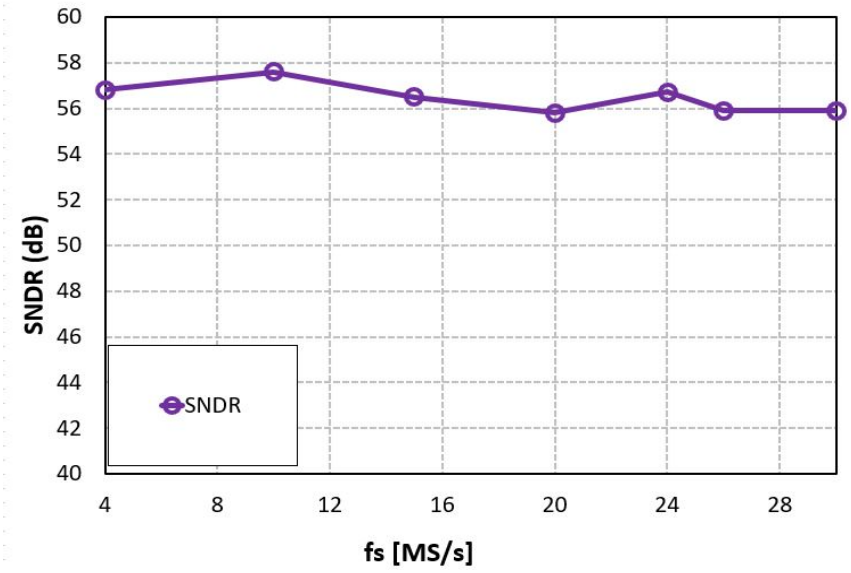


Figure 4.5: Measured 32768 point FFT spectrum with 30MS/s sampling rate and (a) 1.5 MHz input and (b) 12 MHz input.

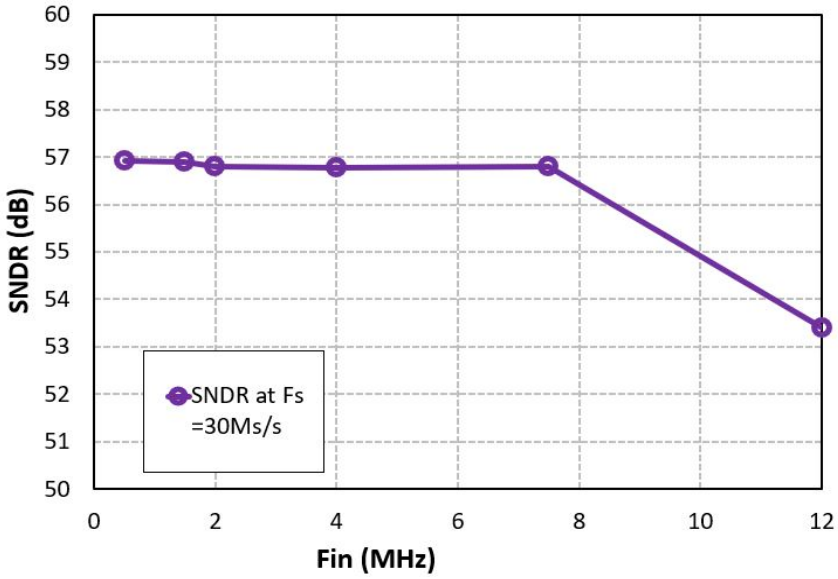
SAR ADC. The input amplitude was varied from -35 dBFS to 0 dbFS and measured SNDR varied linearly in accordance with the input amplitude.

Fig.4.8 presents the INL and DNL found from the chip measurement. The DNL found to be +0.83 LSB/-0.76 LSB and the INL value was +0.32 LSB/ -0.8 LSB.

Fig.4.9 shows the different power supplies for the designed hybrid SAR ADC. The total power consumption at 30MS/s is 0.38mW, whose breakdown is: 0.169mW (44%) used by the digital logic and comparators ($V_{DIGITAL}$), 0.125mW (33%) used by DAC (V_{Analog}) and 0.086 mW (28%) consumed by reference volt-



(a)



(b)

Figure 4.6: (a) Measured SNDR under different sampling frequencies with 7.5 MHz input (b) under different input frequencies with 30 MS/s sampling rate.

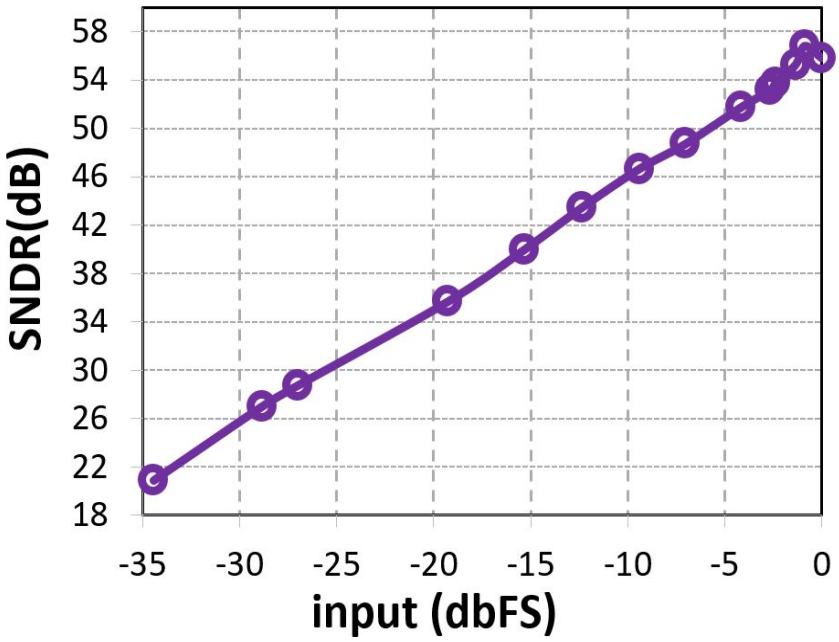


Figure 4.7: Measured linearity of the hybrid SAR ADC.

age ($V_{Reference}$). Fig.4.10 presents the power distribution between the radix-2 and the radix-3 architectures. Fig.4.10(b) shows that, in digital domain ($V_{DIGITAL}$) the radix-2 architecture consumes 62%, where the radix-3 architecture consumes 38% power. The radix-2 architecture consumes more power as it has 7 bits and it has more flops and the dynamic comparator also has to toggle more than the radix-3 search. As discussed in previous chapter, the radix-2 dynamic comparator also consumes more power as it has higher resolution than the radix-3 comparator. Fig.4.10(c) shows that in the DAC (V_{Analog}), the radix-3 consumes 82% power. The MSB capacitors are from the radix-3 architecture and their sizes are much larger than the radix-2 architecture. Fig.4.10(d) shows that in reference voltage domain ($V_{Reference}$), radix-3 consumes 57% power. Though there are more num-

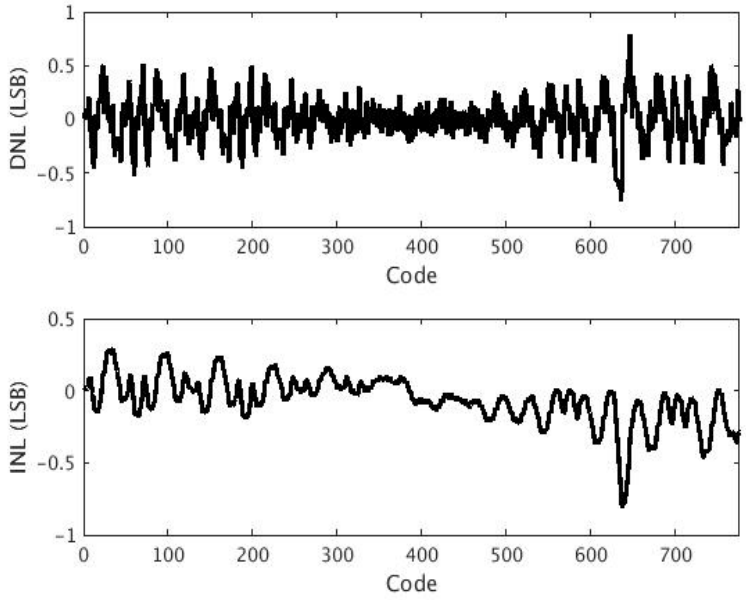


Figure 4.8: Measured DNL/INL from the designed hybrid SAR ADC.

ber of bootstrapped switches for radix-2 architecture, the sampling switches for the radix-3 architecture are really big and consume more power. Fig.4.10(e) shows that overall, the radix-3 architecture consumes 56% power and the radix-2 architecture consumes 44% power.

The measured Walden figure-of-merit (FOM) [Walden [1999]] at the Nyquist rate is 21.5 fJ/conversion-step. Fig.4.11(a) and Fig.4.11(b) present the comparison of FOM among this work and works published in ISSCC 2009-2017 and VLSI 2009-2017 from [Murmann] in terms of sampling frequency (Fs) and signal-to-noise-and-distortion ratio (SNDR), respectively. The FOM is well comparable with other published works in terms of sampling frequency as well as SNDR. Fig.4.12 compares the area of the ADC with the works published in ISSCC 2009-2017 and

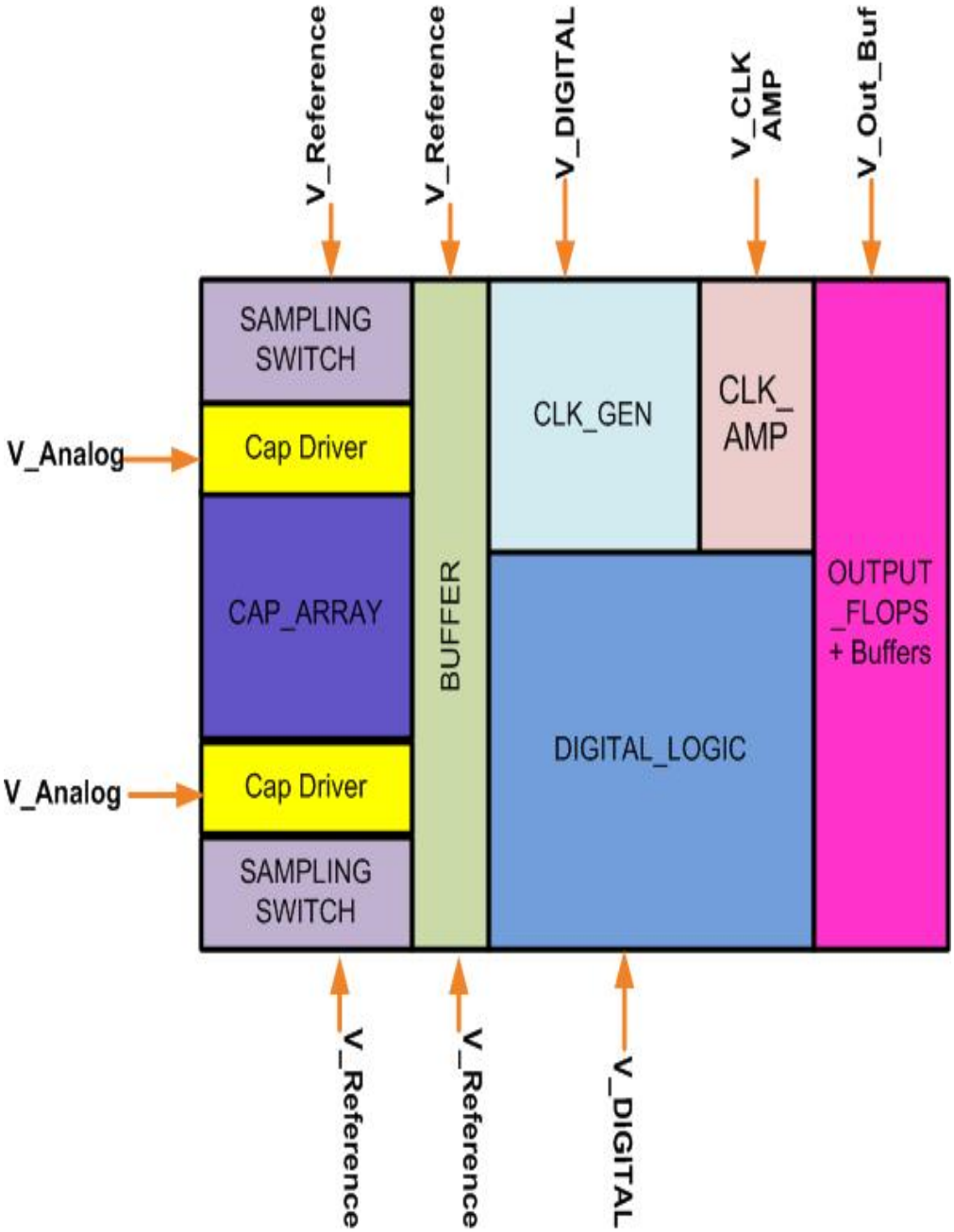


Figure 4.9: Different power sources for the hybrid SAR ADC.

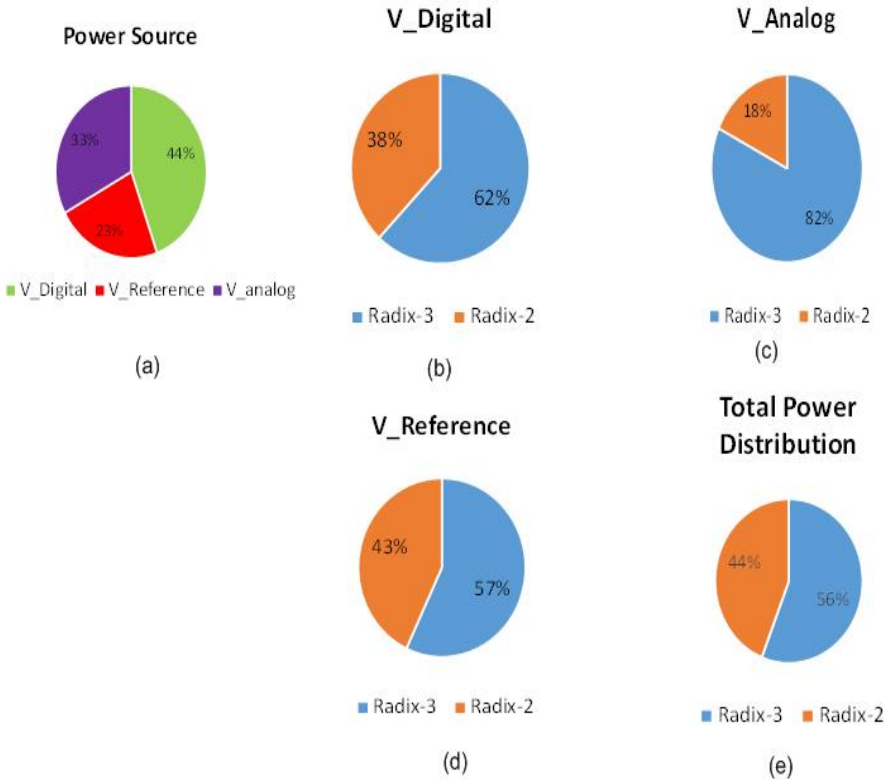
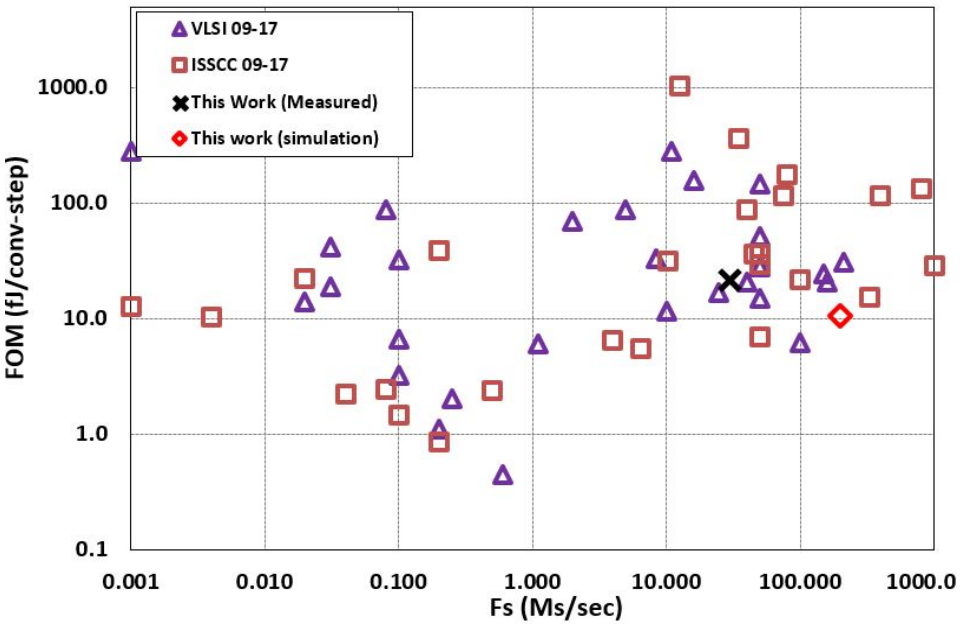
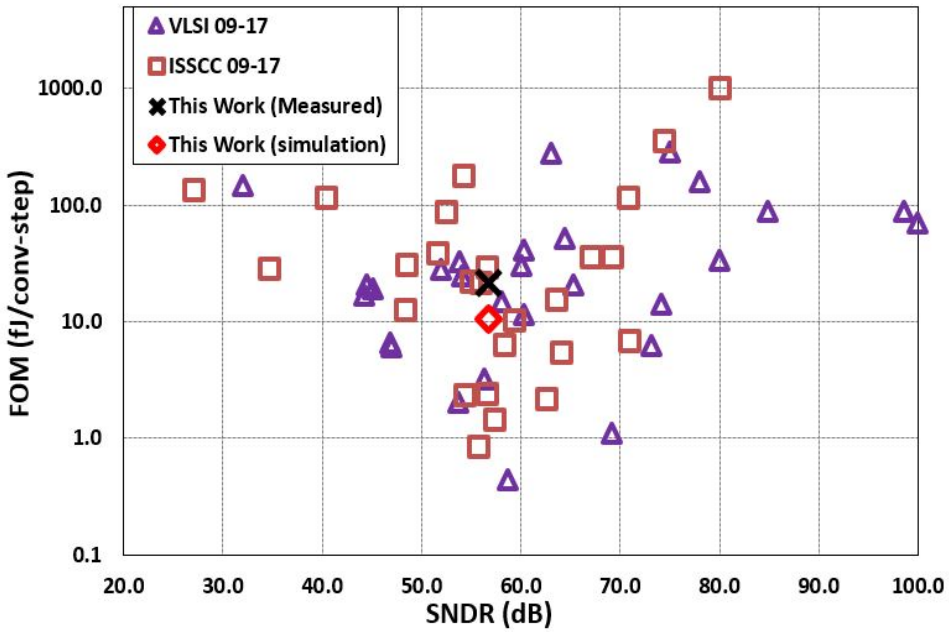


Figure 4.10: Power distribution between the radix-3 and the radix-2 architecture

VLSI 2009-2017 from [Boris Murmann] in 40nm process node. This ADC achieves competitive area of all the ADCs that have 10 bit or higher resolution.



(a)



(b)

Figure 4.11: Comparison of FOM with ISSCC '09-'17 and VLSI '09-'17 w.r.t (a) sampling frequency (Fs) (b) SNDR.

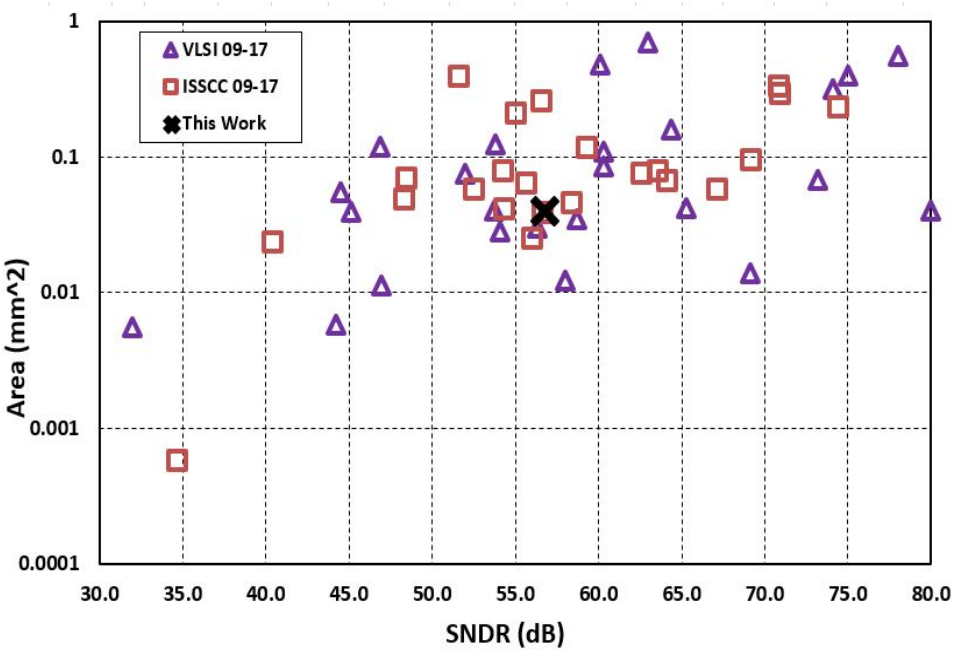


Figure 4.12: Comparison of area with ISSCC '09-'17 and VLSI '09-'17 in 40 nm CMOS process

4.4 Conclusion

In this chapter, setup for chip testing and measured results have been discussed. The ADC achieved 9.2 ENOB at 30MS/s sampling rate and consumed 0.38mW power. The silicon results verified the concept of a novel radix-3/radix-3 based hybrid SAR ADC.

Chapter 5

Conclusion and Future Directions

5.1 Conclusion

This thesis focuses on multi-bit-per-step, high speed and low power SAR ADCs. Chapter 2 presents a novel technique to develop a radix-3 SAR ADC. To the author's best knowledge, this is the first work that comprehensively introduces an efficient switching algorithm for a radix-3 SAR ADC. This is the first radix-3 SAR ADC than can be programmable for any number of bits. Also, the characterization of radix-3 SAR ADC has been done. Several design challenges such as comparator offset mismatch, common mode noise, capacitor mismatch, etc. have been considered and approaches have been introduced to solve these challenges. Also, DAC energy, speed gain, switching energy, DAC sizes, etc. have been compared in detail with a conventional radix-2 SAR ADC. We also present the capacitor calibration for the very first time for a radix-3 DAC array. The capacitor ratio is different for a radix-3 SAR ADC and the calibration technique is unique and novel. Finally, we introduced a novel and simple technique for comparator offset calibration with minimum hardware cost. Including all these features, it is evident that proposed radix-3 SAR ADC is suitable for applications that require high-resolution and high speed SAR ADCs.

Chapter 3 presents a novel technique to develop a radix-3/radix-2 based hybrid SAR ADC to introduce a balance between speed and power. To the author's best knowledge, this is the first work that proposed the combination of a radix-3 SAR ADC for high speed and a radix-2 SAR ADC for low power and accuracy. Also, a monotonic switching technique is adopted for the radix-2 search to reduce the DAC capacitor size and hence, to reduce switching power. This ADC can be configured for any resolutions. A detailed characterization of the radix-3/radix-2 based hybrid SAR ADC has been done. It has been shown that typical design challenges such as comparator offset mismatch, common mode noise, capacitor mismatch, etc. do not affect the linearity of this ADC as we provide solutions for these as well. Also, DAC energy, speed gain, switching energy, DAC sizes, etc. have been compared in detail with a conventional radix-2 SAR ADC and a radix-3 SAR ADC and it proves to have the best gain over the radix-2 and the radix-3 SAR ADCs with respect to these characteristics. We also present the capacitor calibration for the very first time for a radix-3/radix-2 based hybrid SAR ADC. Finally, we introduced a novel and simple calibration technique for comparator offset calibration with minimum hardware cost. Including all these features, it is evident that the proposed radix-3/radix-2 based hybrid SAR ADC is suitable for applications that require high-resolution, high speed, and low-power.

Chapter 4 presents a detailed description of the chip and testing board setup. Also, several considerations have been made to avoid the power supply noise in analog and digital domain. Detail description of chip packaging, pin location and the consideration behind that have been presented. Finally the measurement data

for a 10 bit radix-3/radix-2 based hybrid SAR ADC has been shown in Chapter 4. The hybrid ADC achieves an SNDR of 56.9dB at 30MS/s sampling rate and achieves an FOM of 21.5fJ/conversion-step.

5.2 Future Directions

The proposed radix-3 SAR ADC can be used in high speed SAR ADC applications. It can be modified for 6-bit or 5-bit configurations and can be optimized with loop unrolled techniques proposed by [Chen et al. [2014]] to achieve a higher convergence speed. Another interesting path to reduce the DAC size is to use a hybrid architecture, such as [Sanyal et al. [2014]]. By doing this, the first stage SAR ADC only needs to resolve fewer bits, leading to reduced DAC size and power.

In the radix-3/radix-2 based hybrid SAR ADC, a unit capacitor of $1.86fF$ is used, which is the minimum MOM capacitor provided in the PDK. Since the DAC switching power is proportional to the unit capacitor size, a smaller unit capacitor is desired. This can be achieved by designing a custom unit capacitor with metal wires. It is also a good direction to investigate low power calibration techniques to calibrate the capacitor mismatch in order to use the ultra small unit capacitors. Also, the capacitor calibration can be implemented on chip and it will be interesting to see the efficacy of the proposed calibration algorithm. During the measurement, we learned that the SAR logic consumes a significant power out of total ADC power. Although the power of logic circuits will be less in more advanced technologies, it is still desirable to explore circuits design techniques to optimize the logic power.

Although the power and linearity of the radix-3/radix-2 based hybrid SAR

ADC have been improved by using optimized switching technique and capacitor calibration technique, there is still some work which can be done in the future. One possible direction is to design asynchronous clocking to optimize the clock period for different bits. For example, the MSB bits require more time to resolve than the LSB bits and it can improve the speed of the SAR ADC. Also, synchronous design can be investigated to control different clock cycles for different bits and it will be easier to control and debug on silicon.

Appendix

Appendix 1

List of publications

1. **Manzur Rahman** and Nan Sun, "A 21.5 fJ/conv, 30MS/s, 380μW, 10-bit Radix-3/Radix-2 Based Novel Hybrid SAR ADC in 40nm CMOS Process," to be submitted to *IEEE Transaction on Circuits and Systems-II* (TCAS2).

2. **Manzur Rahman**, Arindam Sanyal and Nan Sun, "A Novel Hybrid Radix-3/Radix-2 SAR ADC With Fast Convergence and Low Hardware Complexity," *IEEE Transaction on Circuits and Systems-II* (TCAS2), vol. 62, no. 5, pp.426-430, May 2015.

3. **Manzur Rahman**, Long Chen, and Nan Sun, "Algorithm and implementation of digital calibration of fast converging radix-3 SAR ADC," *IEEE International Symposium on Circuits and Systems* (ISCAS), pp. 1336–1339, 2014.

4. Long Chen, **Manzur Rahman**, Sha Liu, and Nan Sun, "A fast radix-3 SAR analog-to-digital converter," *IEEE International Midwest Symposium on Circuits and Systems* (MWSCAS), pp. 1148–1151, 2013.

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