Experimental Test Bed to De-Risk the Navy Advanced Development Model

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***Abstract*—This paper presents a reduced scale demonstration test-bed at the University of Texas' Center for Electromechanics (UT-CEM) which is well equipped to support the development and assessment of the anticipated Navy Advanced Development Model (ADM). The subscale ADM test bed builds on collaborative power management experiments conducted as part of the Swampworks Program under the US/UK Project Arrangement as well as non-military applications. The system includes the required variety of sources, loads, and controllers as well as an Opal-RT digital simulator. The test bed architecture is described and the range of investigations that can be carried out on it is highlighted; results of preliminary system simulations and some initial tests are also provided. Subscale ADM experiments conducted on the UT-CEM microgrid can be an important step in the realization of a full-voltage, full-power ADM three-zone demonstrator, providing a test-bed for components, subsystems, controls, and the overall performance of the Medium Voltage Direct Current (MVDC) ship architecture.**

Keywords—advanced development model; dc system protection; MVDC; pulsed load; real-time digital simulator; shipboard power system

I. INTRODUCTION

The Electric Ships Office (ESO), in coordination with the Office of Naval Research (ONR), is planning the realization of an ADM to demonstrate feasibility of an MVDC Integrated Power and Energy System (IPES) on future surface combatants [1]. This is a major investment on the part of the US Navy and is beneficial through preliminary steps aimed at de-risking the innovative technology elements of the ADM. This paper presents the reduced-scale demonstration test bed at UT-CEM with a focus on reducing risk for the realization of the full scale ADM. Preliminary simulation and experimental results obtained to date on some crucial issues of interest including fault detection, localization, and isolation, dc bus stability under pulsed loads, and system control strategy are summarized and discussed in the paper.

One function of the reduced-scale demonstration test bed is to test various new dc distribution protection methods to de-risk these technologies in the full-scale ADM. The MVDC ship power system is a power-electronics dominated, isolated, low inertia, and low-line-impedance system [2]. Once a short-circuit fault occurs, the fault current raises extremely fast [3]. The fault current needs to be interrupted rapidly to reduce electrical and thermal stress on power equipment, especially electronic devices on the fault path. The fault path is the set of components between the power source and the fault.

It is expected that the power converters in the dc system may be used to limit the fault current to a low level. In addition, conventional mechanical breakers or disconnectors will be used to isolate the fault. Once the fault current is limited to a constant value, it becomes difficult to discriminate faults. This makes the fault localization and coordination more difficult in the dc system than it would be in an equivalent ac system [4]. For at least these reasons, novel dc distribution protection methods need to be developed and tested for shipboard power systems.

Pulsed loads may introduce sudden load demand changes and the high current rate of change in the MVDC system [5]. These sudden changes may induce high voltage and current transients, which may deteriorate the dc system power quality. Thus, the integration of pulsed loads in the MVDC system needs special consideration for navy ships. Various methods have been proposed to mitigate the impact of pulsed load on the power quality of ship systems including the smooth of charging currents for pulsed loads [5], dynamic load management [6], and the integration of energy storage systems [7]. The integration of a pulsed load in a 2-MW dc microgrid has been successfully demonstrated at UT-CEM. The proposed subscale ADM system can be potentially used to test and demonstrate various solutions for pulsed load integration in future ships.

The outline of this paper is as follows. The proposed subscale ADM test bed at UT-CEM is discussed in section II. In section III, fault detection, localization, and isolation for the subscale ADM system is studied numerically. Some critical design issues are also explored. Section IV presents the initial demonstration results of pulsed load integration in the subscale dc system. The integration plan of a real-time simulator in the hardware dc system is discussed in Section V. The conclusion and future work are presented in Section VI.

II. SUBSCALE ADM TEST BED AT UT-CEM

In support of the ESO/ONR plans for the implementation of an ADM, UT-CEM has configured its existing flexible, megawatt-scale dc microgrid to realize the anticipated demonstration of at least three ship electrical zones, populated

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with representative hardware capable of operating at relevant power levels and under the control of a hierarchical power and energy control system. The objective configuration of the UT dc microgrid test-bed is shown in Fig. 1. The test-bed is currently configured to represent a notional MVDC ship power system with a 1,150 V dc distribution voltage. To reflect realistic ship installations, the various components of the microgrid are distributed among three separate laboratories with approximately 100 m long primary distribution buses connecting them.

It is worth noting that the current installation presented in Fig. 1 not only reproduces exactly the projected architecture of the three-zone demonstrator shown in [1], but also, through real-time emulation implements in actual hardware other critical subsystems identified as probable components on future ships [2], and in particular the following ones:

IPNC	Integrated Power Node Center
PCM	Power Conversion Module
PCM1-A	Power Conversion Module (incorporating an Energy Storage Module)
PGM	Power Generation Module
PMM	Power Propulsion Module

The UT microgrid features a distributed control system with a central supervisory controller interfaced with individual sub-system and component level controllers located in the separate labs. The existing supervisory control system is based on the National Instruments (NI) LabView controls and data acquisition platform and the Power Electronic Building Blocks (PEBB) in the power converter modules were specifically selected for compatibility with this system.

Power for the test-bed can be supplied from the facility's electric distribution grid or from isolated diesel or gas turbine driven generators. In either case, the behavior of a dual-wound generator feeding two separate buses will be emulated with the Opal-RT Multi-purpose Real Time Simulator (MRTS) now operating at UT-CEM. The Opal-RT MRTS can also be used as a key tool in emulating a variety of other sources and loads as a means of vetting different control schemes and several potential concepts of operation for the system.

Thus, the UT-CEM microgrid has all the elements to implement the circuit of the ADM, albeit at the scaled down dc bus voltage of 1.15 kV instead of the planned 12 kV and at the 2 MW power level. Therefore, it can be a useful tool in de-risking components, subsystems, and control concepts prior to implementation in the full scale ADM.

The system, including all major subsystems, has been exercised to verify its functionality. Demonstrations have also been carried out as, for example, firing an electromagnetic railgun, some preliminary assessment of signal latency on system performance, bus stability under various pulsed loads, effect of series faults and their detectability, and a study of the potential destabilizing effects of prescribed power loads.

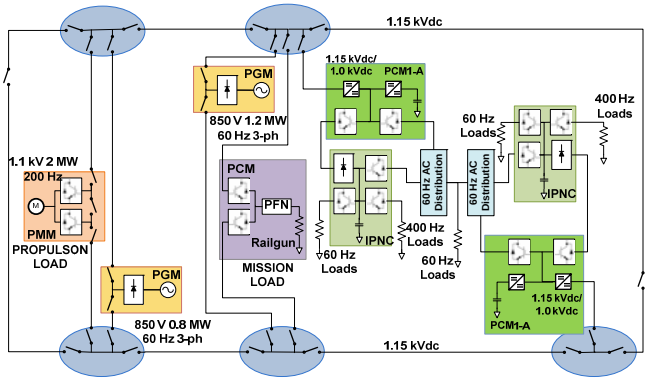


Fig. 1. Configuration of the UT-CEM dc microgrid test-bed.

III. Preliminary Demonstration of Fault Detection, Localization, and Isolation

DC systems challenge conventional protection system design. There is no natural zero crossing in dc currents. Thus, mechanical dc circuit breakers are limited by the fault current interruption capability. Hybrid dc circuit breakers have been developed mainly for HVDC transmission systems [8]. A hybrid dc breaker consists of arrester banks and an additional branch including a solid-state load commutation switch and a fast mechanical disconnector. The additional elements in the hybrid breaker increase its cost and volume, which may be an undesired solution for dc shipboard power systems. Recently, solid-state dc circuit breakers are being developed for medium voltage applications [9]-[13]. This type of dc breaker could quickly interrupt faults in a reliable manner.

In addition to dc fault interruption technologies, various dc fault detection and localization schemes are also extensively studied to achieve fast and reliable fault isolation and system restoration [14]-[18]. MVDC shipboard power system is a type of power electronics dominated system. The fault currents could be potentially limited by power converters such as full bridge Modular Multi-level Converter (MMC), thyristor-based rectifier, and buck converter. Once the fault current is limited to a constant value, the downstream protective devices would immediately lose selectivity, which makes the protection coordination much more challenging. The conventional over-current protection method may not work well in this case. In addition, shipboard power systems supply power to pulsed loads with high current rate of change (di/dt). This may make the current-rate-of-change protection method difficult to be used. The pulsed power systems may produce radiated and conducted signals that interfere with the sensing and control system, which may have negative impacts on the dc fault protection.

In order to address these challenge problems in dc system protection, the UT-CEM research team developed a lab-based dc microgrid to test and demonstrate the feasibility of developed dc fault detection, localization, and isolation methods. The protection methods will be initially tested in a simplified dc system as shown in Fig. 2. More comprehensive tests would be conducted on the full subscale ADM test bed, as shown in Fig. 1, once the research team gains confidence in this preliminary test. The simplified dc system includes two

PGMs, one propulsion load, one mission load, one equivalent dc zonal load, two mechanical dc circuit breakers, and five contactors. In each PGM, a three-phase lab power source is used as a generator to supply power for the system and the ac power is converted to dc power by a diode or thyristor-based rectifier. There is no fault current limiting (FCL) function implemented in the rectifier. A dc-dc buck converter with an output capacitor and a line reactor is adopted to implement the FCL function for each PGM.

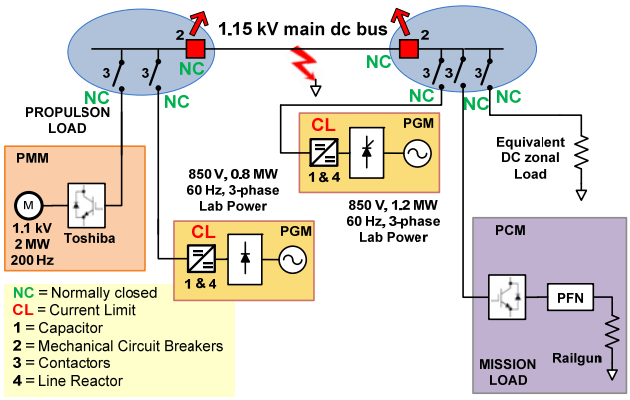


Fig. 2. Diagram of a simplified MVDC system for protection system test.

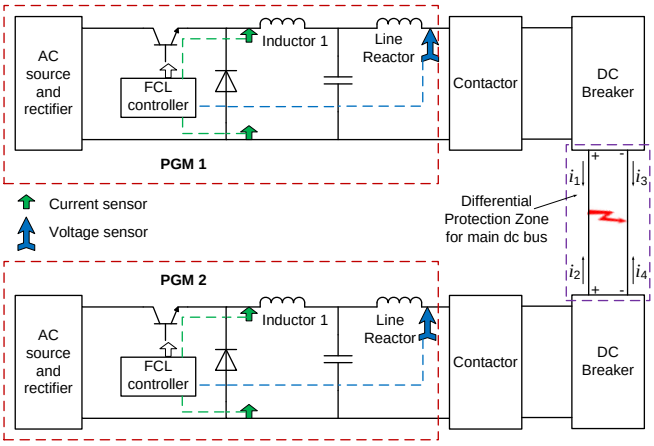


Fig. 3. Diagram of the converter FCL + differentional protection scheme.

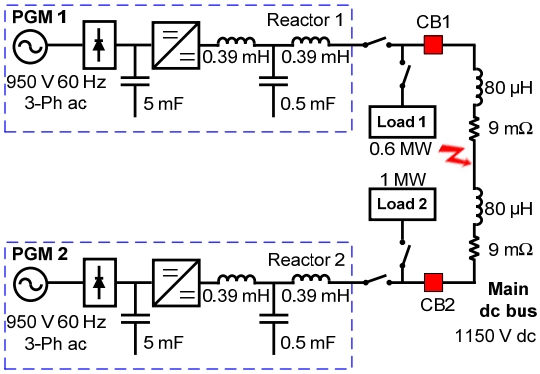


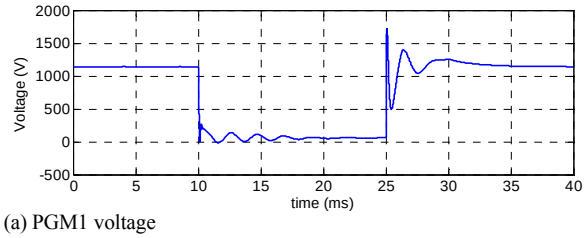
Fig. 4. SLD of the simulated system in Matlab/SIMULINK.

Two mechanical dc circuit breakers with 3.6 kV dc and 2.6 kA ratings are used to isolate faults on the main dc bus. A short-circuit fault is placed on the main dc bus to test the developed dc protection strategies. All the other switches in the circuit are contactors with 4 kV and 0.4 kA ratings. The mission load in the dc system is a railgun powered by a PCM and a pulse forming network (PFN). An induction motor with a dynamometer is driven by a Toshiba variable frequency drive to emulate a ship propulsion load. When a short circuit fault occurs on the main dc bus, each PGM first limits fault current at 150% of the rated current. The mechanical dc breakers are selected by the protection system to isolate the fault. After fault clearance, dc-dc converters in PGMs are restored to supply power to the healthy part of the dc system. Thus, the propulsion load and the mission load are only interrupted for a very short time. The load interruption time depends on the dc fault clearing time.

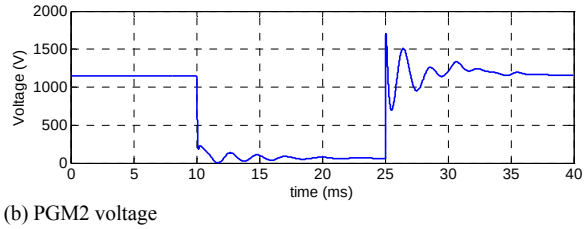
The first protection method to be tested in the dc microgrid is a hybrid protection approach combining the converter fault current limiting and the main dc bus differential protection (converter FCL + differential protection). Once an over-current is detected by the buck converter in a PGM, the buck converter is switched from voltage control mode to current control mode to maintain the output current at 150% of the rated current. This FCL function prevents any damage to the semiconductor devices in PGMs during downstream dc faults. A differential protection zone is designed for the main dc bus as shown in Fig. 3. Two mechanical dc breakers are used to isolate faults on the main dc bus. The differential protection scheme uses the current differential to detect fault on the main dc bus. If the summation of currents on positive pole or negative pole exceeds a predefined threshold, the fault is detected and located and dc breakers are tripped to isolate the fault. Once the fault is isolated, converters are restored to normal condition and continuously supply power for the healthy circuit.

To illustrate the protection scheme and support the experimental tests, numerical simulation study is performed in Matlab/SimPowerSystem. The simulation time step is chosen as 2 μs. The switching frequency of dc-dc converter is chosen as 5 kHz. The single-line-diagram (SLD) of the dc system and the main circuit parameters are shown in Fig. 4. It is assumed that a dc short-circuit fault is placed at the midpoint of the main dc bus. The fault resistance is varied from 1 to 200 mΩ to study the impact of fault resistance on the fault current behavior. The resistance of each breaker or contactor is neglected in the simulation. A line reactor is added at each PGM output terminal to limit the current rate of change.

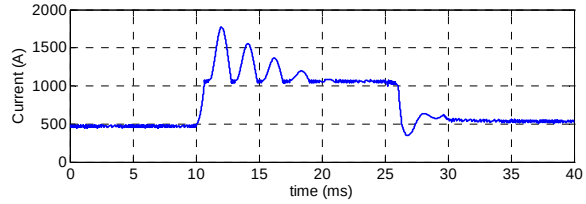
Once a short-circuit fault occurs, the terminal voltage starts dropping due to the capacitor discharge, as shown in Fig. 5 (a) and (b). The initial transient is very fast depending on the fault resistance and line impedance as well as the line reactor inductance. Each PGM monitors its output current right before the output capacitor. If the measured current exceeds the threshold, the buck converter is switched to current control mode by limiting the current at 150% of the rated current, as shown in Fig. 5 (c) and (d). The current oscillations in the next few milliseconds are caused by the natural damping of the RLC circuit. Once the capacitors are fully discharged, the currents reach steady-state.



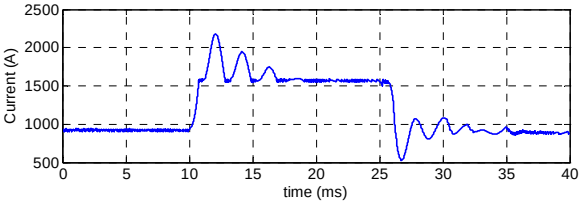
(a) PGM1 voltage



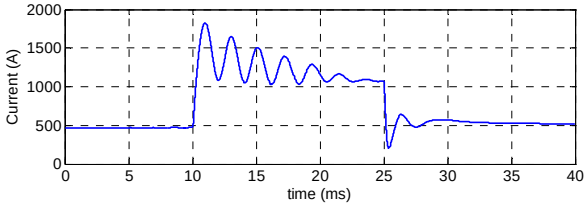
(b) PGM2 voltage



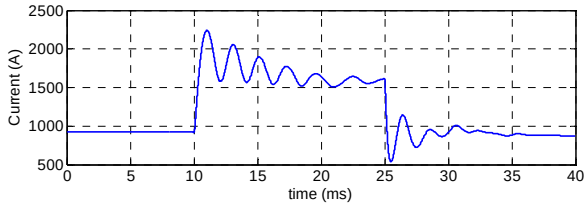
(c) Current flow on inductor 1 of PGM 1



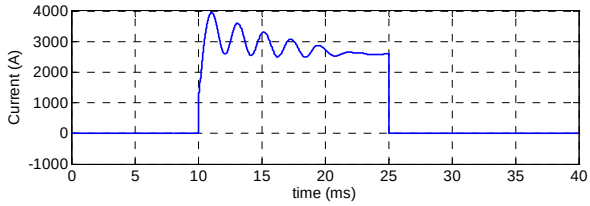
(d) Current flow on inductor 1 of PGM 2



(e) Current flow on the contactor of PGM1



(f) Current flow on the contactor of PGM2



(g) Current differential in the main dc bus protection zone

Fig. 5. Simulation results of the converter FCL + differential protection approach with a fault resistance of 20 mΩ.

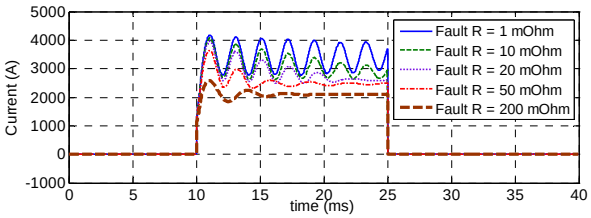


Fig. 6. Current differentials in the main dc bus protection zone with different fault resistances.

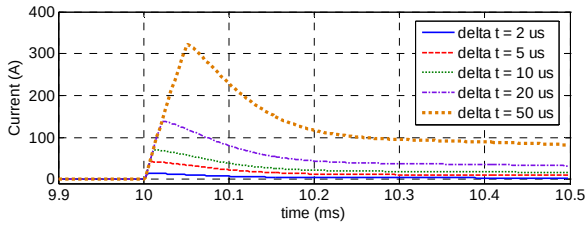


Fig. 7. Current differentials in the main dc bus protection zone with different measurement time differences.

The current differential of the main dc bus protection zone is increased to a high value right after the fault, as shown in Fig. 5 (g). It is assumed that the two dc breakers wait 15 ms to isolate the fault. Once the fault is isolated, the current flow on each converter starts decreasing and the buck converter switches to voltage control mode to maintain the terminal voltage at the rated value, as shown in Fig. 5 (a) and (b). The initial spikes in voltage signals are caused by the discharge of line reactors, and then the system voltage and current converge to steady-state values in a few milliseconds. After the fault is cleared, the dc system operates as two isolated subsystems in split mode.

To study the impact of the fault resistance on fault current behaviors, the fault resistance is varied from 1 to 200 mΩ. When the fault resistance is low at 1 mΩ, the fault current includes significant oscillations and takes a longer time to settle, as shown in Fig. 6. When the fault resistance is 50 mΩ, the fault current reaches steady-state in 10 ms. If the fault resistance is further increased to 200 mΩ, the fault current settles in 5 ms, as shown in Fig. 6.

As suggested in [14], [19], the signal synchronization of current measurements for differential protection is critical under the high *di*/*dt* conditions. In dc shipboard power systems, line impedance is relatively low and the capacitors are distributed system wide. Once a short circuit fault occurs, the *di*/*dt* usually becomes extremely high. In addition, the pulsed load may introduce high *di*/*dt* by its charging circuit. To better understand the performance of the differential protection, a sensitivity analysis is performed to investigate the impact of unsynchronized measurements on the current differential under high *di*/*dt* conditions.

In this study, it is assumed that a short-circuit fault with 20 mΩ resistance is placed at the terminal of PGM 1. It is also assumed that the difference in measurement time between the two current signals is varied from 2 to 50 μs. As the time difference increases, the current differential is increased as shown in Fig. 7. It should be noted that this is an external fault for the differential protection zone. The current differential

should be 0 in an ideal case. However, the unsynchronized current signals introduce a positive value in the current differential which may cause a misoperation of the protection system. Thus, the maximum *di*/*dt* and the maximum difference in measurement time between signals need to be considered in the current threshold design for the differential protection. In the practical design, the current differential threshold for tripping should be well above the maximum error current observed in the worst-case scenario.

In addition to differential protection, other dc distribution protection methods, including impedance protection, over-current protection, and *di*/*dt* protection, will be explored both numerically and experimentally for shipboard power systems.

IV. Preliminary Demonstration Results for Pulsed Load Integration

The UT-CEM research team has successfully integrated a 4-meter long and 54-mm diameter electromagnetic launcher and its 12 MJ capacitor-based pulse forming network into the dc microgrid. The single-line-diagram of this module is shown in Fig. 8. A Semikron 1.67 MVA 3-ph full bridge liquid cooled power inverter module [20] connects the main dc bus of the microgrid and a 3-ph transformer. A 3-ph line reactor was inserted between the inverter and the transformer to smooth the inverter output current. A 3-ph PWM controller was implemented for the Semikron module to invert dc voltage to a 60 Hz 3-ph variable voltage in order to maintain a constant charging current for capacitor banks. This controller manages the capacitor charging power supply (CCPS). The CCPS control algorithm was implemented on an NI single board reconfigurable I/O board (sbRio-9606) and an NI general-purpose inverter controller (GPIC) [21]. The CCPS control platform is shown in Fig. 9. The top board is the sbRio-9606 embedded controller; the GPIC card is in the middle layer; the bottom layer is the custom interface board.

Once a charging command is received from the PFN controller, the CCPS controller initiates the capacitor bank charging process and maintains the charging current at a constant value. Once the capacitor voltage reaches the desired value, the CCPS controller stops the charging process and controls a high-voltage relay to disconnect capacitor banks from the source. The PFN controller is responsible for configuring the capacitor bank network and the capacitor bank discharge sequence required to form the current pulse fed to the Electromagnetic Railgun (EMRG). To mitigate the risk, the CCPS controller was initially developed and implemented on a subscale CCPS network as shown in Fig. 10. After verifying the performance of control algorithm on the subscale system, the control platform was transferred to the full-scale system as shown in Fig. 11.

The CCPS first charged ten capacitor modules to 11 kV dc which was required to fire a test shot. The capacitance of each capacitor module is 4.944 mF. The total energy stored in the capacitor banks was 3 MJ. A test round was then loaded in the EMRG. The ten capacitor modules were recharged and the projectile was successfully launched.

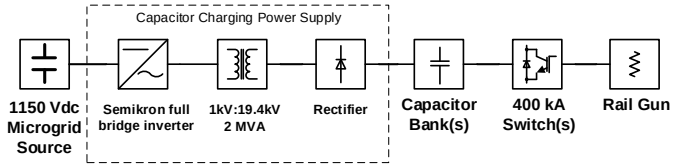


Fig. 8. Diagram of capacitor charging power supply and PFN.

Fig. 9. Capacitor charging power supply control platform.

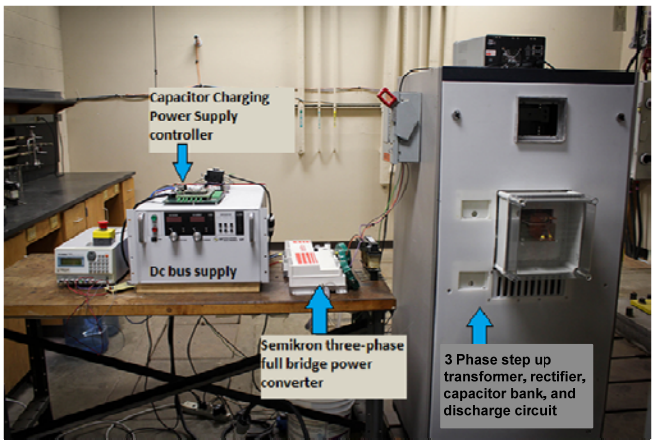


Fig. 10. Subscale CCPS set up with controller, dc bus, and capacitor bank.

Fig. 11. Full-scale CCPS with inverter and three-phase line reactor.

As suggested in Fig. 12, there is a sudden power drop at the end of the charging profile which could significantly perturb the isolated dc microgrid. The charging current profile of CCPS may need to be improved through advanced control of

the power inverter to reduce its impact on the dc system stability. The integration of a hybrid energy storage system may be an alternative solution to address this issue. Future work would include the demonstration of multiple charge and discharge cycles of the pulsed load and the integration of hybrid energy storage to improve the dc microgrid stability.

V. Integration of Real-Time Digital Simulator

The Opal-RT MRTS is integrated in the dc microgrid at UT-CEM to perform power hardware-in-the loop (PHIL) simulation. The digital simulator has the capability to emulate a variety of sources and loads as well as power converters. The power amplifiers and analog/digital I/Os are used as an interface between the digital simulator and the hardware dc microgrid. The digital simulator at UT-CEM includes Opal-RT OP5600 and the NI PXI FPGA system. OP5600 can simulate a 900 node system with a 50 µs time step (electromagnetic transient simulation). The NI PXI FPGA system is a dedicated simulator to simulate fast power electronic switching behavior with a 500 ns time step. Two eHSx64 solvers can simulate 144 switching devices for power converters. The two simulators are connected by a high-speed communication link to execute a co-simulation.

As an initial step, a megawatt-scale generation unit would be emulated using the Opal-RT MRTS platform as shown in Fig. 13. The Opal-RT OP5600 simulator would be used to simulate the generator electromagnetic transients, engine thermal dynamics, electromechanical dynamics, and accessory loads. The power conversion system would be implemented in the NI PXI FPGA simulator. The two simulators would exchange information every 50 µs to execute a co-simulation for a PGM model. The behavior of a dual-wound generator feeding two separate buses could also be simulated in this set up with some modification.

In addition to the generation system emulation, the Opal-RT MRTS platform will be used to emulate a PCM1-A in the subscale ADM at UT-CEM, as shown in Fig. 14. The power converters as well as the associated energy storage system are simulated in the Opal-RT MRTS platform. Power amplifiers are designed to interface the simulated PCM1-A with the hardware dc microgrid. The experimental test data would also be used to improve the model fidelity in the digital simulator.

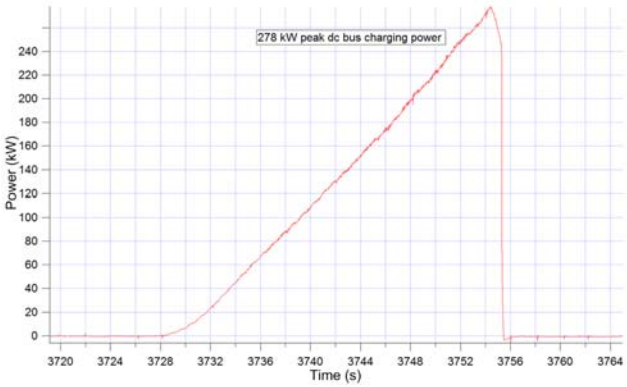


Fig. 12. Full-scale CCPS input power to charge capacitor banks.

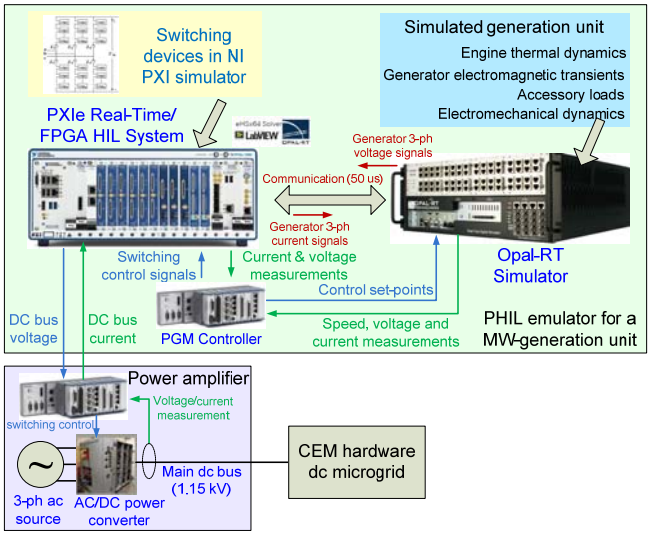


Fig. 13. Diagram of a PHIL emulator for a generation unit.

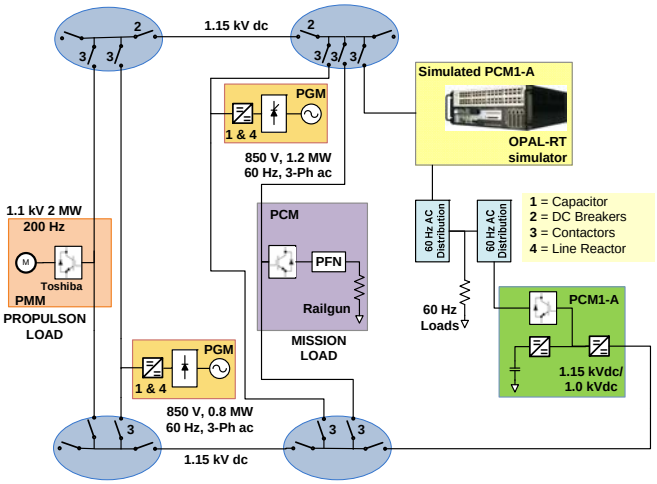


Fig. 14. Diagram of a PHIL emulator for a PCM1-A.

VI. Conclusion and Future Work

This paper presented a reduced scale demonstration test-bed at the UT-CEM in support of the anticipated Navy ADM. The existing flexible, megawatt-scale dc microgrid is being configured to realize the anticipated demonstration of at least three ship electrical zones. The preliminary demonstration results show the successful integration of a pulsed load (EMRG) in the dc microgrid. The preliminary fault detection, localization, and isolation studies for a simplified dc microgrid have been performed in a numerical environment. A hybrid dc protection approach combining converter FCL and differential protection was illustrated in numerical simulation. The results support hardware dc short circuit fault tests in the subscale ADM. In addition, the PHIL simulation using the Opal-RT MRTS platform was introduced to emulate a variety of sources and power converters to argument the capability of the subscale ADM system.

Future work includes the integration of the Opal-RT MRTS platform and the hardware test for the dc fault detection, localization, and isolation methods in the subscale ADM at

UT-CEM. The demonstration of multiple charge and discharge cycles of the pulsed load and the integration of hybrid energy storage in the dc microgrid may also be conducted.

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