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LOW POWER VCO-BASED ANALOG-TO-DIGITAL CONVERSION

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LOW POWER VCO-BASED ANALOG-TO-DIGITAL CONVERSION

by

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This thesis is dedicated to my parents for their love, endless support and encouragement.

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Low Power VCO-Based Analog-To-Digital Conversion

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Co-Supervisor: Arjang Hassibi

This dissertation presents novel two stage ADC architecture with a VCO based second stage. With the scaling of the supply voltages in modern CMOS process it is difficult to design high gain operational amplifiers needed for traditional voltage domain two-stage analog to digital converters. However time resolution continues to improve with the advancement in CMOS technology making VCO-based ADC more attractive. The nonlinearity in voltage-to-frequency transfer function is the biggest challenge in design of VCO based ADC. The hybrid approach used in this work uses a voltage domain first stage to determine the most significant bits and uses a VCO based second stage to quantize the small residue obtained from first stage. The architecture relaxes the gain requirement on the the first stage opamp and also relaxes the linearity requirements on the second stage VCO. The prototype ADC built in 65nm CMOS process achieves 63.7dB SNDR in 10MHz bandwidth while only consuming 1.1mW of power. The performance of the prototype chip is comparable to the state-of-art in terms of figure-of-merit but this new architecture uses significantly less circuit area.

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Chapter 1 Introduction

Scaling of the CMOS technology in last few decades has encouraged time-domain analog to digital conversion techniques. The scaling leads to lower supply voltages which lead to smaller signal swings and lower signal to noise ratio. The transistors in advanced CMOS nodes also typically have lower output impedance making it difficult to design high gain opamps. One of the benefits of scaling is that the f_T of the transistors keeps increasing as the technology scales. This leads to improved time resolution and benefits ADC architectures which rely on time domain processing for analog to digital conversion. In this chapter we will look at trends in the technology scaling and improvement in time resolution. We also look at some time-based ADC architectures which benefit from technology scaling.

1.1 Technology trends

Figure 1.1 (a) shows projections from International technology roadmap for the semiconductors (ITRS) [1] for the supply voltage as the gate lengths are scaled. The supply voltage is expected to drop as low as 0.57V for gate lengths of 5.9nm. The reduction in supply voltage will make design of traditional voltage domain ADCs challenging. In contrast Figure 1.1(b) shows that the stage delay of a ring oscillator is expected to continue improving with each technology node reaching sub-ps levels for most advanced nodes. This means that ADC architectures relying on time-domain processing will benefit from scaling and can be operated at higher speeds. Since time domain ADC's are mostly digital circuits the power consumption in these ADC's should also reduce with the reduction in the supply voltage.

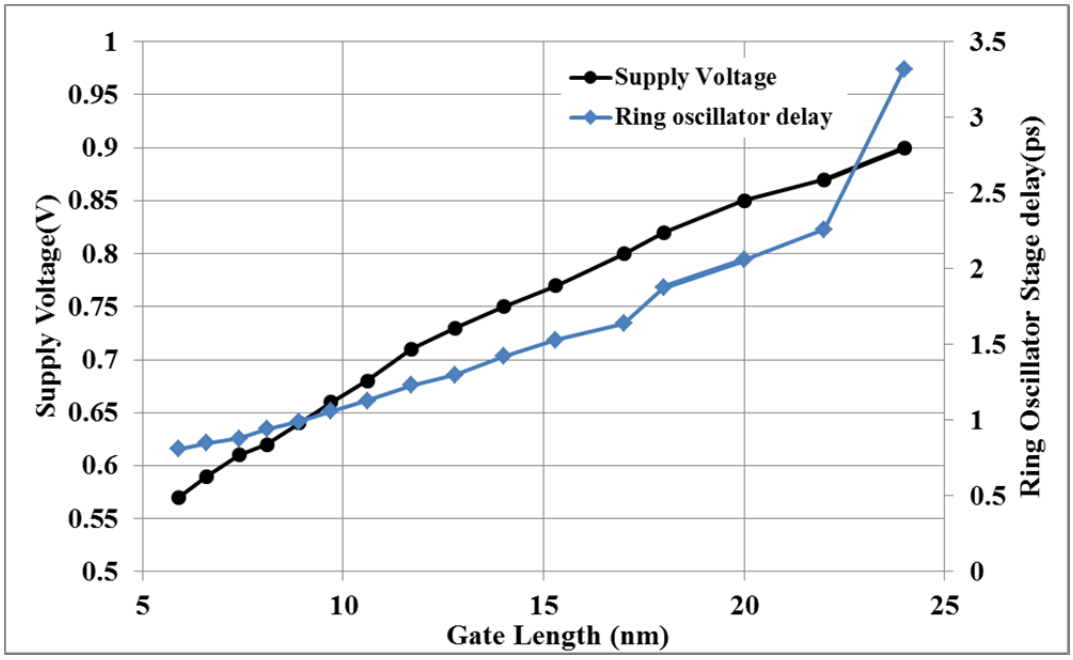


Figure 1.1 Technology trends

1.2 Voltage domain ADC

Figure 1.2 illustrates the challenge in conventional voltage domain analog to digital conversion using a 3 –bit flash ADC [2]. In this design the comparator compares the analog input V_{in} to a different reference voltages. As the supply voltage reduces the LSB (least significant bit) size on the ADC reduces. This makes the design of comparator difficult as it must have smaller offset and noise. Traditional techniques like pipelining also becomes challenging because of the need for high gain opamps which are difficult to realize in advanced CMOS nodes.

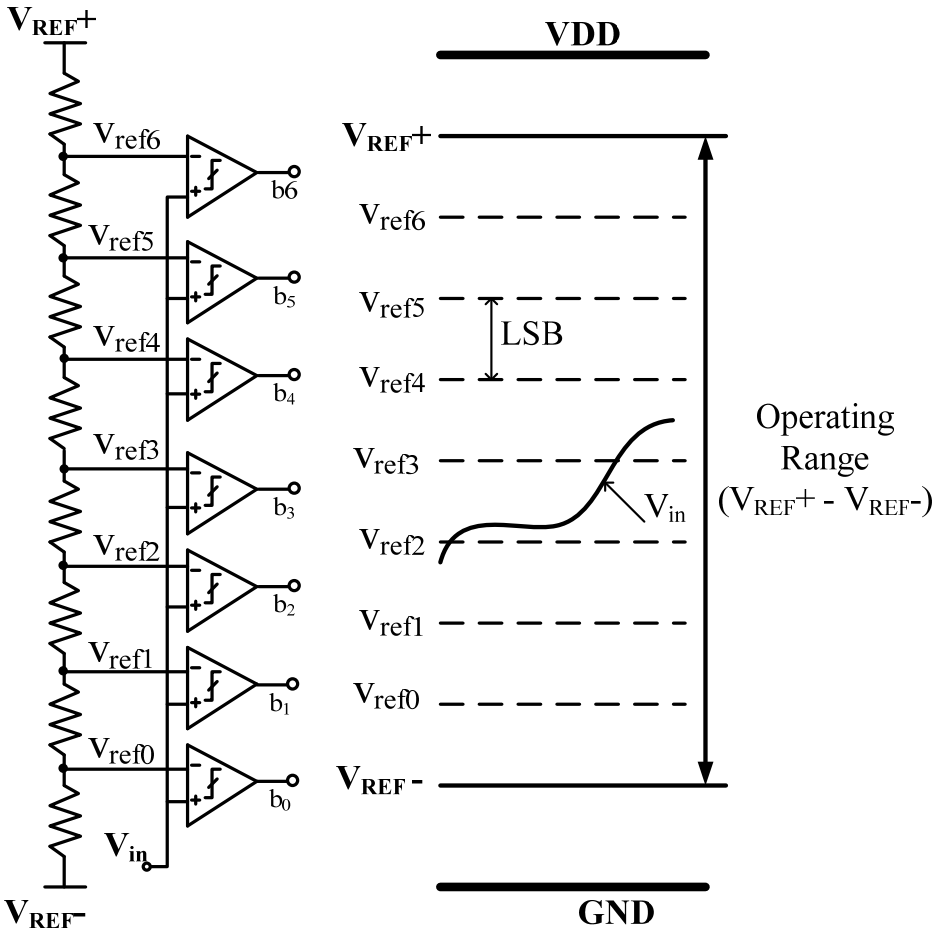
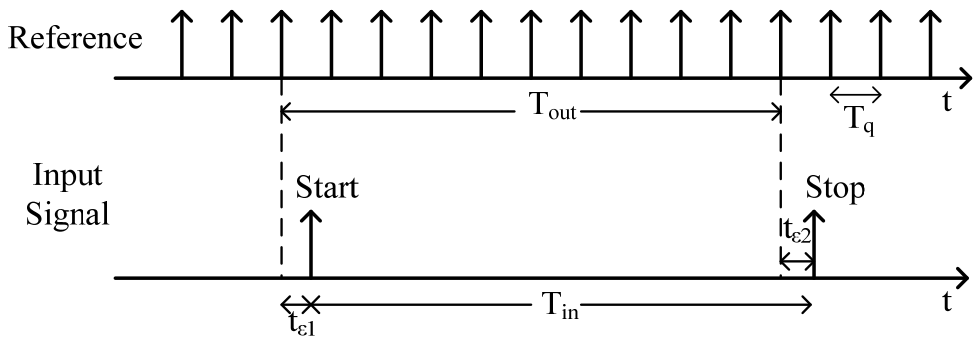


Figure 1.2 Voltage domain Flash ADC

1.3 Time to digital converters (TDC)

Figure 1.3(a) shows the concept of time to digital converters. The aim is to measure the time interval (T_{in}) between two events indicated by signals "Start" and "Stop". The time-resolution is limited by the reference time interval (T_q). If the time interval is quantized by counting the reference edges between "Start" and "Stop" it can be seen that the TDC output is given by

$$T_{out}(k) = T_{in}(k) + t_{\varepsilon 1} - t_{\varepsilon 2} \qquad (1)$$



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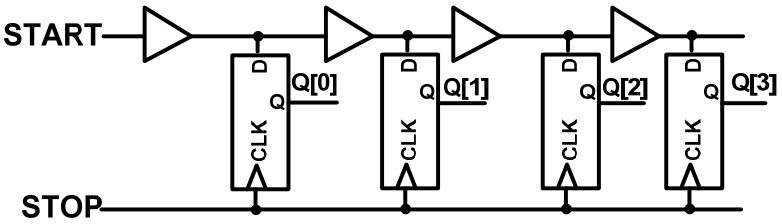
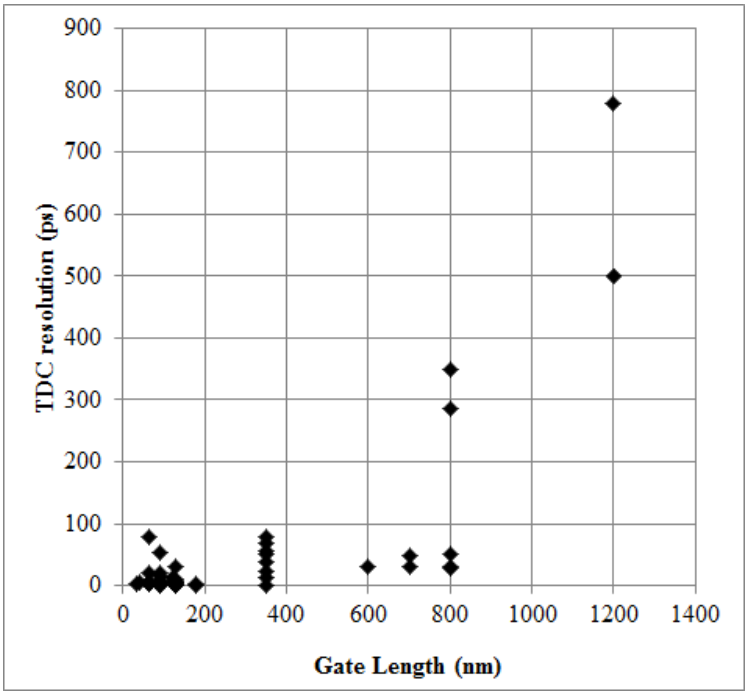


Figure 1.3 TDC (a) Concept (b) Delay line based TDC

The raw TDC resolution is determined by the period of the reference signal. The simplest form of TDC is a digital counter. However, to achieve a high resolution TDC, one needs to use a very high frequency counter for a wide dynamic range. The resolution of counter-based TDCs can be improved significantly by resolving the counter residual error with a high resolution fine TDC based on gate delay [3]. Figure 1.4 shows a typical implementation of a delay line based time to digital converter. Since the resolution for TDC in Figure 1.4 is limited by the inverter delay it will improve with the improved device f_T.



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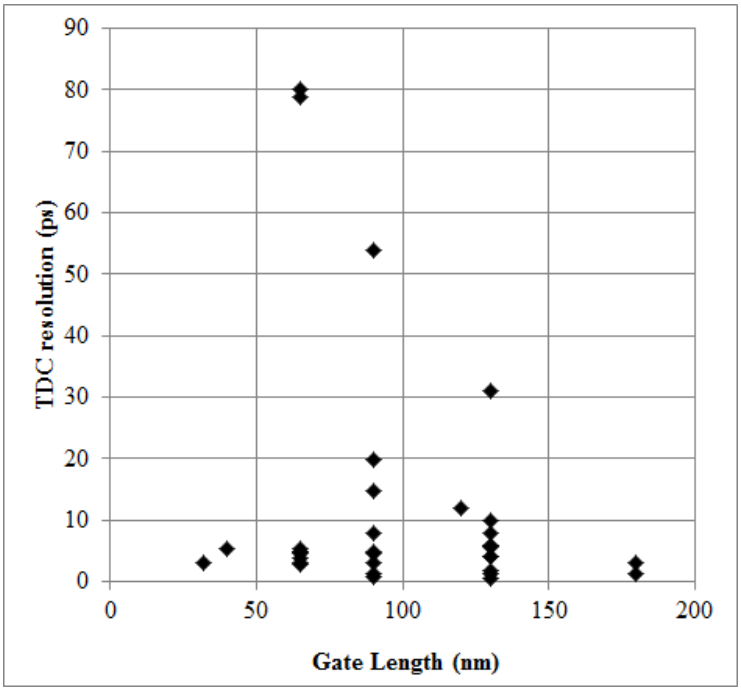


(b)

Figure 1.4: TDC resolution (a) survey (b) 180nm or lower technologies

A literature survey [4- 54] on the reported resolution of time to digital converters in last two decades shows (Figure 1.4a) that the TDC resolution has improved dramatically as technology has advanced to sub -100nm range. Figure 1.4(b) focuses only on technologies 180nm and lower. A vast majority of TDC's in this plot have a resolution of 20ps or lower. A resolution of 0.63ps has been reported in [44]. This is in effect equivalent to having a virtual clock [55] of greater than 1THz. Since the ring oscillator stage delay is projected to keep reducing further, we can expect that TDC resolution will improve further as technology scales.

1.4 Time Based ADC architectures

In this section we look at some time based ADC architectures which benefit from improved time resolution offered by advanced CMOS nodes.

1.4.1 Voltage-time-digital scheme

In the voltage to time conversion scheme illustrated in Figure 1.5 the input voltage is converted into a time window T_{in} which is digitized using a time-to-digital converter. In a simple implementation TDC may be replaced with a counter. Integrating ADC or slope based ADC discussed in next chapter are based on this concept. They typically use counters to quantize the time window which limits their speed. Recently some high speed slope based ADC's have been reported which use advanced time-to-digital converters [55, 56].

Another example of voltage-time-digital scheme is pulse position modulation (PPM) ADC [57] illustrated in Figure 1.6(a). The input signal is continuously compared with

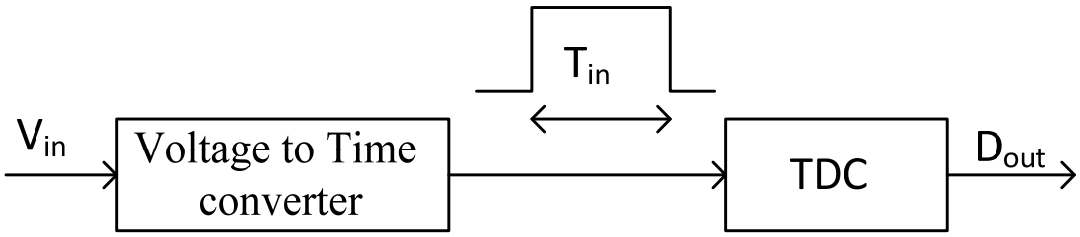


Figure 1.5 Voltage–to-time to digital scheme

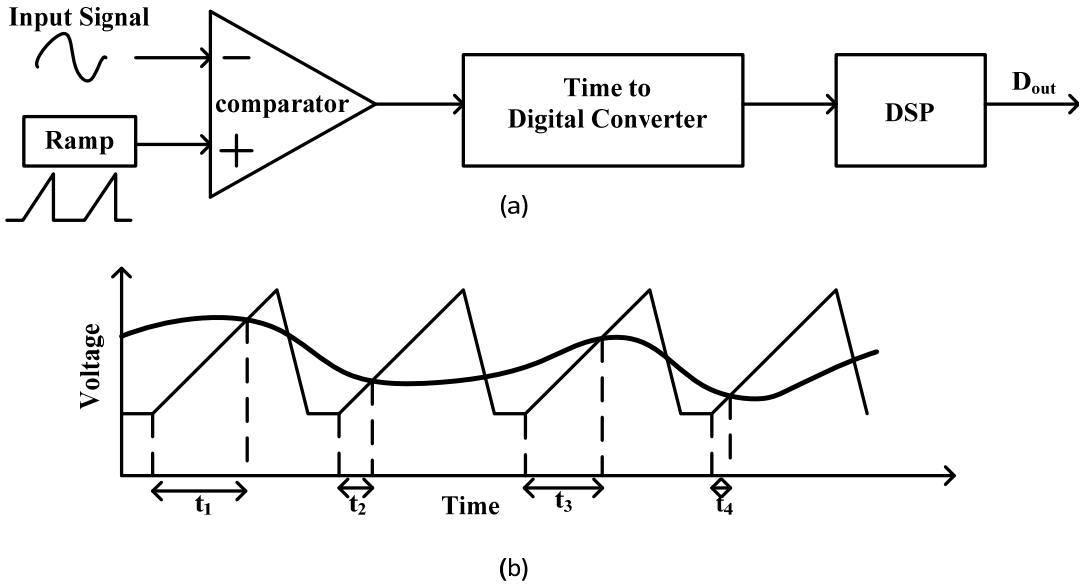


Figure 1.6 PPM ADC (a) block diagram (b) typical waveforms

a voltage ramp. When the input signal and the ramp intersect, the comparator generates a pulse. The time interval between the start of the ramp and the instant the input signal crosses the ramp (i.e [t_1,t_2,t_3,t_4 ..]) in Figure 1.6(b) is measured by a time-to-digital converter. Assuming the ramp slope is constant, the time vector is proportional to the signal amplitude at the crossover points. In a PPM ADC measuring the time vector leads to nonuniform sampling of the input signal. This leads to

distortion if the samples are treated as uniformly sampled. Low-pass filtering is a straightforward linear technique for constructing uniform samples from non-uniform sample information (Fig. 3). Generally an over- sampling ratio of 8 or higher is required. Another approach is to apply a time-varying, nonlinear recovery technique [57] which allows sampling the signal at a frequency close to the Nyquist rate.

1.4.2 Voltage-delay-digital scheme

In the voltage to delay to digital scheme [58, 59] illustrated in Figure 1.7 the input signal V_{in} modulates the delay (t_d) per buffer instead of the time window as in Figure 1.5. The number of delay cells the signal passes through in a constant time window (T_s) is proportional to the input voltage. A major benefit of this type of structure lies in its all digital implementation. This makes it compatible with technology scaling. The ADC with this scheme has a built-in first-order antialiasing sinc filter with nulls at ($1/T_s$). This is similar to the integrating ADC where the input is integrated for time window T_s. The biggest drawback of the approach is the nonlinearity in the voltage to delay transfer function.

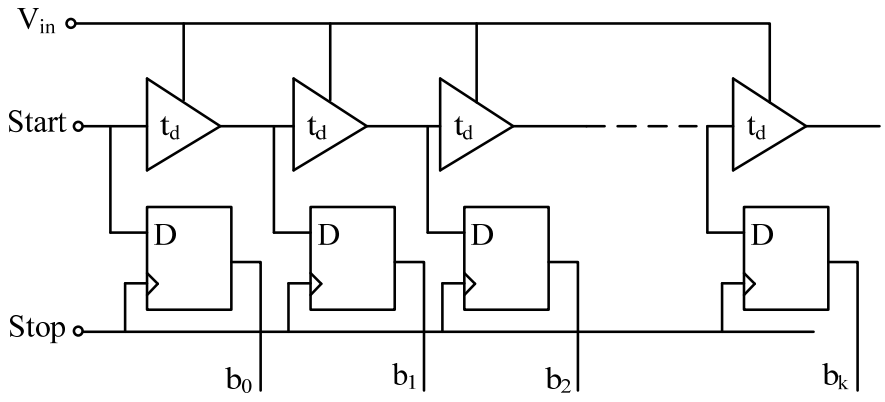


Figure 1.7 Voltage-delay-digital scheme

1.4.3 Voltage-frequency-digital scheme

In a voltage-to-frequency-conversion based ADC architecture, the input signal is converted to frequency (or phase) and then quantized by a frequency (phase) quantizer. Typically, this time-based ADC uses a voltage-controlled oscillator (VCO) as a voltage- to-frequency converter where the frequency is controlled by the analog input voltage. Figure 1.8 shows the block diagram of a VCO based ADC [60, 61] using a multiphase ring oscillator. The output of the VCO is fed to a phase quantizer whose digital output corresponds to the analog input signal. The phase quantizer can be implemented using counters which detects the rising and falling edges of the VCO output, thereby quantizing the output phase by π/N. The output of the counter is sampled at rate of F_s which is the ADC output data rate. The calibration block compares the the count obtained with a reference count to generate the digital code. The resolution of the VCO based is given by

$$Resolution = log_2\left(\frac{f_{max}}{F_s} - \frac{f_{min}}{F_s}\right) + log_2(2N) \qquad (2)$$

where f_{max} and f_{min} are maximum and minimum oscillation frequencies.

Since the counter is reset every clock period the architecture in Figure 1.8 doesn't provide any noise shaping. It is suitable for design of nyquist rate ADC which is the focus of this work. If the counter is not reset it can be shown that VCO based quantizer can provide first order noise shaping when used as an oversampled data converter [62-69]. One of the biggest challenge with the VCO based ADC is the nonlinearity in the voltage-to-frequency transfer function.

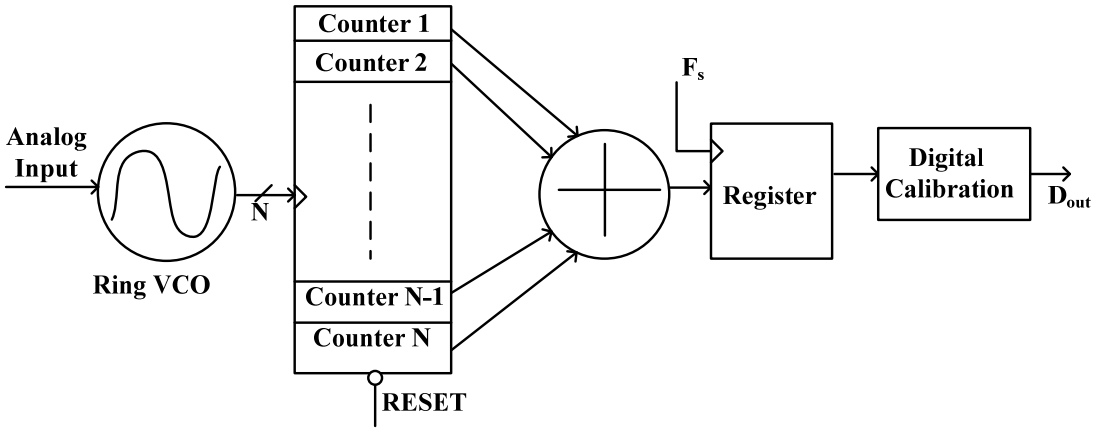


Figure 1.8 VCO based ADC architecture

This problem has been addressed [62-64] and a solution is to embed the VCO based quantizer in a delta sigma loop. The work in [65-66] uses digital calibration to improve the linearity performance of an open loop VCO based ADC. The work in [67] uses a dithering technique to linearize the VCO by randomizing the VCO input.

1.5 Research Contribution

Here we present the design of a two stage ADC using VCO based ADC as the second stage. Prior VCO based ADCs achieve high dynamic range using oversampling. They typically clock the circuit at very high frequencies (>=600MHz) leading to high power consumption. This is the first work on open loop VCO based Nyquist rate ADC. The design uses a hybrid voltage-time approach to get a power efficient ADC. The first stage is optimized using the fact that VCO based ADC is very good at quantizing small residue. The reference refreshing scheme is used for the first time in digital domain in this work. The design achieves lower power compared

to a traditional two step voltage ADC's by using a simple telescopic opamp in the first stage. The figure of merit (FOM) of 44fJ/conversion step is best among the VCO based ADCs. The design solves the VCO nonlinearity problem in a innovative way by making the VCO as a backend of two stage ADC design. We also present a design of a novel differential VCO in this work which achieves 9 bit linearity. The VCO based backend in this design is very digital intensive and occupies only $0.02mm^2$. The architecture is well suited for advanced CMOS technology nodes and the performance will continue to improve in the years ahead.

Chapter 2: Dual Slope ADC based on VCO

Dual slope ADCs were traditionally used for highly accurate measurements [69]. The speed limitations of the architecture limited its use to low speed conversions. With the advancements in the CMOS processes time resolution is improving making this architecture viable again [55, 56, and 70]. In this chapter we have a brief look at the traditional dual slope integrating ADC, followed by an implementation of such an ADC using VCO as an integrator. Next we look at potential application for such an ADC.

2.1 Traditional Dual slope ADC

The block diagram of a typical dual slope ADC is shown in Figure 2.1. It consists of an integrator, comparator, counter, logic and switches. The algorithm starts with the integrator in its reset state. This is achieved by shorting the integrating capacitor. The counter is reset and then switch is connected to analog input. The integrator generates a negative ramp whose slope is proportional to analog input. The comparator goes high and the counter is pulsed by external clock input. When the counter overflows, it resets to zero and the control circuit switches the integrator input to a negative reference voltage. This causes the integrator to generate a ramp with positive slope. When this ramp reaches zero, the comparator goes low and stops the counter. The counter output represents the digital equivalent of analog input.

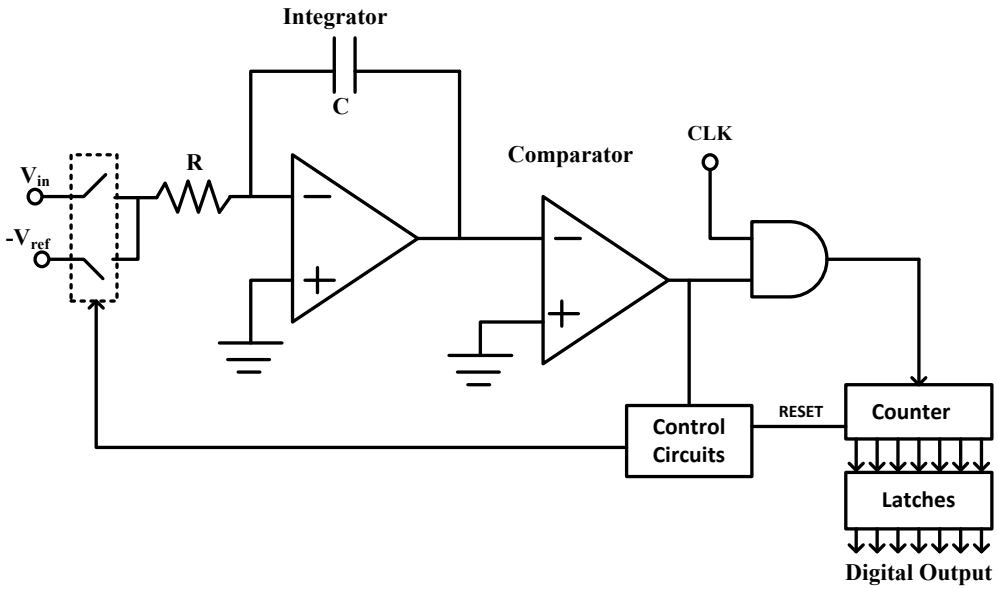


Figure 2.1: Dual slope ADC architecture

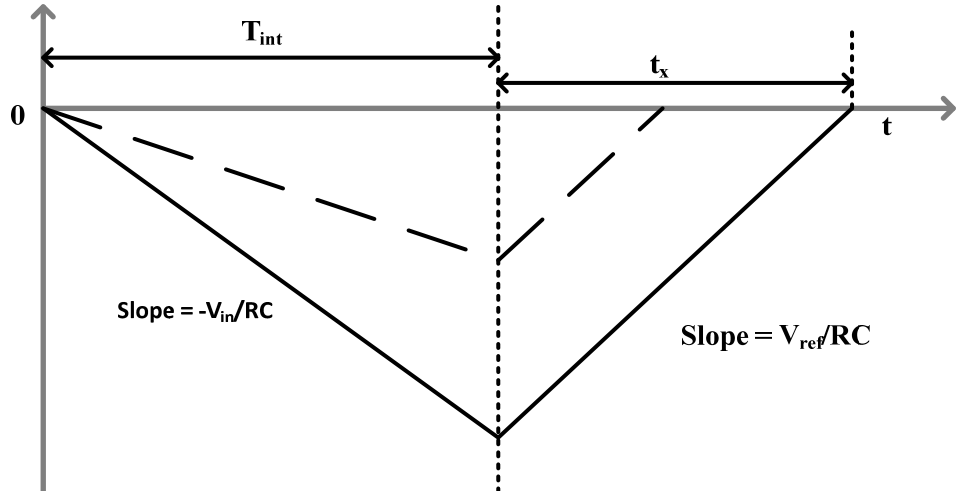


Figure 2.2 Dual slope ADC timing

Figure 2.2 illustrates the integrator output waveform for two different levels of analog inputs. The input integration time is T_{int} and the ramp down time is t_x. It is easy to see that $t_x = V_{in}/V_{ref} * T_{int}$. If T_{int} is chosen to be 2^N clock periods then output code is $2^N * V_{in}/V_{ref}$.

One of the key advantages of dual slope ADC is the inherent antialiasing provided by the input integrator. The signal transfer function for such an ADC is a sinc function with nulls at multiples of the sampling frequency $f_s = 1/T_s$ as illustrated in Figure 2.3. One of the key disadvantages of such a design is that to achieve N bits of resolution 2^N clock cycles are required (assuming counting on both edges). Thus this requires clock frequency to be $2^N f_s$ implying an oversampling ratio of 2^N.

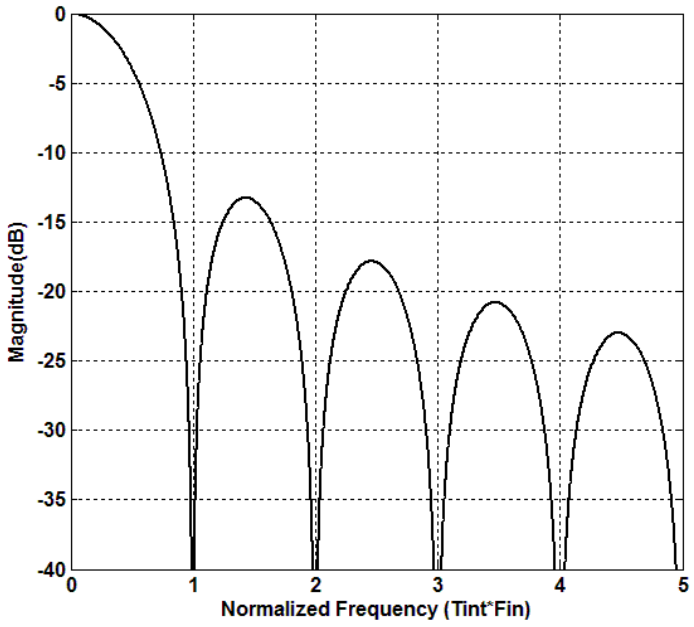


Figure 2.3 Signal transfer function of a dual slope ADC

The improvement in SQNR obtained by doubling the sampling clock is only 6dB per octave. The counter in Figure 3.1 can be replaced with a combination of counter and TDC (time-to-digital converter). In advance CMOS nodes with the improved time resolution it is feasible to build medium speed ADC with the slope based approach [55, 56]. With a 25ps time resolution one can build a 12 bit, 10Msps ADC. The latest TDC's have an LSB resolution of as low as 0.63ps [44] and as technology scales further it will continue to improve making this dual slope ADC approach viable. The bigger challenge is the design of a precise integrator which needs an opamp with high DC gain which is not easily achievable in short channel technologies. Also the comparator noise and offset can limit the performance of the ADC. The metastability in the comparator will limit the maximum speed of the ADC. In the next section we discuss the design of a dual slope ADC using a voltage controlled oscillator as an integrator. The analog comparator in this case is replaced by a digital subtractor simplifying the design.

2.2 VCO based dual slope integrating ADC

The VCO ADC is conceptually based on dual slope integration principle shown in Figure 2.4. In a VCO-based scheme illustrated in Figure 2.4(a), the integration is provided by the combination of VCO and the counter. In first phase, the input is applied to the VCO for 2^N clock periods (T_c). The VCO phase is counted by incrementing a counter for each transition of the VCO output. In the second phase a reference is connected to VCO input and the counter until it decrements to zero.

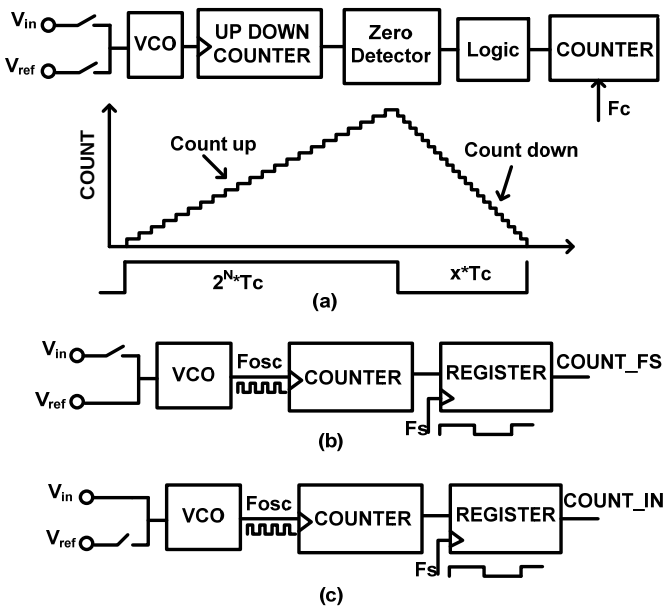


Figure 2.4 (a) VCO based dual slope ADC (b) calibration phase (c) Normal operation

Similar to traditional dual slope a counter is incremented at rate F_c during the countdown phase and is stopped as soon as zero crossing is detected. The value in the output Counter is digital equivalent of analog input. Since the integrator output is digital, in this scheme the ramp down phase can be eliminated and replaced by a calibration step which can be repeated as often as needed. During the calibration step shown in Figure 2.4b the input to the VCO is connected to a reference voltage V_{ref} for half the sampling period $T_s/2$ and the counter output is stored as COUNT_FS. During the normal operation shown in Fig 2.4c the input is connected to the VCO for same period of time $T_s/2$. If the count at the ending of integration period is COUNT_IN

$$DOUT = \frac{COUNT\_IN}{COUNT\_FS} * 2\text{^}N \tag{1}$$

The full-scale count needs to greater than 2^N for the ADC to have N bits resolution.

The benefits of VCO based integration compared to traditional dual slope are as follows

1. Opamp is not required: Since the integration is realized using the VCO and Counter the opamp is eliminated from the design.
2. Analog Comparator is not required: The comparator is replaced by a digital subtraction. The analog comparator limits the performance of the ADC because of noise. The comparator also limits the speed of the design because of metastability issues. By eliminating the analog comparator faster operating speeds can be obtained which is limited only by TDC resolution.
3. A high frequency external clock is not required. With a VCO based design as shown in Figure 2.4 only a Nyquist rate clock (Fs) is required. The high speed external clock F_c in the traditional dual slope design is eliminated. This simplifies the system design and can potentially reduce power in i/o buffers. The design in effect is a Nyquist rate design with built in antialias filter.

The biggest disadvantage of a VCO based design is the nonlinearity in the voltage-to-frequency transfer function. The non-linearity can be greatly reduced by doing a fully differential design. Also the linearity can be improved by reducing the maximum frequency deviation Δf with respect to the oscillation frequency (f_c) [71]. This implies that the input signal swing to the VCO must be reduced. In the real world a vast majority of signals from sensors and transducers are small in magnitude. A VCO based design can be ideally suited for such a system. In the next section we look at an application example for a VCO based dual slope ADC.

2.3 An application example

Recently there have been some publications [72, 73] reporting low power VCO based ADC for biopotential measurements. Figure 4.5 shows the voltage and frequency ranges for three common biopotential signals electrocardiogram (ECG), electroencephalogram (EEG) and electromyogram (EMG) [74]. All these biopotential signals are very small in magnitude with ECG and EEG being bandwidth limited to 150Hz.

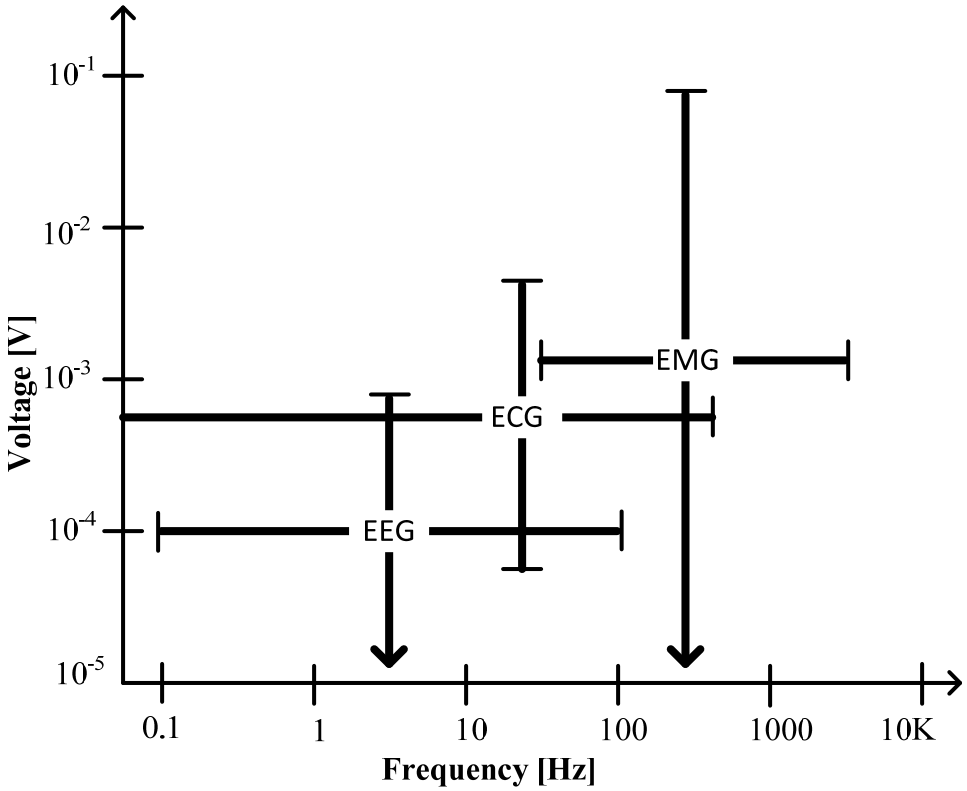


Figure 2.5 Voltage and frequency range for common biopotential signals

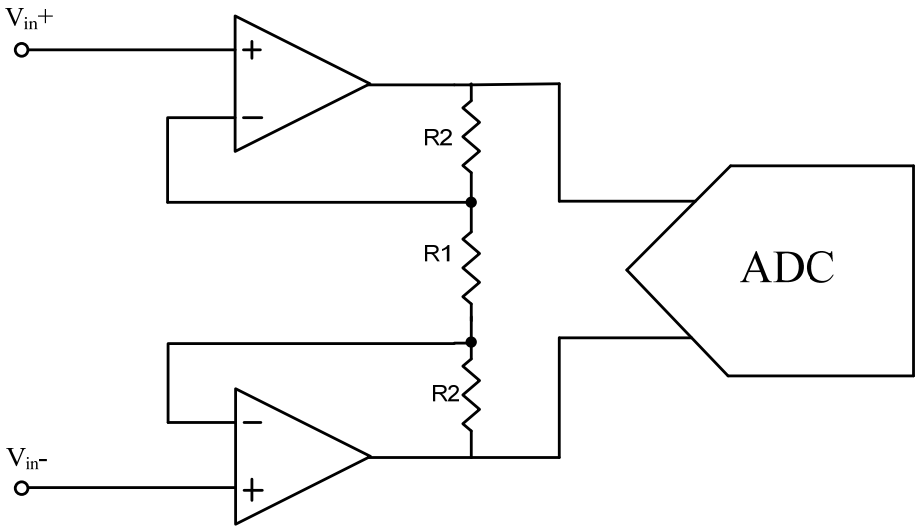


Figure 2.6 A typical front-end for biopotential amplifiers

Figure 2.6 shows a typical acquisition system for such a biopotential amplifier [74] with an instrumentation amplifier amplifying the signal to the full-scale range of the ADC. The instrumentation amplifiers are needed because traditional voltage domain ADC's are not very efficient at quantizing small signals (<10mV). The VCO based ADC's are ideally suited for processing small signals with very high accuracy [72]. The dynamic range can be increased by just increasing the depth of the counter or using multiple phases of a ring based oscillator. Since these biopotential signals are very small the VCO operates in the linear region and the non-linearity in voltage-to-frequency transfer function is not a very big challenge. The work in [73] reports a VCO based ADC for biopotential measurement with only 379nW of power consumption.

The noise in the reported works on VCO based ADC for biopotential measurement remains quite high. One of the challenges in the design biopotential

amplifiers is the 1/f noise because of the low frequency nature of the signals [75]. Though it has not been reported yet traditional techniques like chopper stabilization can be used to eliminate 1/f noise. Figure 2.7 illustrates a conceptual chopper stabilized VCO based ADC for biopotential measurements. The VCO based approach had potential of achieving very low noise levels (< 1μVpp) with much lower power than traditional approach in Figure 2.6.

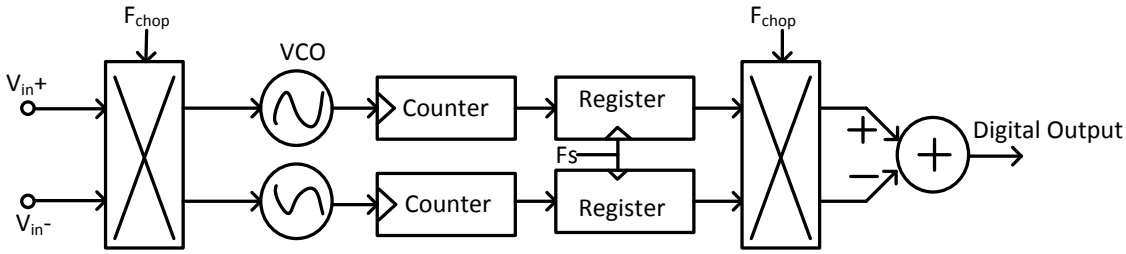


Figure 2.7 Chopper stabilized VCO based ADC

Chapter 3 Power reduction Techniques in Pipelined ADC's

In this chapter we look at various techniques being used in the design of pipelined ADC to reduce its power consumption. We use some of the same techniques in the design of Hybrid voltage-time domain ADC described in next chapter. In the last section we provide the comparison table of ADC's implemented using various techniques described in this chapter.

3.1 Front-end Sample and Hold Amplifier (SHA) removal

Figure 3.1 shows the block diagram of a conventional pipelined ADC with a sample and hold amplifier (SHA) at the front of the pipeline ADC. The purpose of SHA is to provide a constant voltage to the first stage of the pipelined ADC. SHA is not essential to functioning of a pipelined ADC. Typically SHA doesn't provide any gain and consumes almost as much power as the first stage MDAC amplifier. They also contribute significant noise and distortion to the ADC.

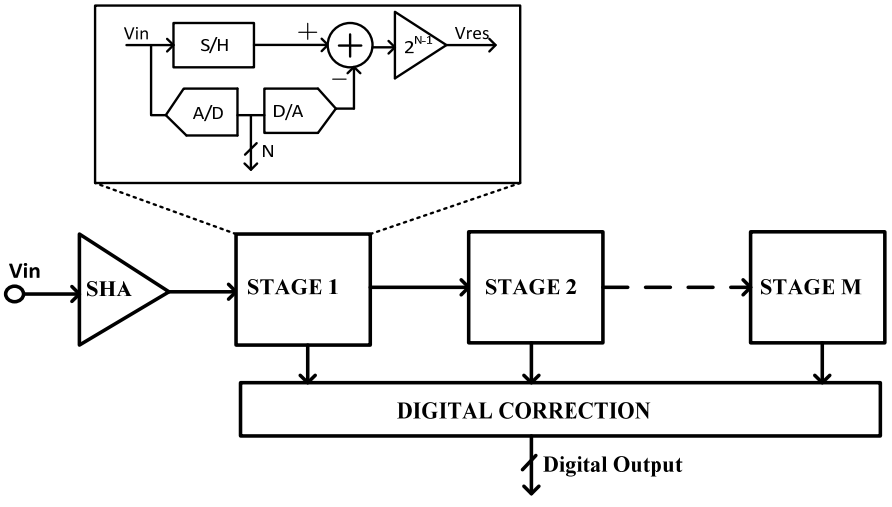


Fig 3.1 Block diagram of a conventional pipelined ADC

There can be significant power savings if the SHA can be removed [76]. The removal of SHA moves the burden of sampling the high frequency input to the first stage of the ADC. The first stage samples the input in the S/H built into the MDAC and the sub-ADC. The sampling in two paths leads to the errors because of clock skew and bandwidth mismatch in two paths as described below.

Sampling Clock skew: The sampling clock skew problem is illustrated in Figure 3.2 Let's assume that the sampling instant for the first-stage S/H and sub-ADC are skewed by Δt. This leads to difference in voltage ΔV (called aperture error) sampled by the two paths. For a sine wave input $V_{in} = V_{ref}\sin(2\pi F_{in}t)$ it can be shown that

$$\Delta V = 2\pi * V_{ref} * F_{in} * \Delta t \quad (1)$$

The problem is more severe for the high frequency inputs and is worst near the zero crossings where the slope of the waveform is largest.

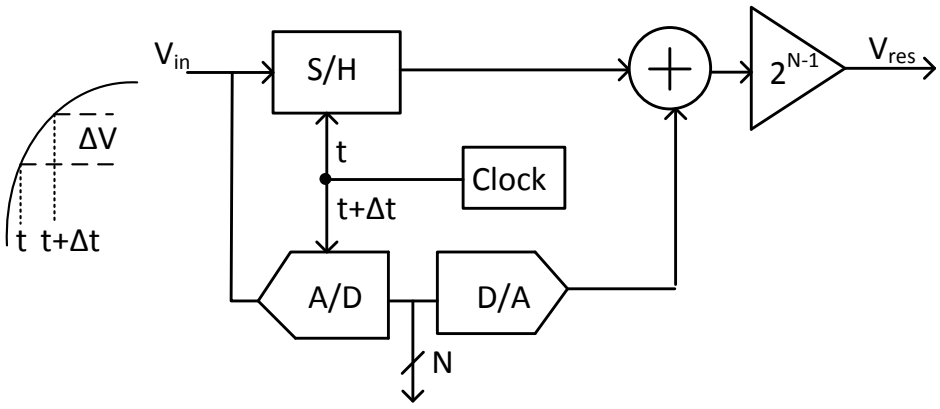


Figure 3.2 Sampling clock skew problem

This sampling clock skew effectively creates a large dynamic offset in the sub-ADC at high input frequencies and leads to conversion failures when the resulting error exceeds the built-in redundancy of the architecture. In conventional designs with SHA there is generally an intentional skew in the sampling instant of the two paths; with MDAC path sampling first to ensure that MDAC path is not corrupted by the kickback noise from the sub-ADC path. In the design without SHA it still may be desirable to let MDAC sample earlier than the sub-ADC. The dynamic offset resulting from this skew can be accounted for in the error budgeting of the sub-ADC.

Sampling time constant mismatch: The mismatch in the sampling bandwidths of the MDAC path and sub-ADC also leads to aperture error. Let τ be mismatch in the time constant of two paths then it can be shown the aperture error is given by

$$\Delta V = 2\pi * V_{ref} * F_{in} * \tau \tag{2}$$

This means that either the two paths must be very wideband compared to largest signal frequency of interest or the paths must match precisely to make sure that dynamic offset resulting from time constant mismatch is within the redundancy range of the architecture. Figure 3.3 shows the two sampling paths in a typical pipeline ADC [76]. The MDAC path contains two switches and sampling capacitor Cs. The input switch S_1 is normally bootstrapped to have a constant gate source voltage to achieve good linearity. The flash path contains a switch, sampling capacitor and the preamplifier in the sampling path.

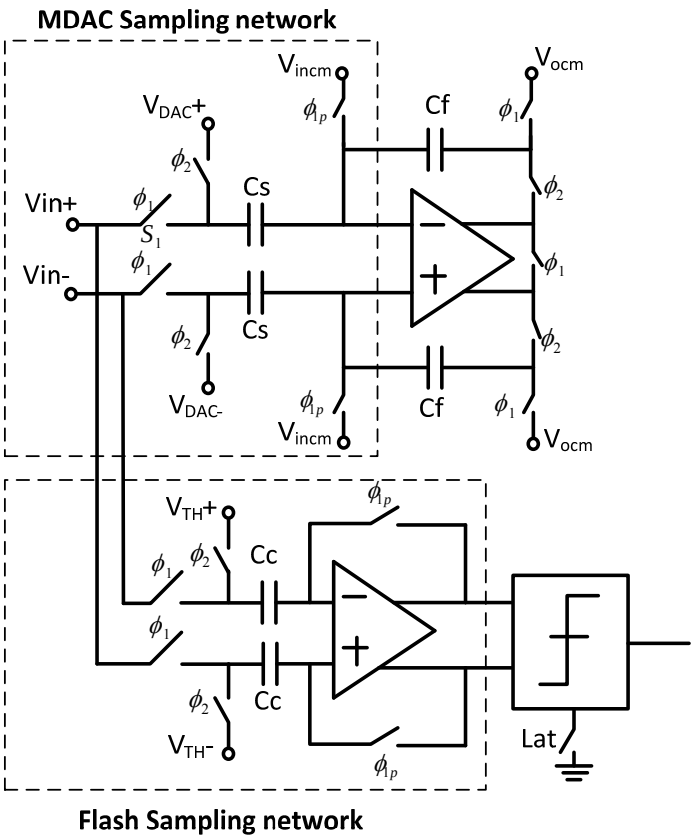


Figure 3.3 Sampling network time constant matching

In this architecture the preamplifier must have a large bandwidth to match the bandwidth of the sampling network in MDAC path. One option will be to remove the preamplifier in the design of flash comparator. In this case both the sampling paths only contain sampling capacitor and switches and can be matched to some extent. The drawback of this approach will be that overall comparator offset will increase limiting the number of bits that can be resolved by the sub-ADC.

Despite the drawbacks listed above removing the SHA has been found to be a very effective technique to reduce power and is implemented in many designs. The above mentioned problems have been solved by the some of the techniques discussed

next. By reducing the number of bits in sub-ADC the allowed offset budget (random + dynamic) is increased. Though this is not optimal from the ADC power perspective, power savings obtained from eliminating SHA outweighs it. The designs in [77, 78, 79] rely on this to combat dynamic offset. By increasing the redundancy [80] a larger offset can be tolerated in sub-ADC, but this is the same as resolving less number of bits in the first stage. Other scheme described in [81] utilizes the S/H in the MDAC as an S/H for the sub-ADC. It does require creating an additional clock phase slowing down the overall operation. Yet another work [82] calibrates the clock skew between the two paths. The works in [76, 83] rely on matching the time constant and minimizing clock skew on the two paths.

3.2 Reference Scaling

With the reduced supply voltages in advanced CMOS nodes it becomes challenging to design a high gain opamp with wide signal swing. The concept of the reference scaling is to reduce the gain in the first stage residue amplifier to reduce the swing at the output of the first stage. In a typical pipeline with N-bit of resolution in the first stage the residue is scaled up $G = 2^{N-1}$ so that the later stage sees a nominal signal swing of $+/-V_{ref}/2$. The signal swing with the opamp offset and flash inaccuracy can be as large as $+/-V_{ref}$. Figure 3.4 shows the residue plot of a pipelined ADC with residue being scaled by a factor α. The benefits of the reference scaling are listed next.

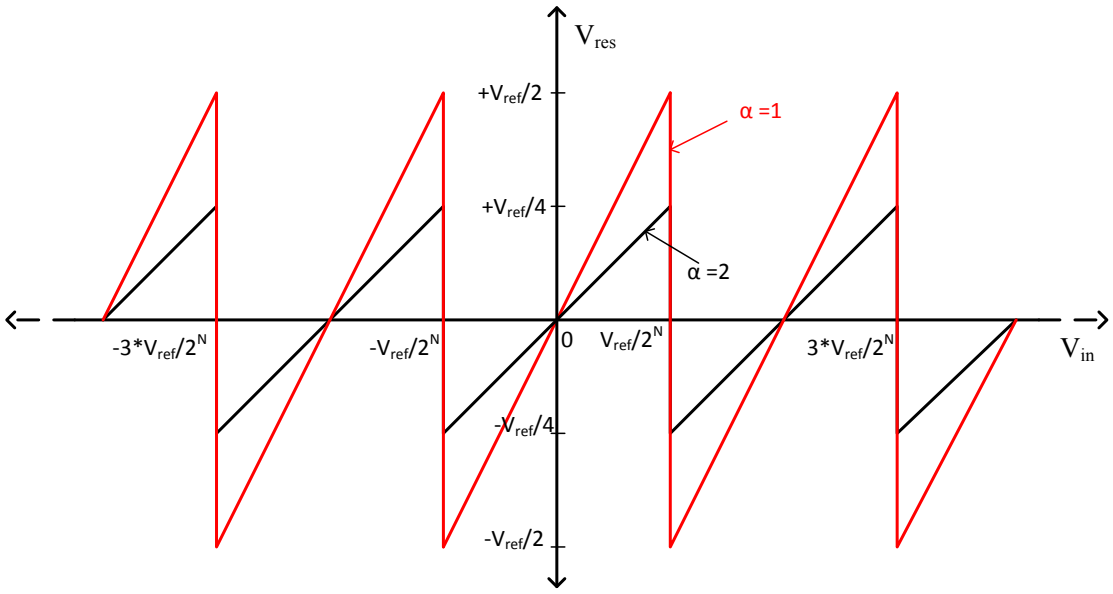


Figure 3.4 Residue plot of a pipelined ADC with reference scaling α

1. Reduced open loop DC gain requirement

For a N-bit first stage (shown in Figure 3.3) with no reference scaling $C_s = 2^{N-1}C_f$. Ignoring the parasitic at the virtual ground node of residue amplifier the feedback factor β is given by $\beta = \frac{1}{1+2^{N-1}}$. As the gain in the first stage is dropped while scaling the reference, the feedback factor β increases. For the reference scaling by a factor α the feedback factor increases to $= \frac{\alpha}{\alpha+2^{N-1}}$. For a given open loop gain A_{dc} in the opamp this increases the closed loop DC gain βA_{dc} of the residue amplifier. This reduces the error due to finite gain in the opamp.

2. Reduced swing at the output

The reduced output swing allows getting some DC gain out of the output stage using cascoding techniques. This is very useful in advanced CMOS nodes where it may be very difficult to get adequate DC gain even with two stage opamps. Also with reduced

signal swing a single stage telescopic cascode amplifier may be sufficient with some digital calibration. The reduced complexity of the residue amplifier leads to reduction in power as multi-stage opamps are difficult to compensate and require more current for the same bandwidth.

3. Reduced open loop bandwidth requirement

As discussed above the increased reference scaling increases the feedback factor β. This means that for same settling error requirements a smaller open loop bandwidth is required. For a single stage opamp the closed loop bandwidth is given by $\omega_o = \beta g_m / C_L$. If the load C_L is held constant than the g_m required can be decreased by the same factor as the β is increased thus saving power [84]. In practice the load C_L will increase with the increased reference scaling diminishing the benefits of increased β. The load C_L increases because of the two factors (a) the loading from the feedback path increases (b) the later stage sampling capacitance has to increase to reduce its noise contribution. The total load C_L at the output of the first stage can be given by

$$C_L = \beta C_S + C_{S2} + C_p \quad (3)$$

Here βC_s is the loading from the feedback path, C_{S2} is the second stage sampling capacitor and C_p is the additional capacitor for the next stage flash, the loading from the common mode feedback circuit, the device capacitance on the opamp and routing parasitics. For high interstage gains C_p term can dominate the load capacitance. Normally the second stage will be scaled such that it contributes less input referred noise compared to the first stage. Assuming the second stage contributes 3dB less noise than first stage it can be seen that

$$C_{S2} = \frac{C_S * \alpha^2}{2^{2N-3}} \quad (4)$$

For a given bandwidth ω_o required g_m is given by

$$g_m = \omega_0 \left[C_S + \frac{C_{S2}+C_p}{\beta}\right] = \omega_0 \left[C_S + \frac{C_S * \alpha * (\alpha + 2^{N-1})}{2^{2N-3}} + \frac{C_p * (\alpha + 2^{N-1})}{\alpha}\right] \quad (5)$$

Let $C_p = k * C_s$ then

$$g_m = \omega_0 C_S \left[1 + \frac{\alpha * (\alpha + 2^{N-1})}{2^{2N-3}} + \frac{k * (\alpha + 2^{N-1})}{\alpha}\right] \quad (6)$$

It can be seen from (6) that g_m requirement because of the feedback loading remains same as the reference is scaled. g_m requirement because of next stage loading increases as α is increased and g_m requirement because of all other parasitic loads (C_p) decreases as reference is scaled. Figure 3.5 shows curve of normalized g_m as α is varied for different values of N and k. It can be seen from the curves above that the g_m requirements on the opamp does drop initially as the reference is scaled and β increases but the benefit diminishes as the capacitance on next stage needs to be increased because of noise. The designs with large number of bits in first stage [84] will benefit more from aggressive reference scaling. The above analysis for a single stage opamp shows that the open loop bandwidth requirements on opamp do get relaxed by reference scaling. The power savings from this is in addition to the one obtained from simplified design. Reference scaling is a powerful technique in low voltage designs and has been reported in some recent publications. Some works including reference scaling are [85-88].

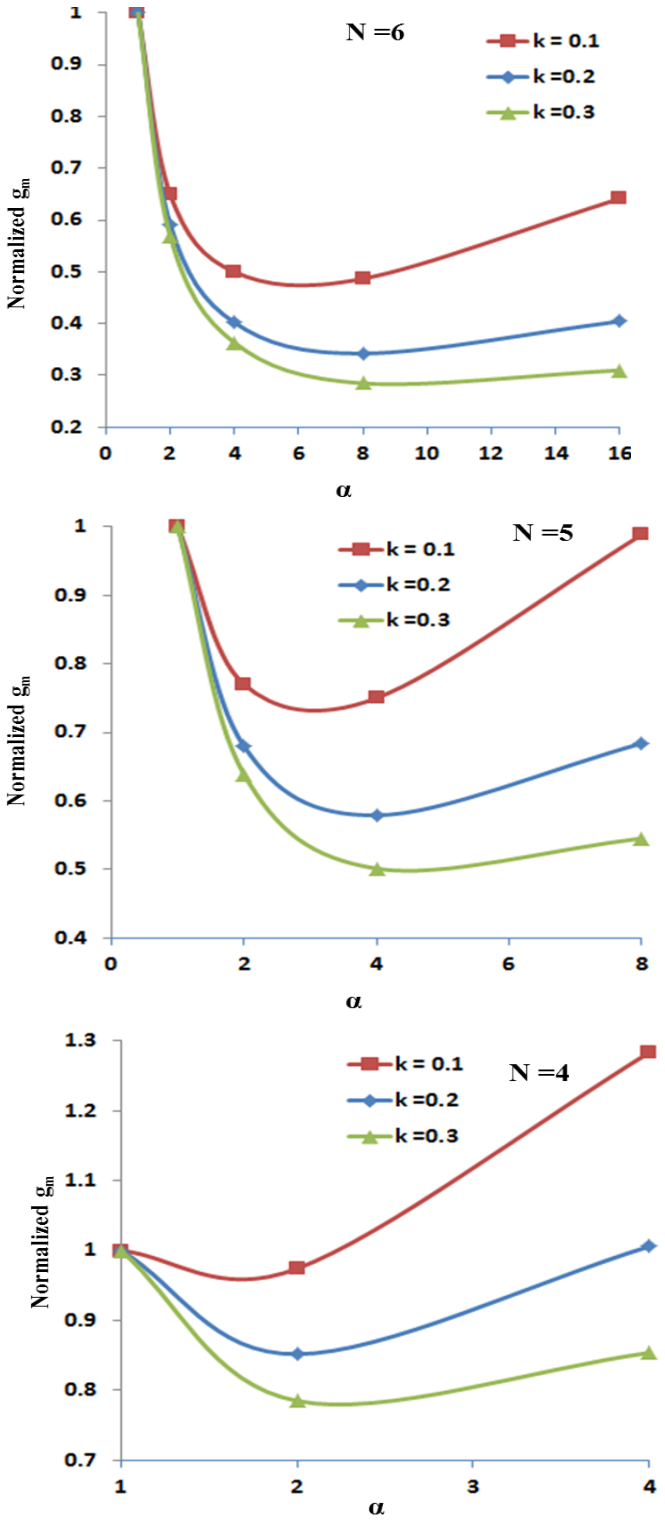


Figure 3.5 Power consumption trends with reference scaling factor α

3.3 Reference Refreshing technique

The reference refreshing technique [89, 90] illustrated in Figures 3.6 doesn't require a high gain opamp in the MDAC. It solves the problem of error in the interstage gain (G) by adjusting the reference to the next stage by the same factor as the error in the interstage gain G. This can be explained by a simple example. Let's assume that the interstage gain for i^{th} stage has an error ε_i so that gain is $G_i(1+\varepsilon_i)$. In this case residue for the $(i+1)^{th}$ stage is given by

$$V_{res[i+1]} = G_{[i+1]}(1+\varepsilon_{[i+1]})\{G_{[i]}(1+\varepsilon_{[i]})[V_{in[i]} - D_{[i]}V_{ref[i]}] - D_{[i+1]}*V_{ref[i+1]}\} \quad (7)$$

If the reference to the $(i+1)^{th}$ stage is changed such that $V_{ref}[i+1] = (1+\varepsilon_i)V_{ref}[i]$ then (7) can be written as

$$V_{res[i+1]} = G_{[i+1]}(1+\varepsilon_{[i+1]})\{G_{[i]}(1+\varepsilon_{[i]})[V_{in[i]} - D_{[i]}V_{ref[i]} - D_{[i+1]}*V_{ref[i]}]\} \quad (8)$$

showing that the nonlinearity due the error in interstage gain is no longer present and it only appears as a gain error term for the ADC.

The design in [90] generates the reference for different stages by propagating the reference voltage through the same gain stages as the residue so as to introduce the same gain error in the reference. By applying the same gain to both reference and the signal interstage gain error is cancelled. One of the problems of the above approach is that the offset in the residue amplifier changes the reference value when the reference is being passed through the gain stage. This leads to distortion, so the opamp offset needs to be calibrated or needs to be small enough to use this reference refreshing technique.

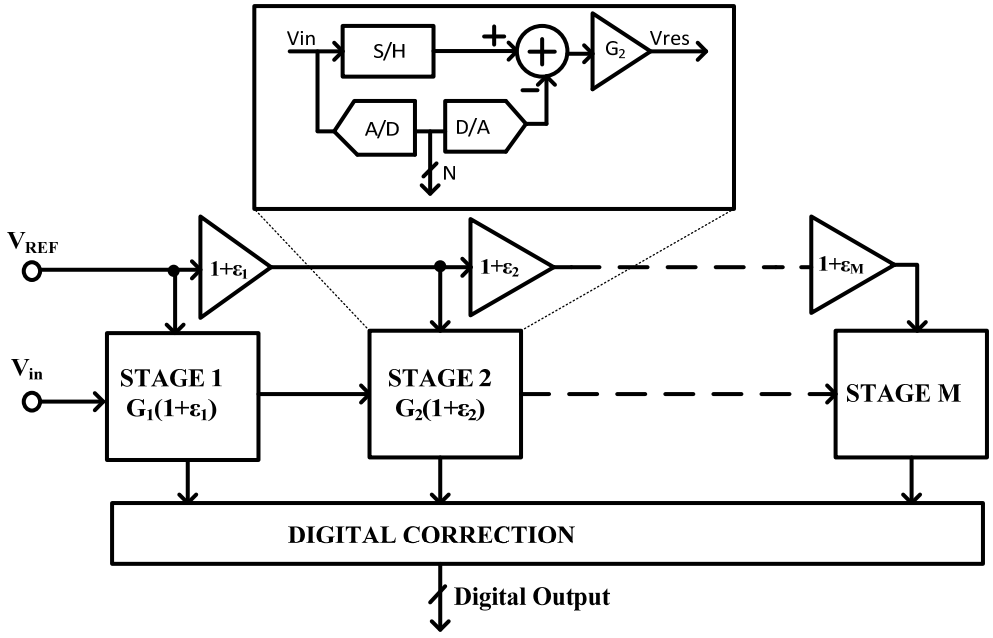


Figure 3.6: Pipelined ADC architecture with reference refreshing

3.4 Two step amplification techniques

In this section we look at some techniques which achieve high accuracy in the residue amplification using two steps in time domain. Using the techniques described below a highly accurate interstage gain can be implemented using a low gain opamp. Low DC gain opamps typically consume much lower power than multi-stage high gain opamps.

3.4.1 Correlated Double sampling

One solution to low opamp gain problem is the use of correlated double sampling (CDS) technique [91]. CDS techniques have been used successfully in integrator and amplifier designs. With CDS, the error resulting from the finite opamp gain becomes inversely proportional to the square of the opamp gain.

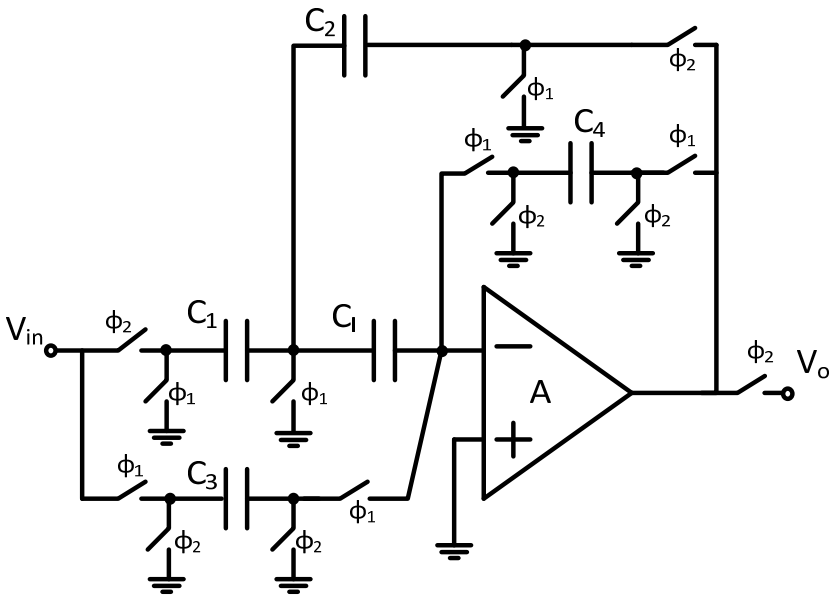


Figure 3.7 Amplifier with correlated double sampling (CDS)

Furthermore, the opamp offset is removed, and 1/f noise is also suppressed. Fig 3.7 shows a switched-capacitor amplifier with CDS technique. The input is assumed to be held constant over phase's φ_1 and φ_2. During phase φ_1, a preliminary amplification (PA) operation is performed using capacitors C_3 and C_4. This operation suffers from an error due to the finite gain, giving rise to a nonzero voltage at the inverting input of the amplifier. This voltage is stored in C_I. During phase φ_2, the desired amplification (A) is done using C_1 and C_2 with C_I placed in series with the inverting input of the amplifier. The finite gain error with CDS technique can be quantitatively represented by means of the equation

$$V_o(n) = -\frac{C_1}{C_2}V_{in}(n) - \epsilon \tag{9}$$

Where

$$\epsilon = \frac{1}{A^2}\left[1 + \frac{C_1}{C_2}\left[\left(1 + \frac{C_1}{C_2} + \frac{C_I}{C_2}\right)V_o(n) - \frac{C_1}{C_2}V_o(n-1)\right]\right] \quad (10)$$

Note that the error is inversely proportional to A^2. This makes it much smaller than the error in the conventional circuits, which can be shown to be inversely proportional only to A. However, the straightforward implementation of CDS in pipelined ADC design increases load on the opamp and adds one extra clock phase.

The work in [92] solves this issue with some timing adjustments to the conventional CDS scheme. The scheme called time-shifted CDS is compared to traditional CDS scheme in Figure 3.8. In the traditional timing scheme illustrated in Figure 3.8(a) there are there three phases. In first phase both set of capacitors sample the inputs (S &PS), second phase is the preamplification phase (PA) and the third phase is the amplification phase (A). It is during this amplification phase that the second stage samples the input. This leads to reduced throughput in a pipeline ADC design with conventional CDS scheme. In the time-shifted CDS technique illustrated in Figure 3.8(b) the extra clock phase is removed by using preliminary residue voltage (from stage i) for sampling in the preamplifying phase of stage (i+1) and merging the amplifying phase and the presampling phase in one time slot. The splitting of sampling and presampling in two separate time slot helps remove any extra capacitive loading from extra sets of capacitors. The speed and/or power consumption overhead in the conventional CDS technique is removed completely with this scheme. This technique has potential to reduce power consumption as very simple single stage opamps can be used for residue amplification.

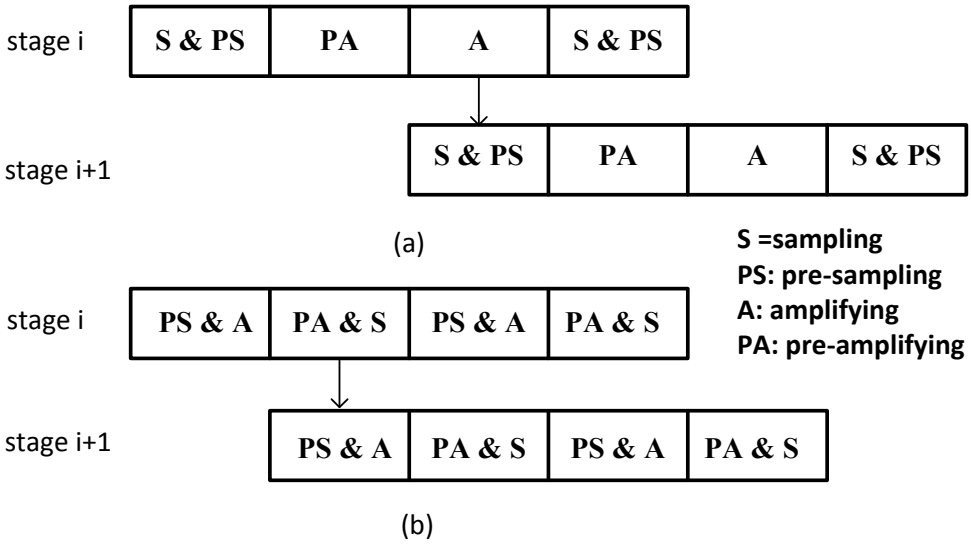


Figure 3.8 Timing change from conventional CDS to time-shifted CDS.

3.4.2 Correlated level shifting

Correlated level shifting (CLS) is a general technique that reduces opamp errors due to finite gain and increases the distortion-free swing. The basic CLS MDAC structure introduced in [93] and shown in Figure 3.9 can be used to reduce finite opamp gain error and increase the opamp's useful output swing. After sampling the input in phase φ_S, the MDAC switches into an amplification phase φ_A which is split in two parts the estimation phase (φ_{EST}) and the level shifting phase (φ_{CLS}). In the estimation phase an estimate of correct output voltage with respect to common mode voltage V_{CMO} is sampled on the CLS capacitor. In the level shift phase the capacitor C_{CLS} is connected between the MDAC output and the opamp output, which level shifts the opamp output back to V_{CMO}. The opamp now only processes the error of the initial estimate which will reduce the finite opamp gain error and reduces the opamp output swing. It is shown in [93] that the effective gain with this approach is proportional to A^2.

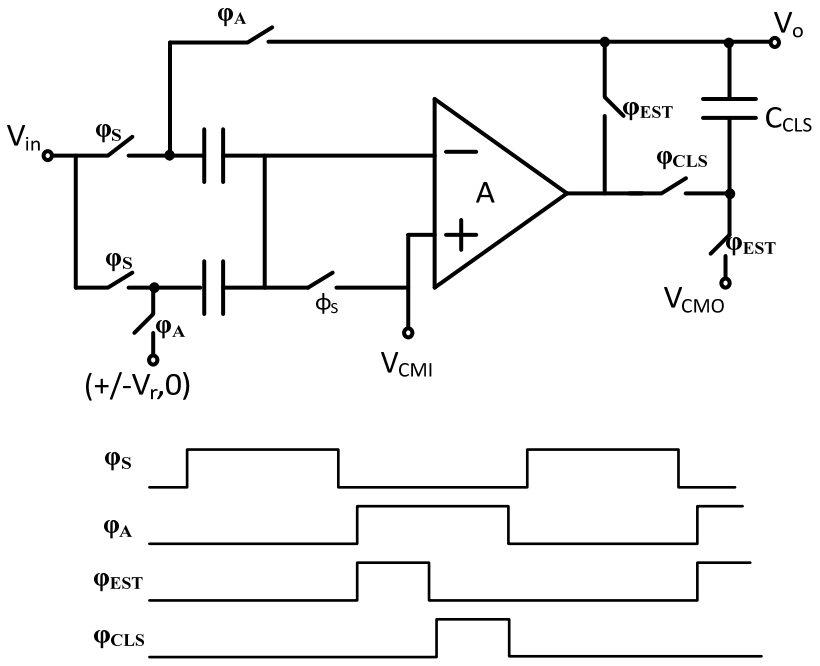


Figure 3.9 Correlated Level Shifting

The work in [94] optimizes the CLS design further by realizing that the gains A_{EST} and A_{CLS} do not necessarily need to be the same or even come from the same amplifier. By splitting the amplifier in Figure 3.9 into two separate amplifiers and then designing each amplifier with its specific requirements in mind, the the overall performance of CLS in terms of power, speed, and accuracy can improve. Figure 3.10 shows a generalized single ended Split-CLS structure. Amplifier $A\varphi_1$ processes the full signal during estimation phase and is directly connected to the output load. Therefore, for optimum performance it should have as large of an output swing as possible and high slewing capabilities. By contrast, $A\varphi_2$ must only process the small error term and charges the output indirectly through C_{CLS}.

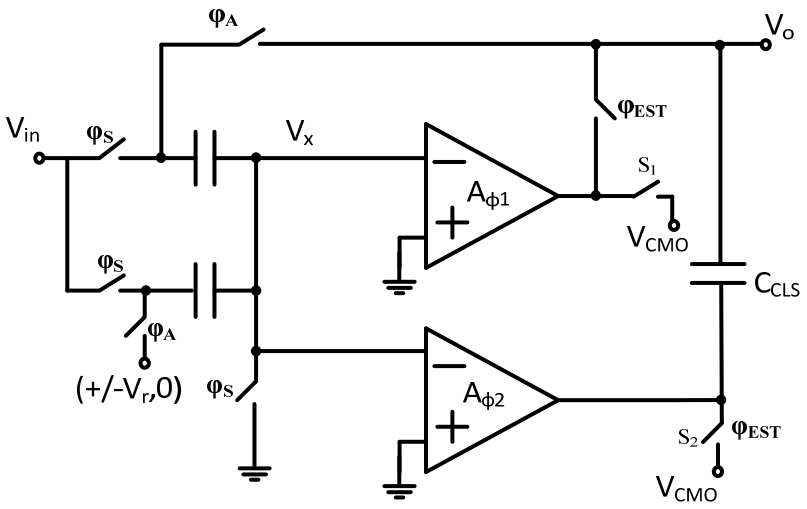


Figure 3.10 Split CLS

The output swing of the $A\varphi_2$ amplifier is much smaller than the $A\varphi_1$ amplifier. The work in [94] uses a dynamic zero crossing based circuit [ZCBC] discussed in next section for amplifier in estimation phase and a regular opamp in the level shifting phase. Power savings are obtained by using a simple telescopic amplifier for $A\varphi_2$.

3.4.3 Extended Correlated Double Sampling (ECDS)

Extended correlated double sampling introduced in [95] is an immediate calibration technique to simultaneously reduce finite- opamp-gain errors and increase the maximum output swing of the opamps while operating from only two clock phases. ECDS is suitable in ADCs where the error that stems from low opamp gain in one stage can be processed in a later stage, such as in pipelined and algorithmic ADCs. Figure 3.11 illustrates the operating principle of ECDS scheme. The output of the first stage V_{o1} during φ_2 phase is given by

$$V_{o1} = 2V_{in} - D_1 V_R + \varepsilon \tag{11}$$

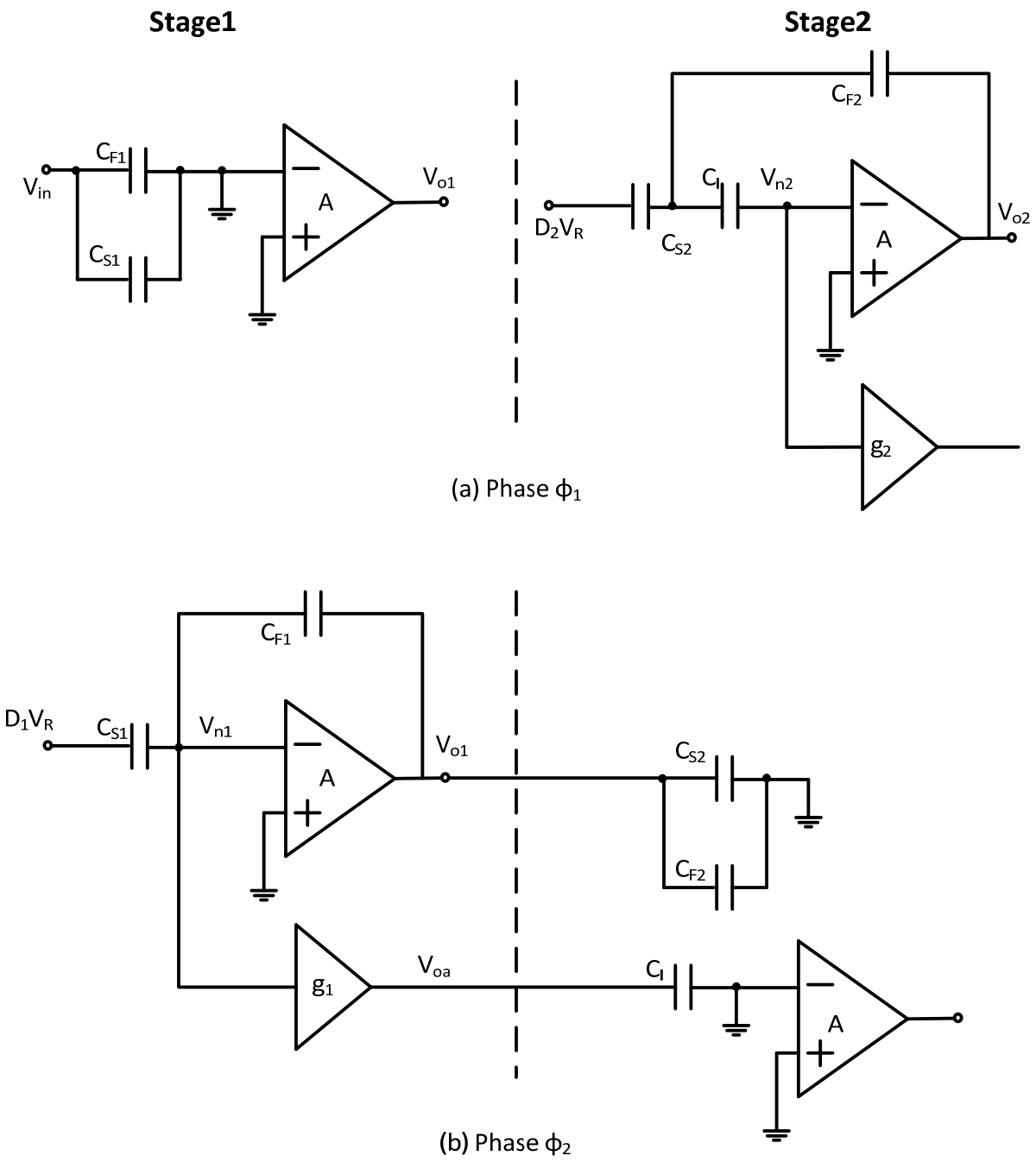


Figure 3.11: Extended correlated double sampling (a) Phase φ_1 (b) Phase φ_2

Where D_1 is the output of the sub-adc and is -1, 0 or 1 and ε is the error in the output. If the parasitic capacitance at the the opamp input is ignored the feedback factor during φ_2 is ½ and the error ε is given by

$$\varepsilon = -2\frac{V_{o1}}{A} \tag{12}$$

The voltage at the opamp input V_{n1} is equal to 0.5 ε. If this voltage V_{n1} is inverted, amplified by a factor of 2 and added to V_{o1}, the effect of the ε in V_{o1} is canceled. This cancellation of the error is done in the second stage. During the φ_2 phase the first stage's residue V_{o1} is sampled onto the second stage's capacitors C_{S2} and C_{F2}. Also in the same phase, V_{oa} which is an inverted version of the error ε in V_{o1}, is sampled on an extra capacitor C_I. V_{oa} is generated by amplifying the voltage at the opamp input V_{n1}, by an auxiliary amplifier with a gain of $g_1 = -2$. Next, during φ_1 phase, the second stage cancels the first-stage error ε by placing the extra capacitor C_I between the node that joins C_{S2} and C_{F2} and opamp input. This placement means that V_{o1} is added to $V_{oa} = -\varepsilon$ in the second stage, completely canceling the effect of the error in V_{o1} if the capacitors are matched and the parasitic capacitances are zero. In practice the parasitic capacitance and non-ideal gain in auxiliary amplifier will limit the effectiveness of the technique [95].

3.5 Residue amplification without amplifiers

Since the residue amplifiers consumes the majority of power in pipeline ADC stage there have been attempts to generate residue without any operational amplifier. In this section we look at two of the techniques which reduce power consumption by eliminating the opamp.

3.5.1 Zero Crossing Based Circuits (ZCBC)

Zero crossings based circuits are a generalization of comparator based switched capacitor circuits (CBSC) that was introduced in [96]. CBSC architecture replaces the function of the opamp with the combination of a comparator and current source to realize the same charge transfer as an opamp-based implementation. It completely eliminates opamps from the design and does not require stabilizing a high-gain, high-speed feedback loop. This not only reduces complexity but also eliminates the associated stability versus bandwidth/power tradeoff. A simplified schematic of the CBSC MDAC stage is shown in Figure 3.12. The sampling phase φ_1 is similar to traditional opamp based design. In the charge transfer phase φ_2 opamp is replaced by a current source and a comparator. When φ_2 goes high to enter the transfer phase, a short pulse is used to initialize the charge transfer by closing switch S_1 to pre-charge the output voltage to ground. Following this pulse, S_1 opens and the current source I_1 charges the capacitors to generate a constant voltage ramp on the output voltage.

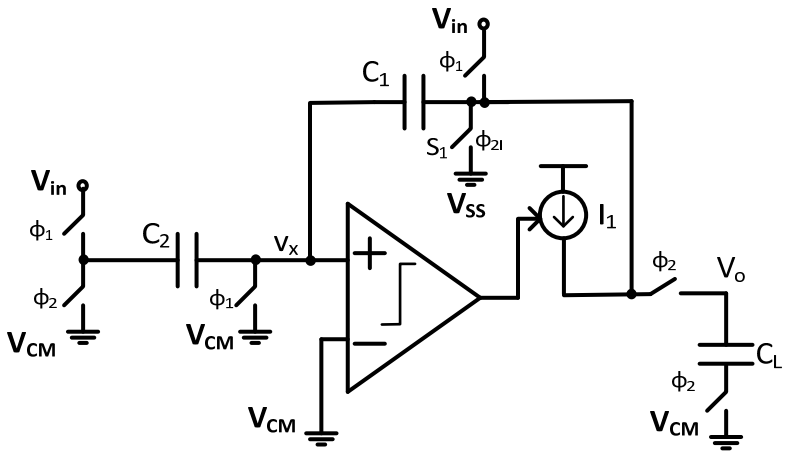


Figure 3.12 CBSC based gain stage

This causes the virtual ground voltage to ramp with it via the capacitor divider consisting of $C_1$and C_2. As the voltage ramp proceeds, the comparator will detect when the virtual ground condition has been reached and then turn off the current source to realize the same charge transfer as the opamp-based implementation.

The work in [97] extended the work on CSBC by realizing that a general purpose comparator is not required for zero crossing detection by the comparator. The comparator in CSBC scheme consumes static power which is reduced in ZCBC scheme by using a dynamic zero crossing detector circuit. The work in [98] further improves the resolution, power efficiency, and robustness of the previous ZCBC designs through various means including fully differential signaling, offset compensation, and output range enhancement. The work in [99] presents a high resolution, low power voltage scalable zero crossing based pipelined ADC which works at supply voltage as low as 0.5V.

3.5.2 Capacitive charge pump based Circuits

Capacitive charge pumps are widely used as voltage doublers in DC-DC converters. The work in [100] uses a doubler circuit to build a residue amplifier for a low power pipelined ADC. The concept of building a gain of two amplifiers using a charge pump is shown in Figure 3.13. A unity-gain buffer is used in Fig. 3.13 to prevent charge sharing between the sampling capacitors C_s, and load capacitance C_L. Ignoring the parasitic capacitors the output voltage is given by

$$V_o = -2(V_{in} - V_{CM}) + V_{DAC} \tag{13}$$

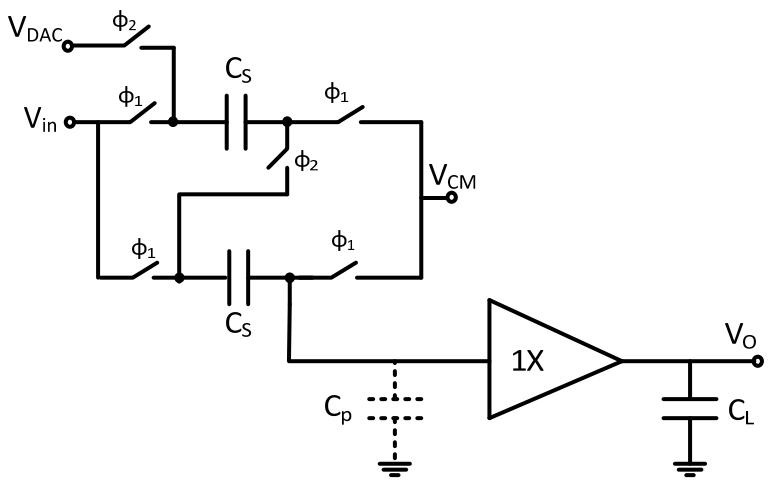


Figure 3.13 Gain of approximately two using a capacitive charge pump

With a capacitive charge pump, the gain is determined by the sampling capacitor arrangement, whereas the bandwidth of the output V_o, during φ_2 is independently established by the unity-gain buffer and C_L. An additional advantage of gain with capacitive charge pumps is that in each pipeline stage since the unity-gain buffer is preceded by the amplification of the input, the noise-power of the buffer when referred to the input of the pipeline stage is reduced by the square of the stage-gain. Hence the buffer adds only a small noise contribution, enabling the use of small sampling capacitors (thus reduced power consumption) to meet the desired thermal noise floor.

If the dominant parasitic capacitor C_p is included the output of the classical charge pump based MDAC is given by

$$V_o = -\left[\frac{2}{1+2(Cp/Cs)}(V_{in} - V_{CM}) - \frac{1}{1+2(Cp/Cs)}V_{DAC}\right] \quad (14)$$

which is a direct function of parasitic capacitors. The work in [100] uses digital calibration to correct for the error in the inter stage gain. The design achieves low power by using a simple source follower as the unity gain buffer.

3.6 Amplifier Sharing:

To reduce the power dissipation, the number of op amps in each pipeline can be reduced by sharing op amps between stages [101]. In general, switched-capacitor circuits afford themselves to amplifier sharing between two different switched-capacitor networks working on opposite clock phases. This is because these networks require the op amp only during the amplification/integration phase and not during the input sampling phase. A scheme showing the sharing of opamp between two stages 'A' & 'B' is illustrated in Figure 3.14 Here, the capacitors C_1 and C_2 are the parts of switched capacitor stage A whereas C_3 and C_4 are part of stage B. These two switched-capacitor networks operate on opposite clock phases, with the op amp alternating between them.

Although the amplifier sharing helps reduce power there a few potential drawbacks of the scheme. First, the additional switches that are used to implement amplifier sharing introduce series resistances which, in combination with the op-amp input capacitance, affect the settling behavior of the stage. Second, the nonzero input voltage of the amplifier is never reset. Thus, every input sample is affected by the finite-gain error component from the previous sample. Third error voltages, including flicker noise and the opamp's intrinsic offset voltage, cannot be cancelled because the amplifier is always in the active mode.

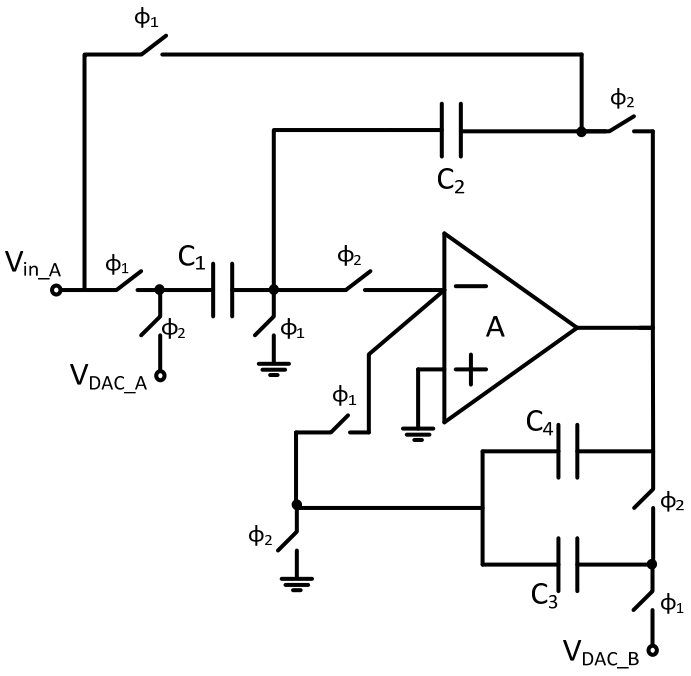


Figure 3.14 Amplifier sharing between two adjacent stages in pipeline

The work in [102] introduces a feedback signal polarity inverting (FSPI) technique to reduce the opamp offset and flicker noise to one third compared to a traditional design of a 1.5bits per stage pipeline. Another issue with amplifier sharing is the crosstalk between the stages because of the source drain parasitic capacitances of 'off switch'. The work in [103] addresses the issue with modified timing and using dummy switches. The work in [81] solves the issue by adding additional switches to isolate the opamp sharing stages. The works in [79, 104] extend the amplifier sharing to share capacitances as well.

3.7 Digital Calibration

The finite gain in the opamps causes the inter-stage gain in the pipeline to deviate from its ideal value. For illustration we look at a two-stage ADC in Figure 3.15 with the interstage gain having an error of ε. This gain can be corrected in the digital domain by doing an inverse transfer function on the M LSB bits as illustrated in Figure 3.16. For a pipelined ADC this concept can be recursively applied to all the stages starting with the last stage. The error ε can be determined with a foreground calibration scheme or a background calibration scheme. Foreground calibration estimates the unknown errors sources by interrupting normal ADC operation and applying a known input sequence to the ADC. By comparing the output of the ADC to the expected ADC output under ideal conditions (i.e. no non-idealities) the impact of each error source can be measured and corrected.

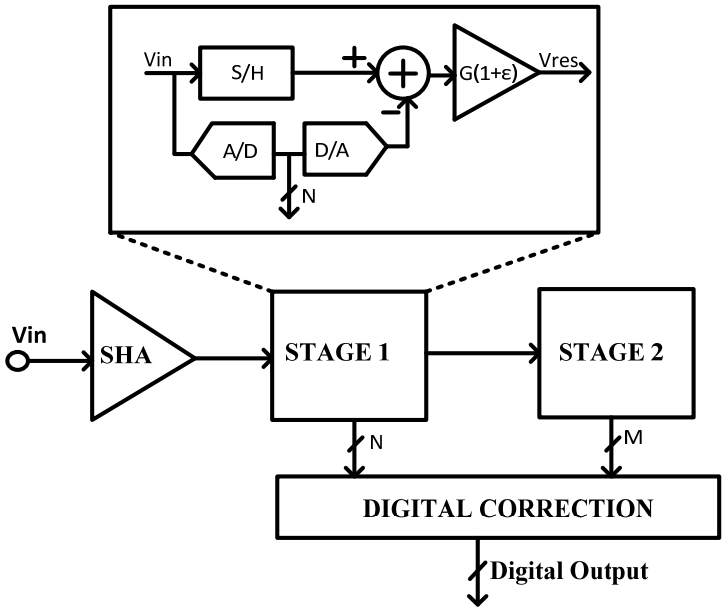


Figure 3.15 Two stage ADC with interstage gain error

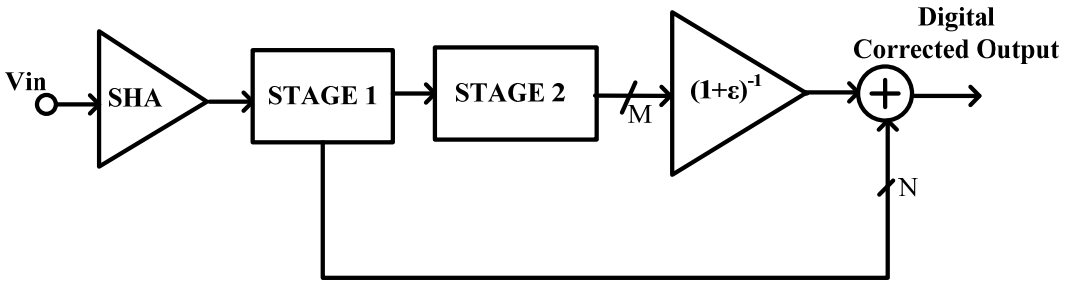


Figure 3.16 Digital calibration of gain error

The advantage of a foreground scheme is that calibration can be achieved within a small number of clock cycles. The disadvantage of foreground calibration is that the ADC is required to be taken offline every time calibration is performed, which in some applications may not be possible. Background calibration continuously measures and corrects the effect of non-idealities in a pipeline stage, thus has the significant advantage that the ADC is not required to be taken offline to perform calibration. The digital calibration techniques can be used to trade-off analog complexity for digital complexity. With the advances in CMOS technology this is a favorable tradeoff as the digital power keeps scaling in advanced process nodes. There has been a large amount of research on power reduction techniques which reduce the power in the opamp by using a low gain opamp and then correcting the error in digital domain. The work in [105] uses open loop amplifiers instead of traditional closed loop amplifiers to save power, whereas the work in [106] uses amplifiers with incomplete settling. The work in [107] uses single stage Class AB amplifiers to achieve low power. Some other recent works relying on calibration to achieve low power are [78, 85, 88, 100, 108, 109, 110, and 111].

3.8 Performance Comparison

In the Table 3.1 we compare the performance of the various references listed in this chapter. We also highlight the power saving technique being employed in the referenced designs. Following code is used for the power reduction technique

A Digital Calibration B Reference Scaling C Shaless design

D Amplifier sharing E Reference refreshing F Zero Crossing based circuits

G CLS H Charge pump based I Correlated double sampling

One observation that can be made from the Table 3.1 is that regardless of the design techniques used latest pipeline ADCs benefit from process scaling. Best figure of merits are obtained by designs in 65nm process node followed by designs in 90nm node. This is due to the fact that newer designs are relying more on digital calibration and trying to minimize static power consumption in the designs.

Table 3.1 Performance comparison

Reference	Year	Power Reduction Technique	Process node	Area (mm^2)	Sample Rate (MHz)	SNDR (dB)	Power (mW)	FOM (fJ/conv)
[108]	2013	A	65nm	0.36	200	61.2	19.85	106
[85]	2013	A,B,C	65nm	0.225	1000	52.4	33	97
[99]	2012	A,F	65nm	0.36	50	67.7	4.07	41
[99]	2012	A,F	65nm	0.36	5	66.3	0.237	28
[107]	2012	A	90nm	0.36	30	65.2	2.95	66
[82]	2011	C	90nm	0.26	100	55	12.2	266
[84]	2011	B,C	65nm	0.16	50	66	3.5	43
[94]	2010	G	0.18um	1.1	10	69.5	8.4	344
[100]	2010	H	0.18um	1.4	50	58.2	9.9	298
[109]	2010	A	90nm	0.36	100	58	6	92
[77]	2009	A,C	90nm	0.5	500	52.8	55	308
[79]	2009	C,D	0.18um	0.86	50	58.4	12	353
[78]	2009	A,C	90nm	0.123	50	49.4	1.44	119
[83]	2009	C	0.18um	-	125	78.6	385	443
[86]	2009	B	65nm	0.164	80	60.1	10.4	157
[88]	2009	A,B	90nm	1	100	73	200	548
[98]	2009	F	90nm	0.3	50	62	4.5	87
[104]	2009	D	0.18um	2.2	80	53.2	36	1205
[110]	2009	A	90nm	4	100	67.6	92	469
[111]	2008	A	0.18um	3.91	20	73	285	3904
[93]	2008	G	0.18um	-	20.2	65	7.5	256
[87]	2008	B	65nm	0.34	30	65.1	18	408
[81]	2008	C,D	0.18um	0.7	30	57.41	21.6	1187
[97]	2007	F	0.18um	0.05	100	43.3	4.5	377
[106]	2007	A	0.35um	7.9	75	65.6	273	2338
[96]	2006	F	0.18um	1.2	7.9	52	2.5	973
[90]	2006	E	0.35u	5.28	10	62	19	1847
[92]	2004	I	180nm	2.52	100	54	67	1636
[103]	2004	C	0.18um		12	75.5	98	1678
[105]	2003	A	0.35um	7.9	75	68.2	290	1841
[76]	2000	C	0.35μm	2.6	40	59	55	1888

Chapter 4 Hybrid Voltage-Time domain ADC

In this chapter we present a design of a hybrid voltage-time domain ADC. The ADC architecture shown in Figure 4.1 consists of two stages. The first stage does voltage domain analog to digital conversion whereas the second stage converts the residue from the first stage using a VCO based ADC. The flash ADC in the first stage provides the 4 bits whereas a VCO and counter combination in the second stage provides remaining 9bits. The output from the two stages is combined together in the digital calibration block according to the relationship below.

$$DOUT = 256 * STAGE1\_OUT + 128 * \frac{COUNT}{COUNT\_FS} \quad (1)$$

where COUNT_FS is the COUNT obtained from the second stage when ADC input is $V_{REF}/16$ and STAGE1_OUT is the first stage output code. COUNT_FS acts as the reference for second stage and is determined by a calibration routine.

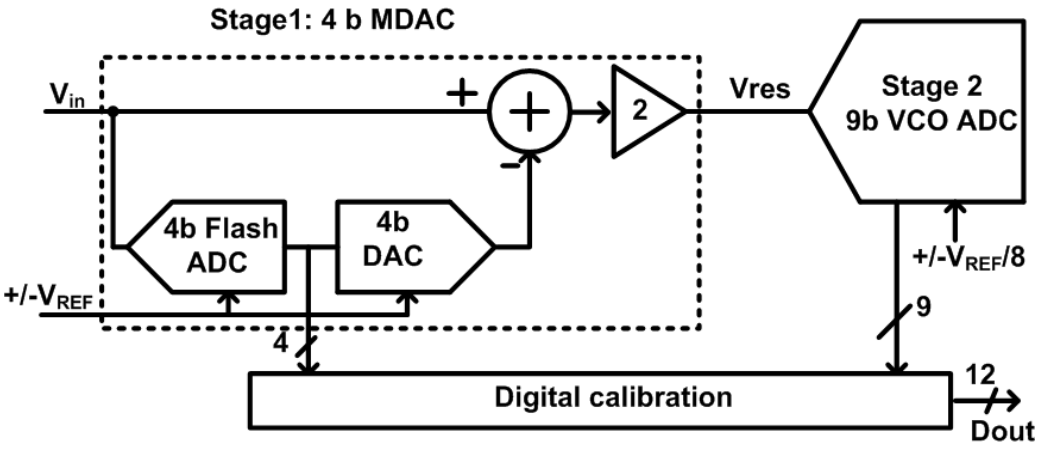


Figure 4.1 ADC architecture

The architecture helps relax the linearity requirement on the second stage by exercising only the linear input range of the VCO. The first stage also consumes significantly less power than a traditional pipeline ADC. In next section we discuss the power saving techniques in the first stage, followed by section on second stage design.

4.1 First stage power reduction techniques

In this section we look at various power reduction techniques utilized in this design to reduce the power consumption of the first stage.

4.1.1 Reference scaling

Although in this architecture the first stage resembles that of a pipeline ADC, its requirements are dramatically relaxed. The primary reason for this is that the VCO based backend allows aggressive reference scaling (the second stage reference is reduced by a factor of 8). As discussed in chapter 3 this helps in multiple ways. Firstly it helps to reduce power by increasing the feedback factor so that a lower bandwidth opamp can be used. Secondly it reduces the swing at the output of first stage which allows the use of a single stage opamp. The reduced swing also helps relax the linearity requirement of VCO based second stage. Such reference scaling is impractical in traditional pipeline ADCs because it leads to very small residue which is difficult to quantize in voltage domain due to comparator offsets and noise in the next stage. The design in [84] limits the reference scaling to two precisely for this reason. In our design quantizing the residue in time domain makes it feasible to digitize the small residue.

4.1.2 Reference refreshing

The reference refreshing technique [89, 90] illustrated in Figure 4.2 relaxes the opamp gain requirement in the MDAC. It solves the problem of error in the interstage gain (G) by adjusting the reference to the next stage by the same factor as the error in the interstage gain G. Traditionally the reference refreshing has been done in analog domain, requiring an additional capacitor array to update the reference for next stage. One of the problems of the analog approach is that the offset in the residue amplifier changes the reference value when the reference is being passed through the gain stage. This leads to distortion, so the opamp offset needs to be calibrated or needs to be small enough to use this reference refreshing technique.

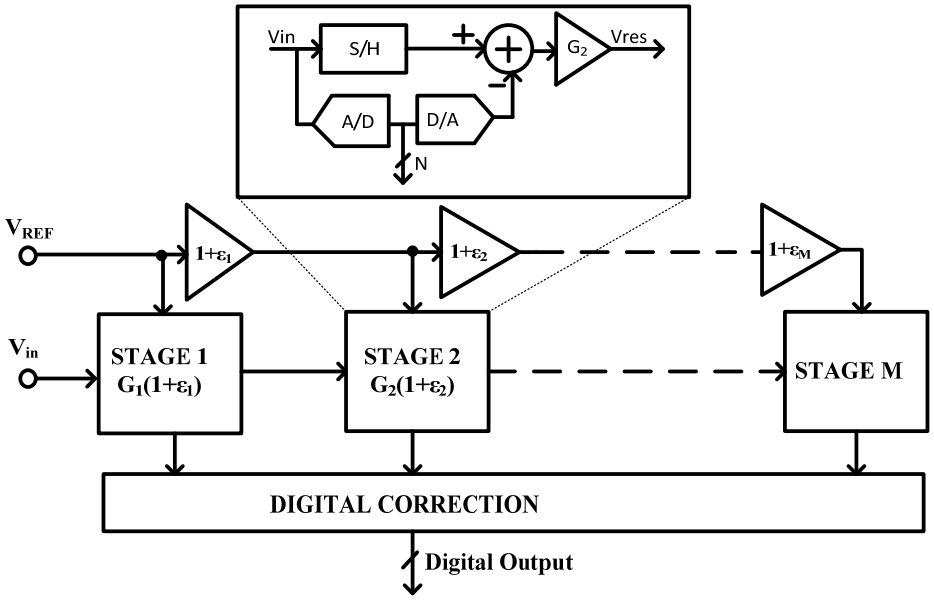


Figure 4.2 Conceptual illustration of reference refreshing technique

In our architecture the reference refreshing is done in digital domain without any additional analog complexity. The inter-stage gain error can easily be digitally calibrated by refreshing the reference to second stage, which is just a digital count referred as COUNT_FS. The calibration process is illustrated in Figure 4.3. First the offset calibration is performed as illustrated in Figure 4.3(a). In the φ_1 phase both the input sampling capacitor and feedback capacitor are reset. In the φ_2 phase the amplifier is converted to a gain stage with input capacitor still grounded. This gives the opamp offset voltage at the output which is converted to a digital count by the second stage. The calibration of finite opamp gain and mismatch in DAC capacitors is shown in Figure 4.3(b). Instead of directly connecting $0.125V_{REF}$ to the VCO following procedure is adopted. The input capacitor is reset in the sampling phase. In the amplifying phase (φ_2) one of the DAC unit capacitor (i) is connected to V_{REF} and the remaining unit capacitors are connected to ground. For ideal opamp this creates a residue equal to $0.125V_{REF}$ at its output and acts as a reference for VCO. Since reference passes through the same path as the signal it also gets scaled by the same factor ($1+\varepsilon_i$). The second stage creates a count COUNT_FS(i) which is the full scale count with i^{th} unit capacitor. The process is repeated for all the 16 unit capacitors and the full scale count (COUNT_FS) which is the reference for the second stage is determined as

$$COUNT\_FS = \frac{1}{16}\sum_{i=1}^{16} COUNT\_FS(i)$$

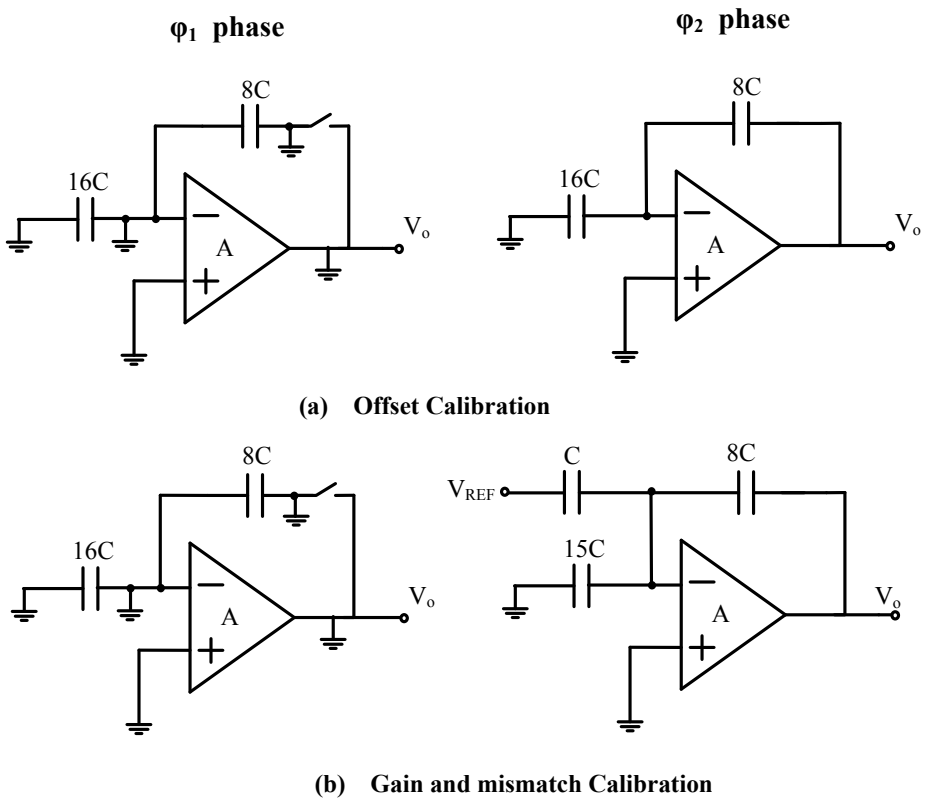


Figure 4.3 Calibration process to determine second stage reference

The interstage calibration scheme described above can also be used to correct the errors because of mismatch in the unit capacitors. The COUNT_FS can be modified to use only the unit capacitors which are used in a given code. Since for this design we need only 9-bits matching in the unit capacitor, so it was not necessary to perform calibration of unit capacitor mismatch. To improve the accuracy of calibration COUNT_FS can be obtained as an average of mulitple measurements. This scheme corrects for constant gain error term in the MDAC. It doesn't correct for gain error variation with swing at the output of the opamp. Since the swing at the output of the opamp is limited to +/-175mV the gain remains fairly constant.

4.1.3 Stage scaling

Scaling the sampling capacitance in the successive stages [103,112] has been shown to reduce the power consumption in a pipelined ADC. In this design interstage gain is equal to two and the second stage sampling capacitor is reduced by a factor of 4 to reduce the loading on first stage residue amplifier and hence reducing its power consumption. Scaling the sampling capacitor by a factor of four with an interstage gain of two will give equal noise contribution from both stages in the traditional design. In this design in the second stage noise aliasing occurs only in the sampling phase, so the kT/C_s noise only affects the sampling phase. In the hold phase the noise passes through an antialiasing sinc filter preventing noise foldover. Because of this reason the second stage in this architecture contributes significantly less thermal noise even with aggressive scaling of the sampling capacitor in second stage.

4.1.4 Reduced redundancy

In a traditional pipelined design a full one bit of redundancy is used to correct for the errors in the flash sub-ADC. In this architecture full one bit of redundancy is not required. The first stage actually gives full four bits of output. The reference to the second stage is $V_{REF}/8$ but the second stage input is allowed to swing beyond this reference. A larger residue translates into a higher count from the second stage which just needs more depth in the counters. The real constraint on the first stage output swing comes from the linearity of the VCO. As the input swing on the VCO becomes larger it becomes more nonlinear. So the VCO needs to be designed to remain linear

with a swing larger than +/-V_{REF}/8. The mismatch simulations indicate that the swing at the VCO input can exceed +V_{REF}/8 by as much as 60mV, so the VCO needs to be linear for a range of +/- (V_{REF}/8 + 60mV). This corresponds to a redundancy of about 0.5bits for 1V reference.

4.1.5 Design without front-end SHA

Figure 4.4 shows the block diagram of a conventional pipelined ADC with a sample and hold amplifier (SHA) at the front of the pipeline ADC. As discussed in chapter 3 front-end SHA consumes significant power and adds noise to the ADC. There can be significant power savings if the SHA can be removed [76]. The removal of SHA moves the burden of sampling the high frequency input to the first stage of the ADC. The first stage samples the input in the S/H build in the MDAC and the sub-ADC. Figure 4.5 shows the schematic of a comparator in a typical pipelined design [83] without front end sample and hold amplifier. During track phase φ_1 both the MDAC capacitors and the flash sampling capacitors C_{S_FLASH} simultaneously sample the input. A separate set of capacitors in the flash sample the reference threshold (V_{TH}). At the beginning of the φ_2 phase the preamplifier amplifies its input which is latched after some delay to produce the flash data. One of the challenges in this implementation is that the time available for MDAC settling is reduced by the total delay through the preamplifier and the latch during φ_2 phase. Hence, in this SHA-less front-end, both the flash comparators and the residue amplifier have to be faster and therefore consume more power compared to a conventional front-end implementation with a SHA.

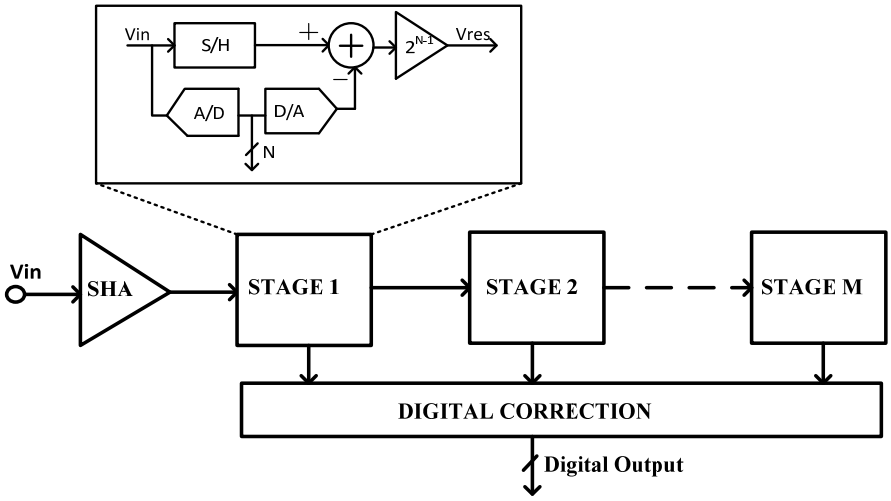


Figure 4.4 Block diagram of a conventional pipelined ADC

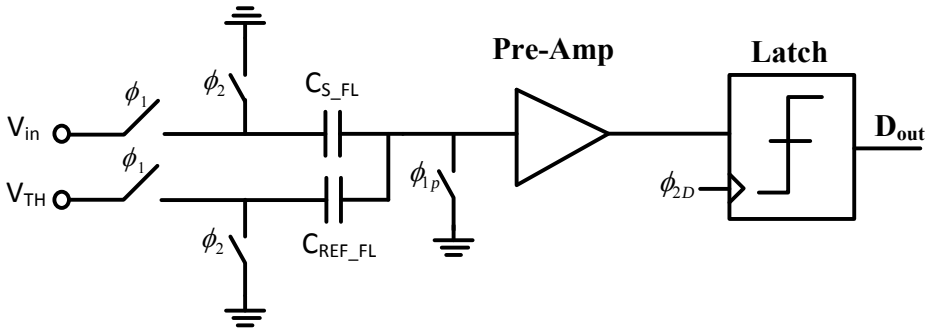


Figure 4.5 Comparator schematic for SHA-less design

In our design since the residue amplifier power is reduced significantly the preamp power in the latch starts dominating the power consumption in the first stage. To minimize the power consumption in the flash ADC the comparator is designed without a preamplifier in this design. Figure 4.6 shows the flash and MDAC sampling network for this design. During φ_1 phase both the MDAC and flash track the input. The MDAC path samples the input at the falling edge of φ_{1p} whereas the flash path latches the input on rising edge of Lat signal after a delay of Δt. This non-overlap of Δt ensures that there is no kickback at

the ADC input at the instant of MDAC sampling. The clock skew between the two paths lead to a dynamic offset in the comparator design given by

$$\Delta V = 2\pi * V_{ref} * F_{in} * \Delta t \tag{2}$$

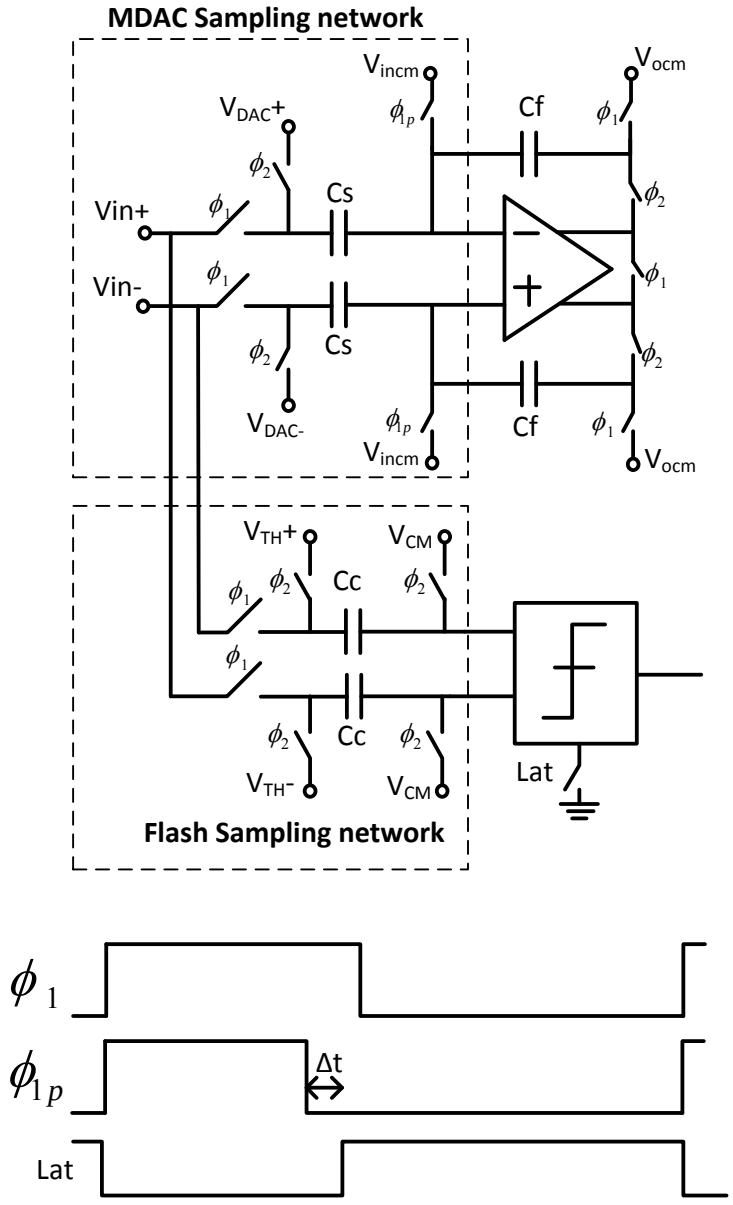


Figure 4.6 Sampling network

Since this design is targeted towards low to medium frequency inputs this dynamic offset is not a big concern. For a 10MHz sine wave and Δt=100ps the dynamic offset is about 6.3mV which can be budgeted for in the design. The benefit of such a scheme is no preamp power and no reduction in time available for residue amplification. The latch regenerates during the non-overlap time between phase φ_1 and φ_2. This scheme is suitable only for relatively low speed designs. For the high speed designs dynamic offset given by (2) may become too large to be handled by the redundancy in the design.

4.1 First stage design

The first stage uses a sampling capacitor of 1.2pF from thermal noise consideration. The input sampling switch uses a signal dependent boost technique [113] to achieve high linearity. Reference scaling by a factor of 8 makes the signal swing at the output of first stage very small so that it is possible to get a flat gain across the signal swing. The combination of reference refreshing and reference scaling allows the use of low gain, low power telescopic opamp show in Figure 4.7 as the residue amplifier in first stage. The opamp has an open loop gain of 49dB which remains constant to within 7% with the signal swing. All the devices in the opamp use non-minimum length to achieve this gain. The large channel length is also desirable to reduce the effect of flicker noise. The design uses a traditional switched capacitor common mode feedback circuit.

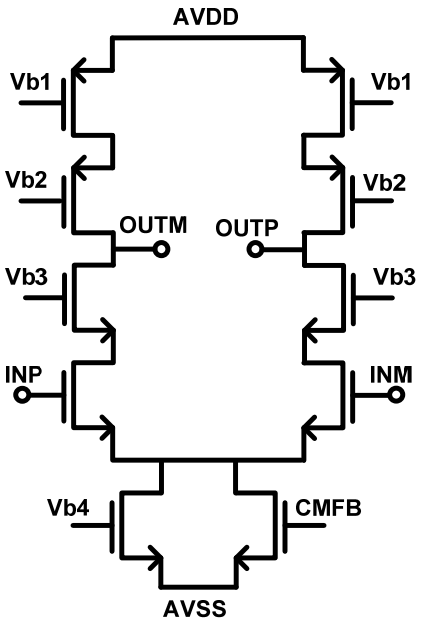


Figure 4.7: Residue amplifier schematic

4.2 Second stage design

Figure 4.8 shows the block diagram of the VCO based second stage. The residue from the first stage is sampled by a sample and hold stage. This sampled voltage is converted to current using a simple differential pair with degeneration. This output current controls the oscillation frequency of two current controlled ring-oscillators (CCO). The output frequency of each CCO is converted to digital form using dual edge counters on all three phases of the ring. The final COUNT obtained from the second stage is proportional to the difference between the frequencies of the two CCO's. This 'differential operation in the frequency domain' enhances the linearity of the voltage to frequency transfer curve of the VCO. The VCO is free running but to save power the counters are clocked only in the phase they are counting.

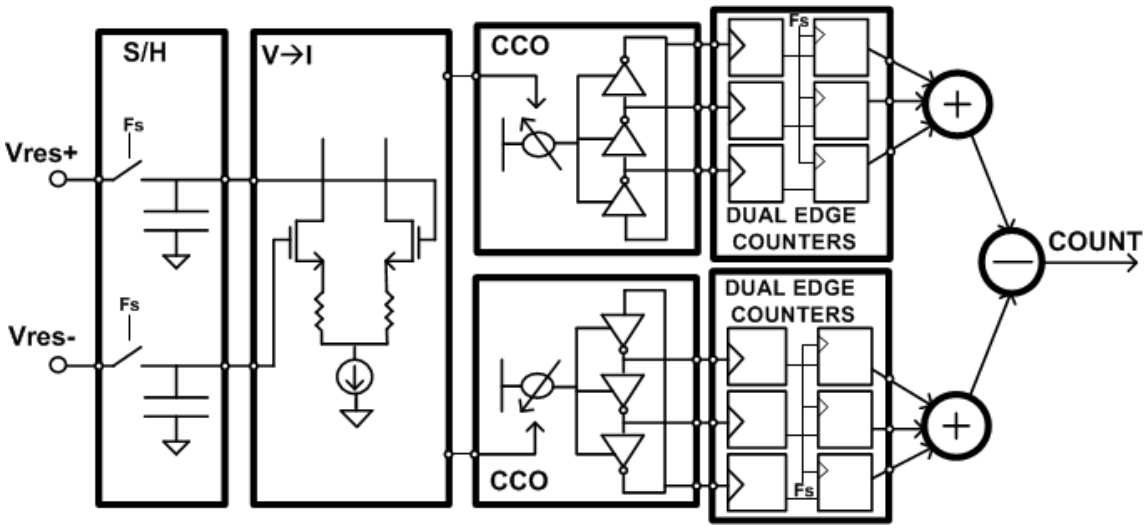


Figure 4.8: Block diagram of second stage

The gating of the VCO output to the counter helps solve the metastability problems which arise when counter outputs are latched on to registers.

The stage 1 samples in φ_1 phase and amplifies in φ_2 phase. Stage 2 samples in the φ_2 phase and integrates in the φ_1 phase. The sampling capacitance of the second stage is chosen as ¼ of the first stage and equals 300fF. Even with a gain of only 2 the second stage contributes smaller thermal noise than the first stage. Second stage sampling phase (φ_2) noise equals $\sqrt{2kTC_s}$ = 166μV(rms) which gives 78dB of SNR when referred to input. But in counting phase there is no noise foldover because of the averaging action provided by counting for 0.5Ts period. The smaller sampling capacitor helps reduce the power consumption on the first stage amplifier by reducing its loading.

Figure 4.9 illustrates the timing for the second stage. In this design the VCO sees a step input when switch φ_2 is turned 'on'. The VCO needs to settle to its new frequency before the counter starts counting, which is the rising edge of signal RZ in the Figure 4.9. The VCO settles to the new frequency at the same time as the first stage is generating the residue. This means that the VCO gets at most 0.5*Ts for its output frequency to settle. There is slight disturbance on the control voltage of VCO when the switch S_1 turns off because of clock feedthrough and charge injection. This disturbance settles out during the time t_2 between the φ_2 falling edge and RZ rising edge. The gating of the VCO output to the counter serves two purposes. First it helps reduce power consumption by clocking the counters for half the time period. Secondly it helps solve the metastability problem which arises when the counter outputs are being latched on the registers in the φ_2 phase. Without the gating logic the VCO output clock is asynchronous with respect to the ADC sampling clock.

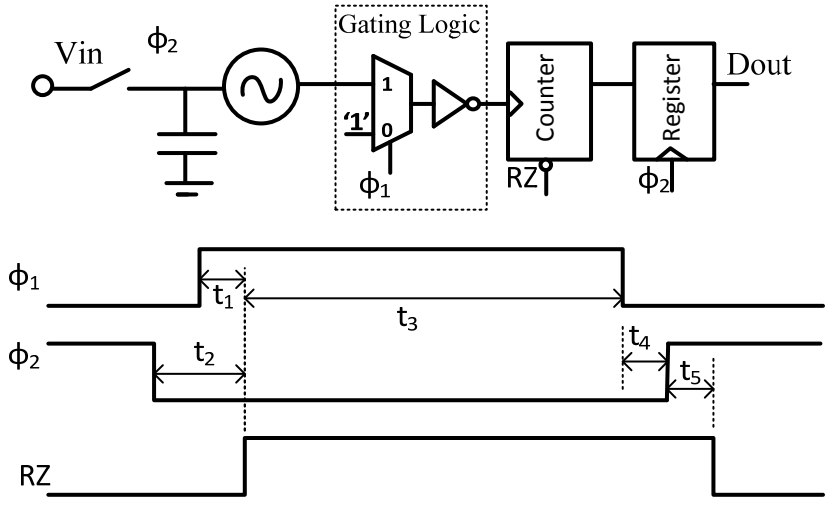


Figure 4.9 Illustration of second stage timing

The counters are updated on both the rising and falling edge of the VCO output. The metastability happens when the registers try to latch the counter output at the same time as it is getting updated. The errors because of metastability can be very large and leads to corrupted digital output. By gating the VCO output we make sure that registers latch the counter output only after they are stable.

The time t_4 between the falling edge φ_1 of rising edge of φ_2 in Figure 4.9 needs to be large enough to account for delay in gating logic block (t_{d1}), the counter delay ($t_{d\_counter}$) and the setup time for the registers i.e

$$t_4 >= t_{d1} + t_{d\_counter} + t_{setup} \quad (3)$$

If the above requirement is satisfied there will not be any metastability problems when the counter outputs are latched on the registers. Effective time available for counting is between the rising edge of RZ and falling edge of φ_1 shown as t_3. This time determines the count which is obtained from the second stage which in turn determines the second stage resolution. The count obtained is given by

$$Count = t_3 * f_{osc} * 6 \quad (4)$$

Here f_{osc} is the differential oscillation frequency and factor of 6 is because of the fact that we are counting both edges of three phases of ring oscillator. The timing t_1 in the figure accounts for the delay in the gating logic block and t_5 is needed to account for the hold time of the registers. For a given clock frequency the aim is to maximize t_3 which means that we need to minimize t_2 and t_4. This means that we should minimize the counter delay and improve the VCO step response time. In the following sections we analyze the design of different blocks in the second stage the VCO, counter and adders.

4.2.1 VCO Design

Figure 4.10 shows the schematic of the differential VCO used in the second stage. The key specifications for this are noise, linearity, gain, and step response time. All these requirements need to be satisfied with the overall aim of minimizing the power consumption. Another requirement on the VCO is the differential frequency stability across temperature. We will look at each of these requirements on the VCO and analyze the performance of the VCO shown in Figure 4.10.

Linearity and Gain: The linearity requirement on the VCO is relaxed significantly for this architecture because 4 MSB bits are obtained from the first stage itself. The VCO sees only a small swing (+/-V_{REF}/8) at its input. Another benefit of the architecture is that the VCO is differential in frequency domain which leads to the cancellation of second harmonic [65,68] in the V-F transfer function. Still the VCO needs to be at least 8-bit linear to obtain 12 bits of linearity in the overall ADC.

VCO gain (GHz/V) determines the resolution of the second stage and is a critical parameter. COUNT_FS is the count obtained from the second stage when input to the VCO is V_{REF}/8. The higher this count higher the resolution obtained from the second stage. There are a couple of ways to obtain a higher count from the VCO. First option is to increase the number of phases in the ring VCO. This leads to higher power consumption if we want to maintain the same oscillation frequency. Another option is to increase the VCO gain (GHz/V) so that for the same reference input it will produce higher differential frequency. For a fixed quiescent oscillation frequency the increase in differential frequency doesn't lead to higher power consumption. The increase in

oscillation frequency of one CCO is accompanied by decrease in speed of another CCO keep the power consumption constant. The aim of the design should be to maximize the VCO gain for a fixed quiescent oscillation frequency.

Let's analyze the VCO circuit in Figure 4.10 initially ignoring the current sources shunting the device M2. The linearity of this circuit is first limited by non-linearity of the input transconductor and next by the nonlinearity in the current to frequency transfer function. For the input transconductance with degeneration (as in this design) the third order distortion is given by [114]

$$HD3 = \frac{1}{32}\left(\frac{1}{1+gm_1R_s}\right)^2\left(\frac{V_{in}}{VDsat}\right)^2 \quad (5)$$

Increasing the source degeneration reduces the third harmonic distortion. One of the parameters to optimize is the voltage drop across the degeneration resistor because in low voltage design voltage headroom is quite limited.

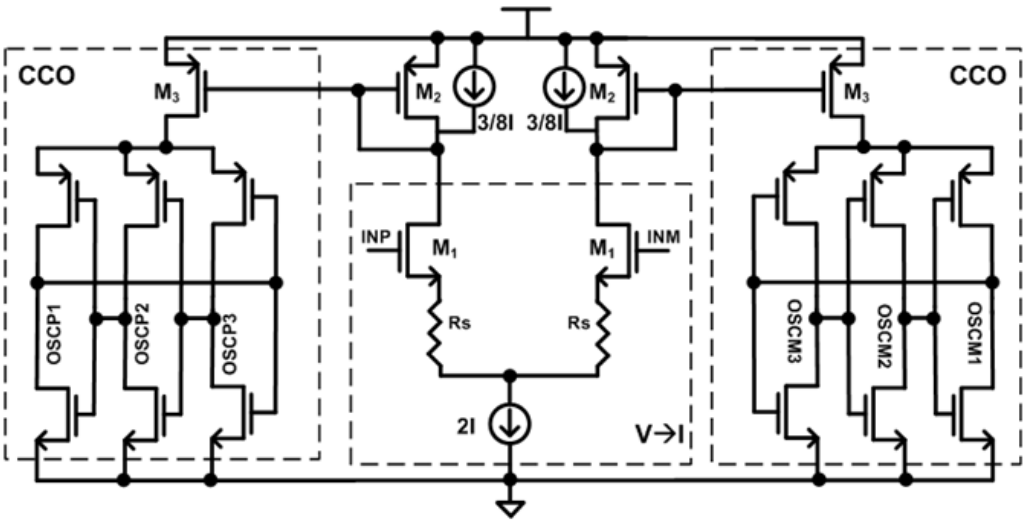


Figure 4.10: Differential VCO schematic

Figure 4.11 shows the simulated linearity of the VCO versus the degeneration voltage for a fixed tail current (2I) and 125mV of differential input. As it can be seen from the figure after about 250mV of degeneration the linearity starts getting limited by current to frequency transfer function and it doesn't help to increase degeneration further. One of the issues with increased degeneration is the accompanied drop in VCO gain. Figure 4.11 also shows the plot of VCO gain versus the degeneration voltage for a fixed bias current. The reduction in VCO gains causes a smaller count for a given input reducing the resolution of the second stage.

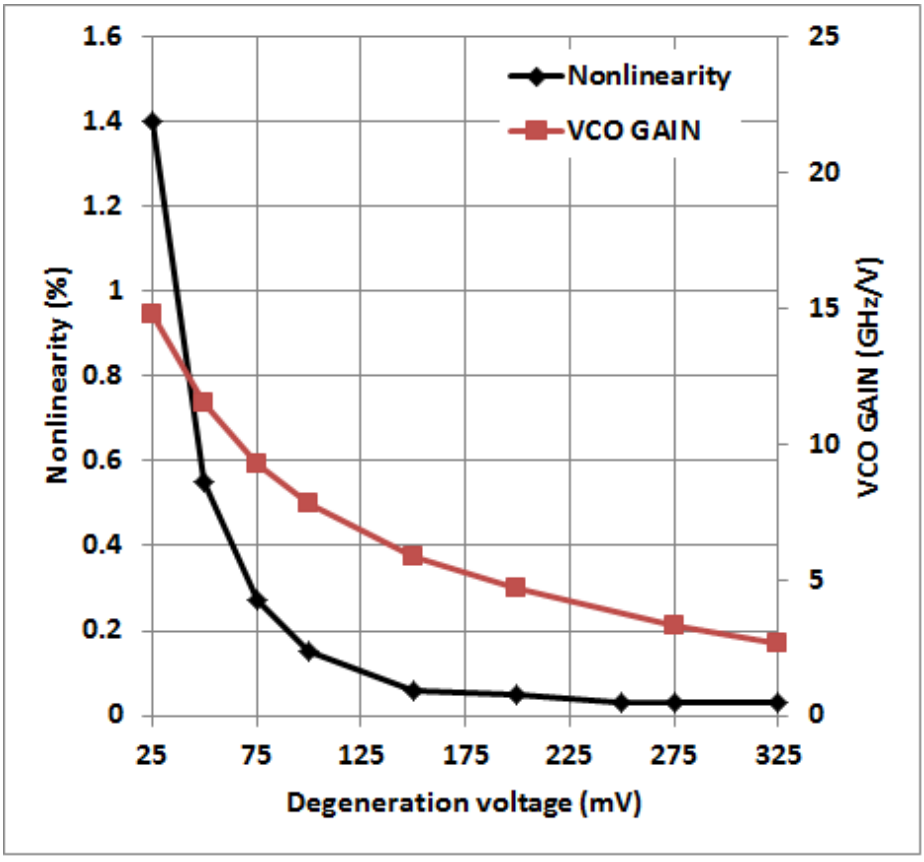


Figure 4.11: Effect of degeneration on VCO nonlinearity and gain

Adding the current source in parallel with diode connected devices M_2 as shown in Figure 4.10 improves the VCO gain. The amount of current that can be shunted depends on the linear input range required. The linear differential input range reduces as shunt current is increased. For this prototype 3/8I was chosen as the shunt current and 100mV of degeneration was used in the differential pair. Figure 4.12 shows a simulation of output frequency versus the differential input voltage. Simulation shows a nonlinearity of better than 9 bits and a gain of 11.3GHz/V.

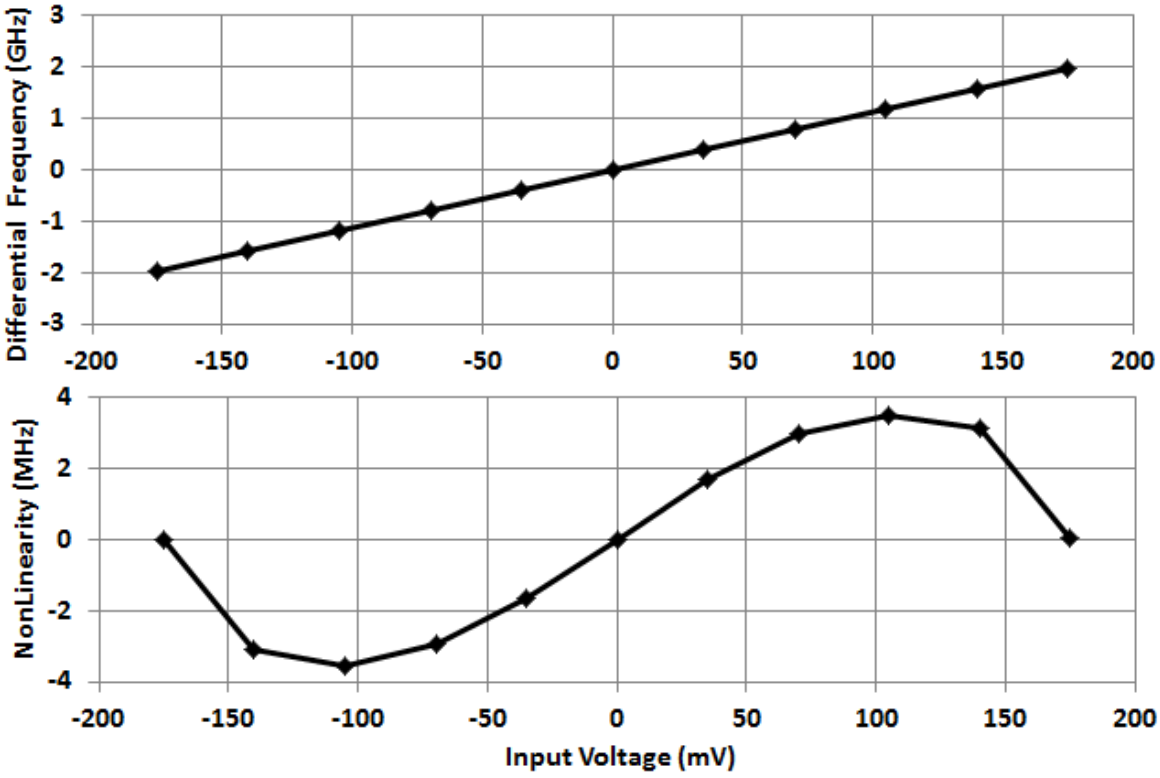


Figure 4.12: VCO output and its nonlinearity

VCO step response: VCO in this design sees a step at its input every clock period. The VCO settles to its new frequency at the same time as first stage amplifier is settling and the second stage sampling network is tracking the residue. Assuming that only bandwidth limitation was from the VCO we can get 0.5*Ts for the VCO to settle. In actual case the residue amplifier from the first stage has finite bandwidth and may limit the settling of the VCO. Another secondary requirement comes from the disturbance on the VCO input node when the second stage input sampling switch is opened. It is desired that there is no non-linear settling component remaining after time t_2 in Figure 4.8. For the VCO design in Figure 4.9 the settling limitations comes from mirror pole formed by the device M_2.

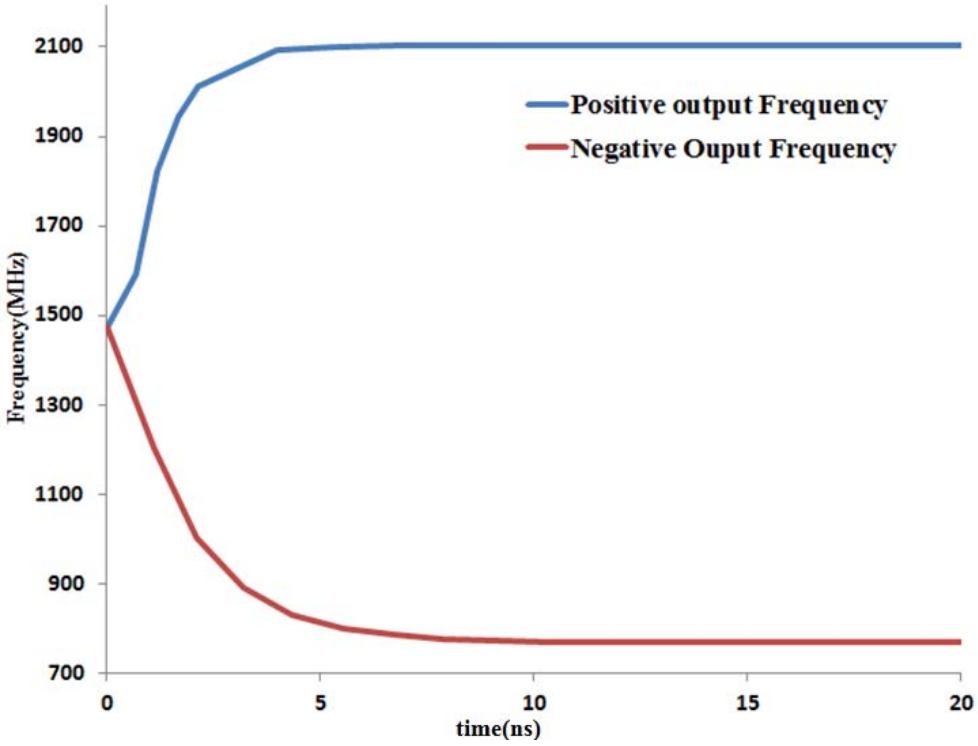


Figure 4.13: VCO step response

The aim of the design is to move this pole as far away as possible. But another design criteria flicker noise (discussed next) prevents use of small channel length devices. The final design has the mirror pole at 140MHz. Figure 4.13 shows the VCO response to an input step from 0 to +125mV. The differential output frequency settles to within 0.1% in 13ns.

Noise Analysis:

The VCO output of interest in this design is its frequency and we are interested in determining the frequency deviation or frequency stability. The frequency is measured by counting the edges of the VCO during the time t_3 in the Figure 4.8 which is approximately equal to 0.5*Ts. Let the count obtained from the VCO in this period be 'N' then

$$N = 6*Fosc*0.5*Ts \quad (6)$$

Here the factor of 6 accounts for the fact that there are three phases in the ring oscillator and we are counting on both the edges. We need to analyze the effect of noise on the count N that we obtain from the VCO. Let us consider a carrier ($\omega = 2\pi F_{osc}$) which is frequency modulated by a single sinusoidal noise component at frequency f_m

$$y(t) = \sin[\omega t + Msin(2\pi f_m t)] \quad (7)$$

Here M is the modulation index and is given by $M = \frac{\Delta f}{f_m}$ where Δf is the peak frequency deviation.

Let φ_1 denote the phase at t_A (beginning of period t_3) and φ_2 denote the oscillator phase at t_B (the end of the period t_3). From (7) we can write

$$\varphi_1 = \omega t_A + M sin(2\pi f_m t_A) \qquad \varphi_2 = \omega t_B + M sin(2\pi f_m t_B) \tag{8}$$

$$\varphi_2 - \varphi_1 = \omega(t_B - t_A) + M[sin(2\pi f_m t_B) - sin(2\pi f_m t_A)]$$

Since the phase is quantized with a resolution of π/3, the count 'N' obtained in the time $t_3 = t_B - t_A$ is given by

$$N = \frac{3}{\pi}\omega(t_B - t_A) + \frac{3M}{\pi}[sin(2\pi f_m t_B) - sin(2\pi f_m t_A)] \tag{9}$$

Using (6) we can estimate the average oscillation frequency in time t_3 by dividing (9) by $6t_3 \sim 3T_s$

$$\overline{Fosc} = \frac{N}{3Ts} = F_{osc} + \frac{M}{\pi T_s}[sin(2\pi f_m t_B) - sin(2\pi f_m t_A)]$$

$$\overline{Fosc} = F_{osc} + \frac{2M}{\pi T_s}[cos(\pi f_m(t_B + t_A))]\sin(\pi f_m T_S/2) \tag{10}$$

Substituting $M = \frac{\Delta f}{f_m}$ we get

$$\overline{Fosc} = F_{osc} + \Delta f[cos(\pi f_m(t_B + t_A))]\frac{\sin(\pi f_m T_S/2)}{\pi f_m T_s/2} \tag{11}$$

The cosine term in expression (11) has a peak value of one. The last term in the expression is a sinc filter with nulls for $f_m = 2/T_s$. This sinc filter effectively works as first order antialias filter with a cutoff frequency of 0.5/Ts. This low pass filter will filter out any noise from voltage to current converter also. This means that for the entire VCO we are only interested in the frequency noise till 0.5/Ts bandwidth.

The power spectral density of frequency noise $S_f(f_m)$ is related to power spectral density of phase noise $S_\varphi(f_m)$ by [115]

$$S_f(f_m) = f_m^2 * S_\varphi(f_m) \tag{12}$$

The frequency deviation over finite baseband bandwidth say $f_{m1} - f_{m2}$ is given by

$$F_n^2 = \int_{f_{m1}}^{f_{m2}} S_\varphi(f_m)\, f_m^2\, df_m \qquad (13)$$

Let the VCO gain be k (Hz/Volts) then the VCO input referred noise can be obtained as F_n/k. The key difference between the frequency noise and phase noise is that frequency noise does not fall off as $1/f^2$ with increasing frequencies. This means that for thermal noise sources frequency noise will be flat and will be significant even at large offset frequencies. Figure 4.14 shows a representative PSD for frequency noise. We can see that $1/f^3$ region in the phase noise plot becomes 1/f region in the frequency noise plot , $1/f^2$ region becomes flat and the white phase noise spectrum actually starts rising in the frequency noise plot.

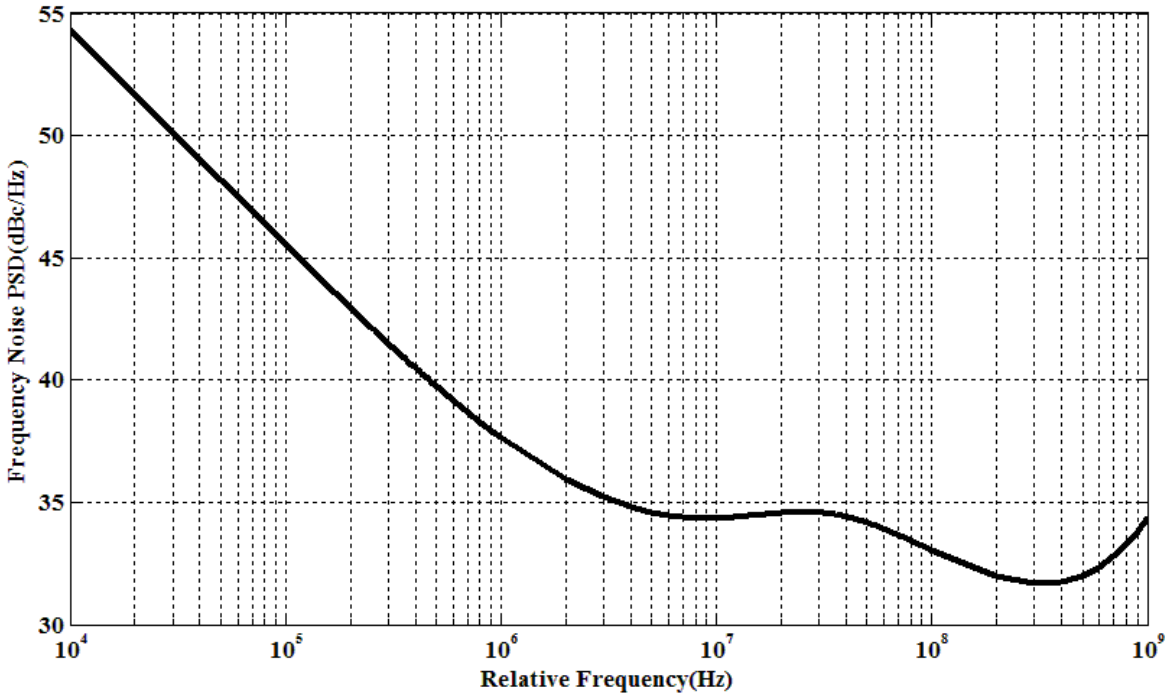


Figure 4.14: Typical frequency noise power spectral density

For the VCO design in Figure 4.9 the noise analysis can be divided in two parts. First part consists of the noise from the voltage to current converter and the current source itself (v_{n1}) and second part consists of noise from the oscillator (v_{n2}). v_{n1} can be analyzed using traditional small signal noise analysis whereas v_{n2} can be estimated by running PSS/ Pnoise simulations to obtain phase noise density and then using (8) to obtain the integrated frequency noise. Figure 4.15 shows half –circuit of the setup used to analyze the noise v_{n1}. Here the VCO current is injected into a noiseless resistor (R_{sim}) instead of the oscillator to determine the noise from the circuit. Rsim is chosen to be equal to $R_{sim} = 1/MG_{m1eff}$

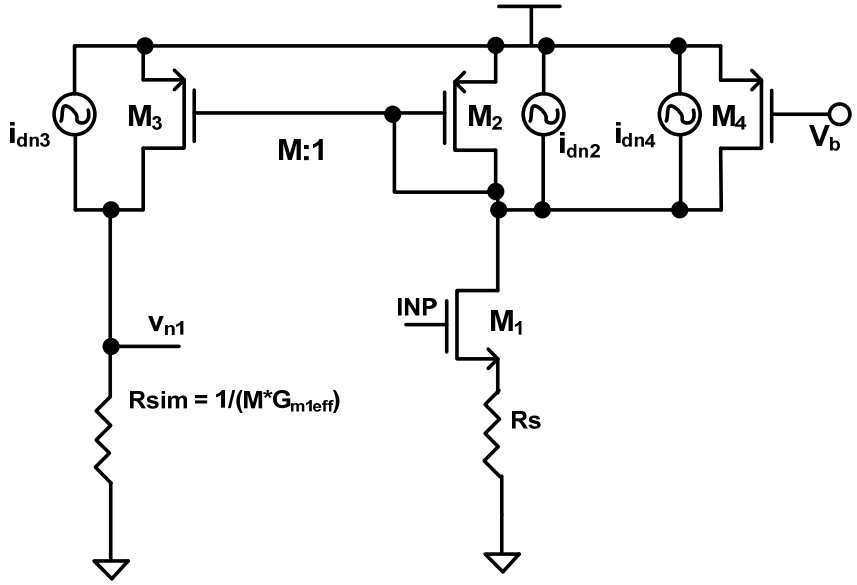


Figure 4.15 : Simulation setup for simulating noise v_{n1}

Here M is the mirroring ratio and G_{m1eff} is effective transconductance of the input differential pair and is given by

$$G_{m1eff} = \frac{g_{m1}}{1 + R_s g_{m1}}$$

Simulations indicate the noise v_{n1} is dominated by flicker noise (about 60%) with total integrated noise being 110μVrms. To estimate v_{n2} the ring oscillator was simulated using PSS and Pnoise. Figure 4.16 shows the phase noise plot obtained from the simulations and Figure 4.17 shows the frequency noise plot derived from it. From the Figure 4.17 it can be seen that in the bandwidth of interest (~20MHz) the noise is dominated by flicker noise. The frequency noise of the oscillator in 20MHz band is about 0.37MHz which translates to a VCO input referred noise of about 31μVrms. Combining v_{n1} and v_{n2} and accounting from noise for both sides of differential VCO circuit the total simulated noise from the VCO is 161μVrms which corresponds to 79dB SNR when referred to ADC input.

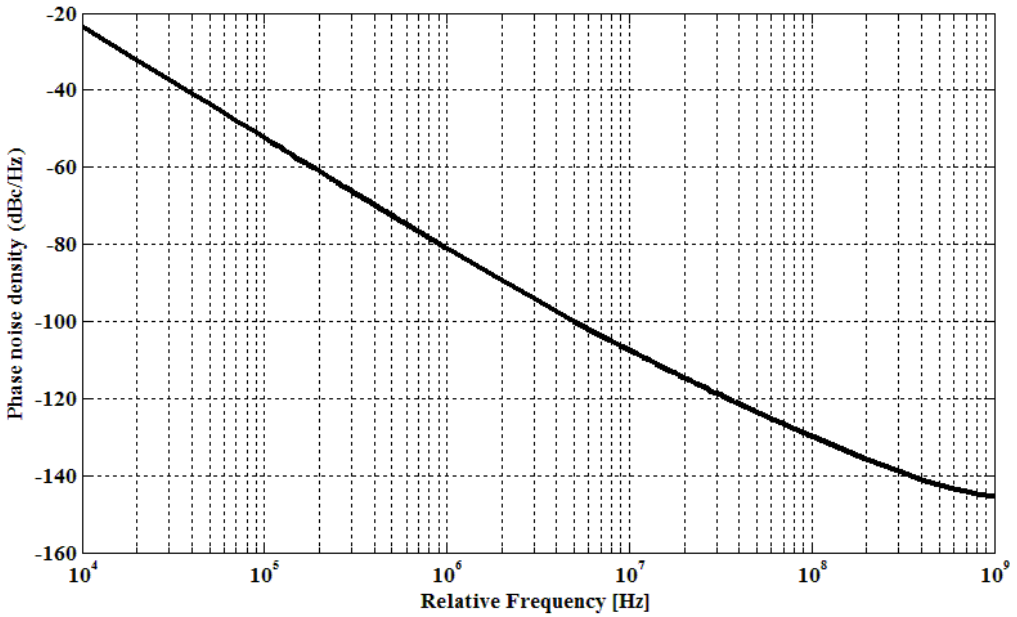


Figure 4.16: Oscillator phase noise density plot

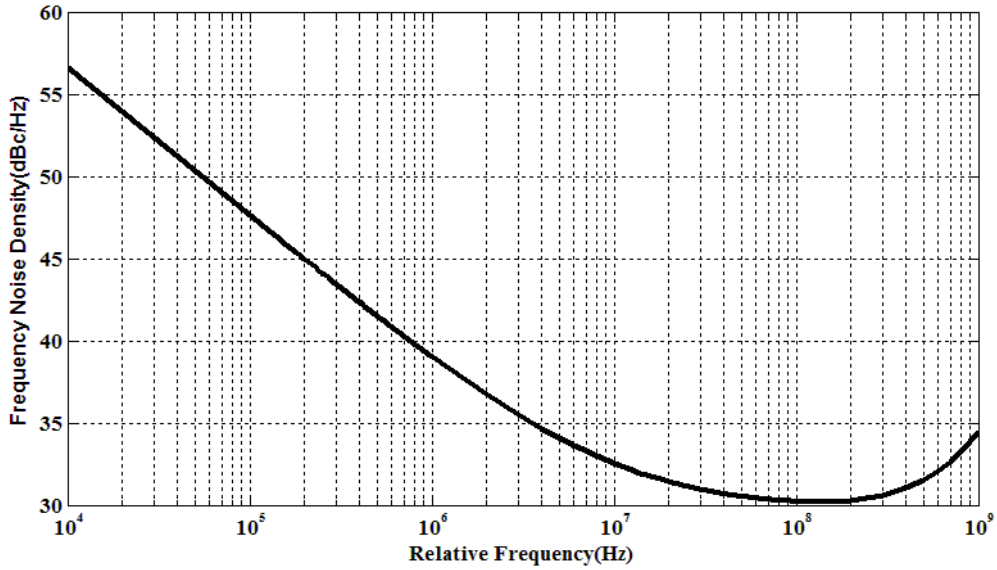


Figure 4.17: Oscillator frequency noise density plot

4.2.2 Counter Design

Since the majority of power in the ADC is consumed by counters which are clocked at high speeds (>1GHz) it is essential to optimize the design of counters. Figure 4.18 shows the traditional counter design approach using D- flip flops illustrated for 4 bits. Figure 4.18(a) shows a ripple counter in which the clock input only goes to one D-Flip flop. The second flip-flop is clocked by the inverted output of first DFF, third is clocked by inverted output of second DFF and so on. Since the clock input to the later stages is delayed all the outputs are not available at the same time. Let T_{CQ} denote the clock to output (Q) delay of a single flip flop. For an N-bit ripple counter the the clock to Q delay $T_{CQ\_CNT} = N*T_{CQ}$ which may not be acceptable for the design. The synchronous counter in Figure 4.1(b) solves this problem by clocking all the flip-flops by the same external clock.

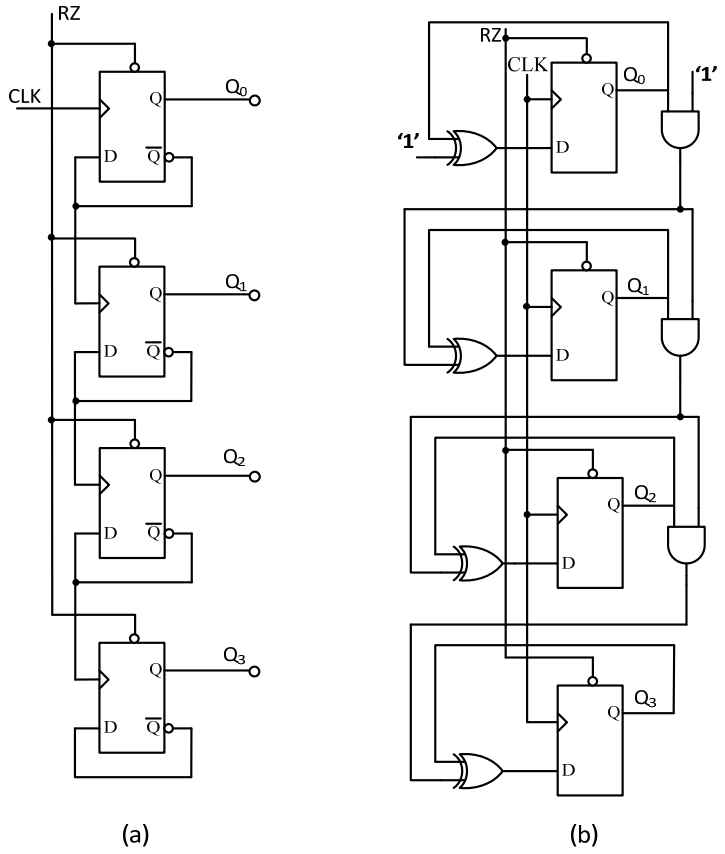


Figure 4.18: (a) Ripple (asynchronous) counter (b) Synchronous counter

The delay of the counter in this case is same as the delay from a single flip-flip T_{CQ}. The problem with this approach is that all the flip-flops are clocked at very high speed leading to significant power consumption.

To design a N (=9) bit counter we used a two stage counter as shown in Figure 4.19. The first stage is a N_1 bit ripple counter and second stage is a N_2 bit synchronous counter, such that $N = N_1+N_2$. The delay of this two stage counter is equal to $(N_1 + 1)*T_{CQ}$ and approaches that of a ripple counter for $N_1 = N - 1$ and of a synchronous counter for $N_1 = 0$. Figure 4.20 shows the power consumption of two stage counter as

N_1 is varied for a 9 bit counter. As can be seen from the figure significant power savings can be obtained For N_1 = 2 or 3 and after that the power savings gradually taper off. For this design we used N_1 =2 to strike a balance between power consumption and the counter clock to Q delay.

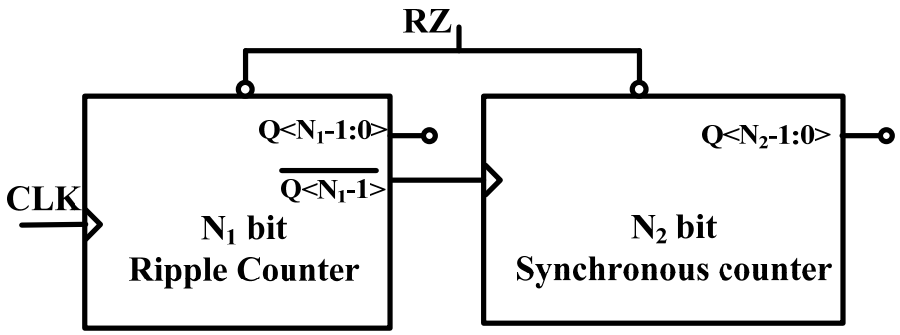


Figure 4.19 Two stage Counter

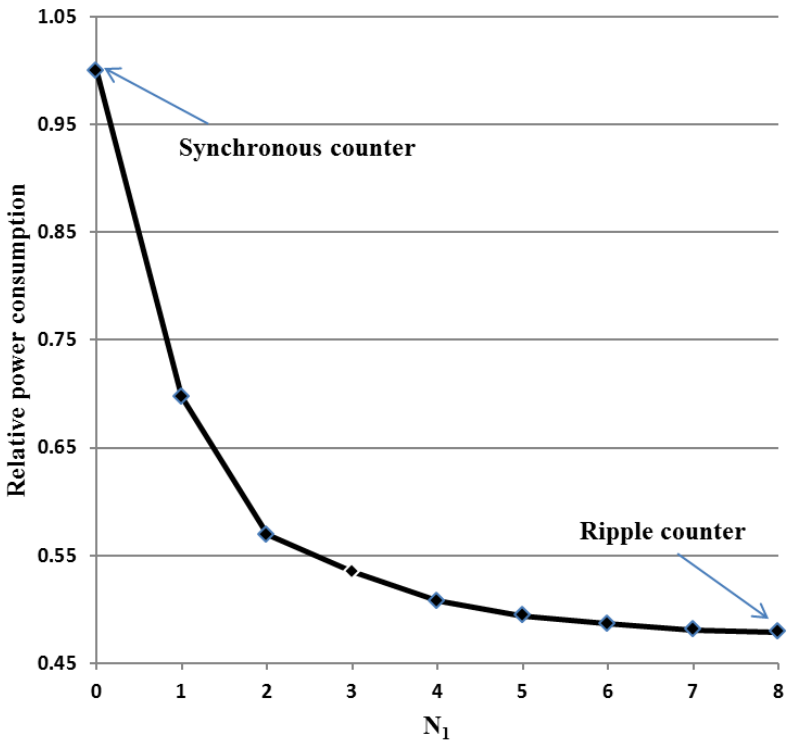


Figure 4.20 Power Consumption of a two stage counter

Since we need to count on both the edges of all the clock phases of the ring oscillator we will need a total of 12 counters. Further optimization is done by building a dual edge counter which counts on both the edges, reducing the total number of the counters to six. Figure 4.21 shows the implementation of the dual edge counter in this prototype.

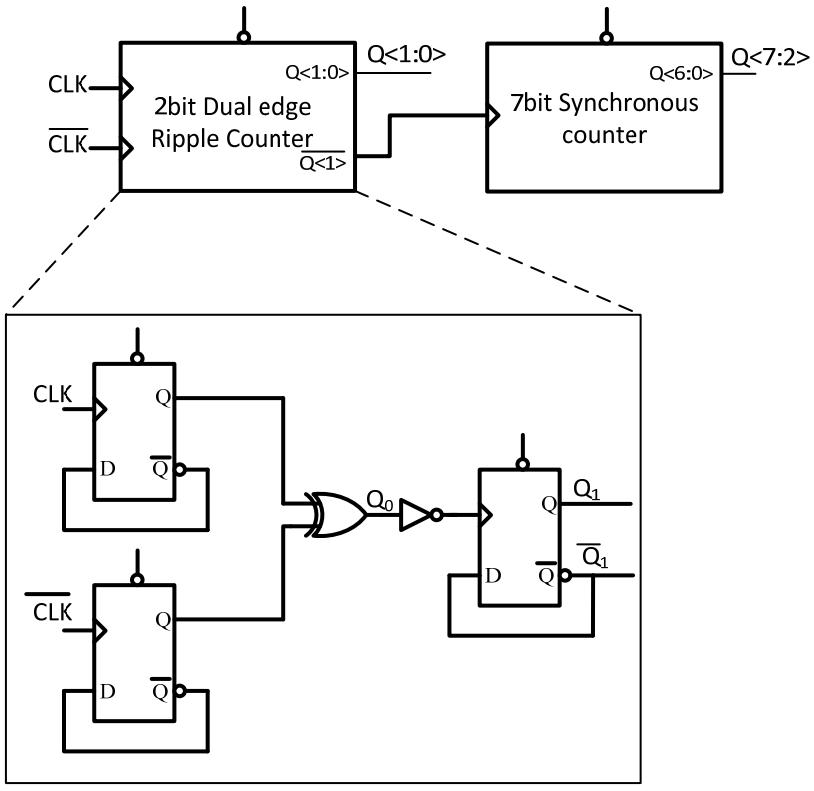


Figure 4.21 Two stage counter with a dual edge counter in first stage.

4.2.3 Adder Design

The adder propagation delay is not very critical in this design. The logic path has two adders and one subtractor in cascade and we have ~0.4*Ts of clock cycle for the data to propagate. At 20MHz clock this is about 20ns of total propagation time giving about 6.7ns for each adder. A simple carry select adder shown in Figure 4.22 is implemented for this design.

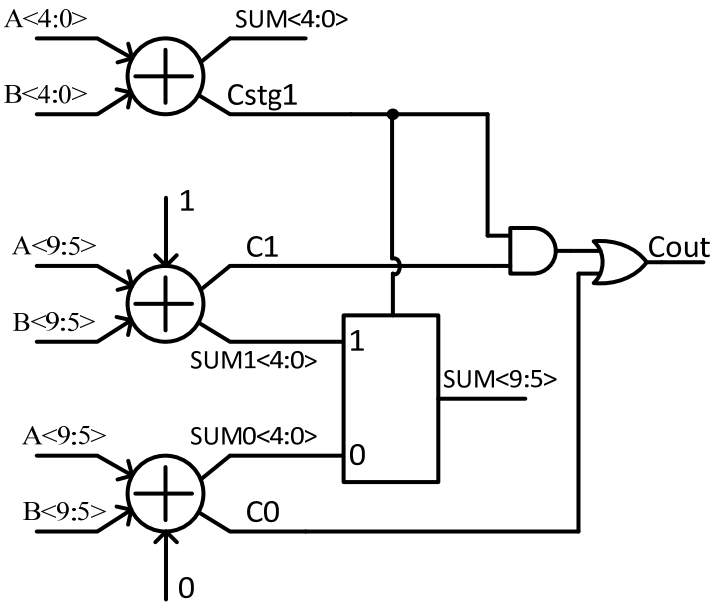


Figure 4.22 Carry select adder

4.2.3 Divider

The ADC needs a divider to properly scale the second stage output. The ADC output is given by

$$DOUT = 256 * STAGE1\_OUT + 128 * \frac{COUNT}{COUNT\_FS} \qquad (14)$$

This division by COUNT_FS is not built on the prototype chip. The divider/adder can easily be integrated. Synthesis of this block in 65nm process shows an area of $0.02mm^2$ and power consumption of 12μW, when running at 20MHz.

4.3 Conclusion

In this chapter we presented design of a two stage ADC with time domain second stage. The ADC architecture reduces the power consumption on the first stage by using a low gain single stage opamp. We also presented the design of a linear VCO which satisfies the noise and settling requirement for this architecture.

Chapter 5 Prototype and measured results

5.1 ADC die and package

The ADC described in the previous chapter was fabricated in Texas Instruments 65nm CMOS process. The test-chip die shown in Figure 5.1 was shared by multiple designs. The hybrid ADC occupies the small area in the top-right corner. The bond pads for the ADC were shared with another ADC on the die. The digital outputs of the ADC had to be routed the entire length of the chip to reach the bond pads. Figure 5.2(a) shows the zoomed in die photo highlighting the key blocks in the ADC. Figure 5.2(b) shows the layout snapshot of the ADC.

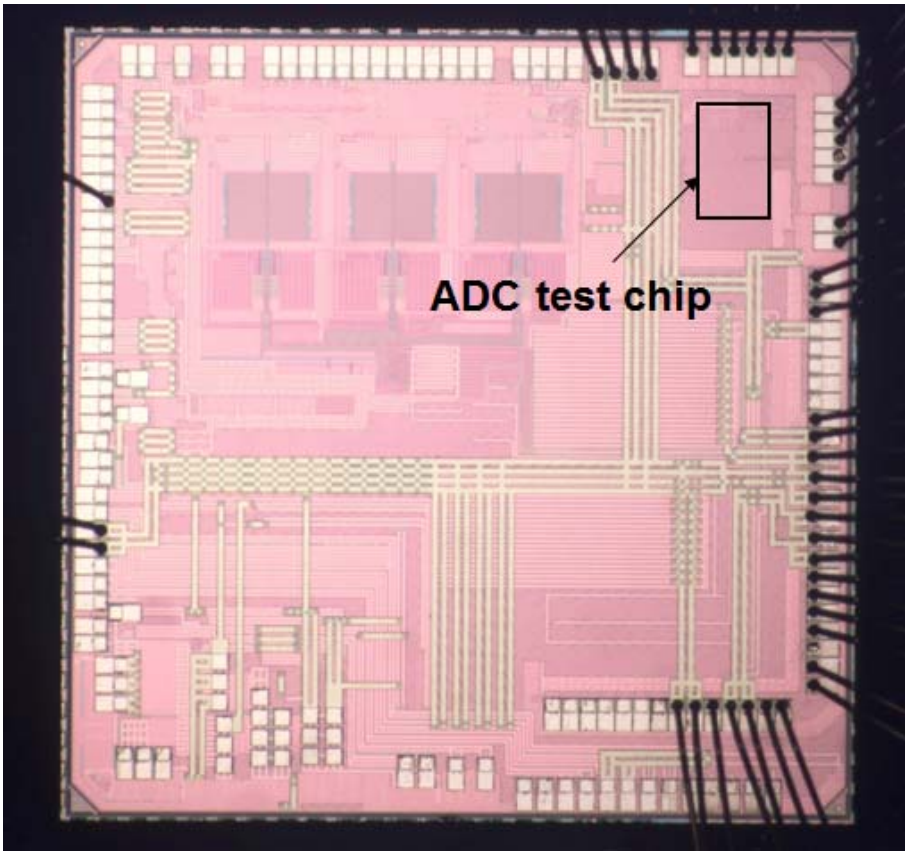
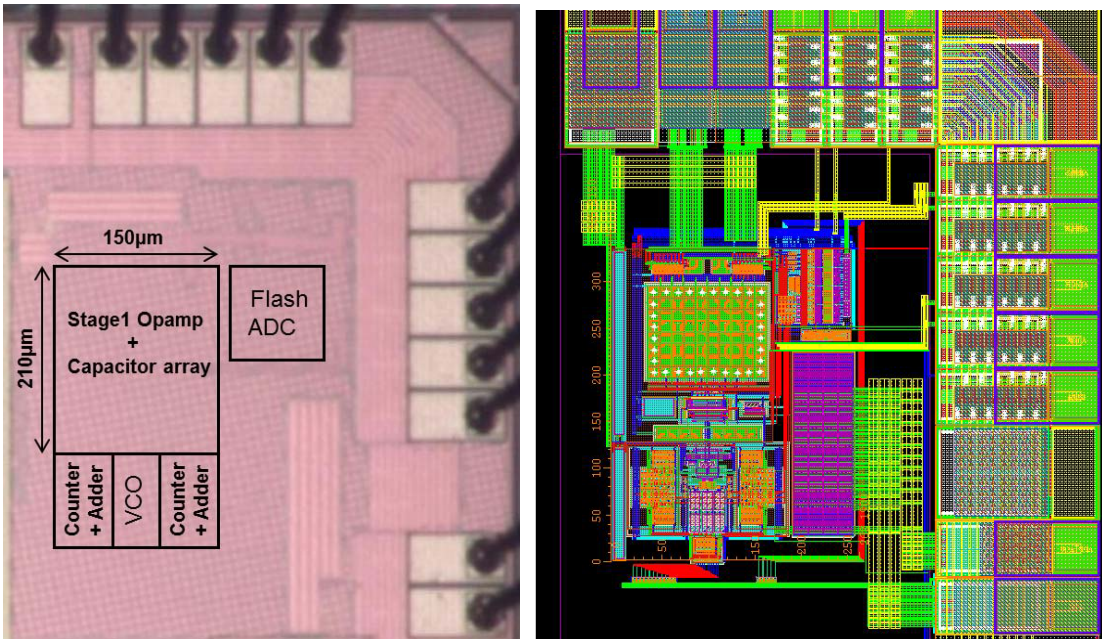


Figure 5.1 Full die photo



(a) (b)

Figure 5.2(a) Die photo (b) Layout snapshot

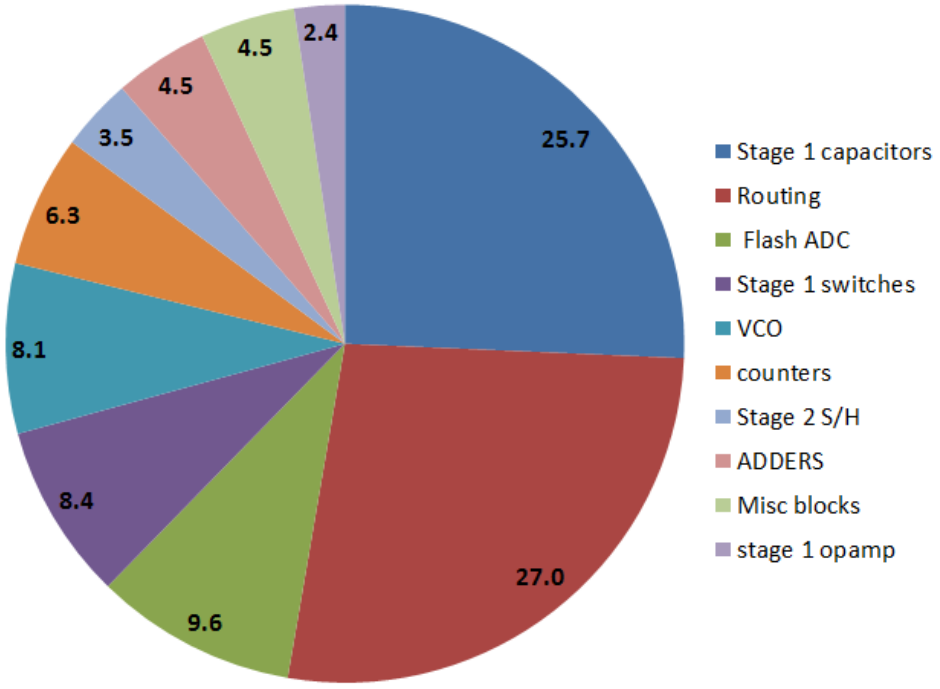


Figure 5.3 Area distributions in percentage

As we can see from the layout the ADC core area is very small ($0.07mm^2$) and is equal to the area of about 8 I/O cells. Figure 5.3 shows the percentage of the area occupied by the different blocks in the die. The second stage occupies an area of less than $0.02mm^2$. The 75 dies were packaged in an 80pin TQFP package using an external vendor VLSIP Technologies Inc. Figure 5.4 shows the mount and bond diagram of the die.

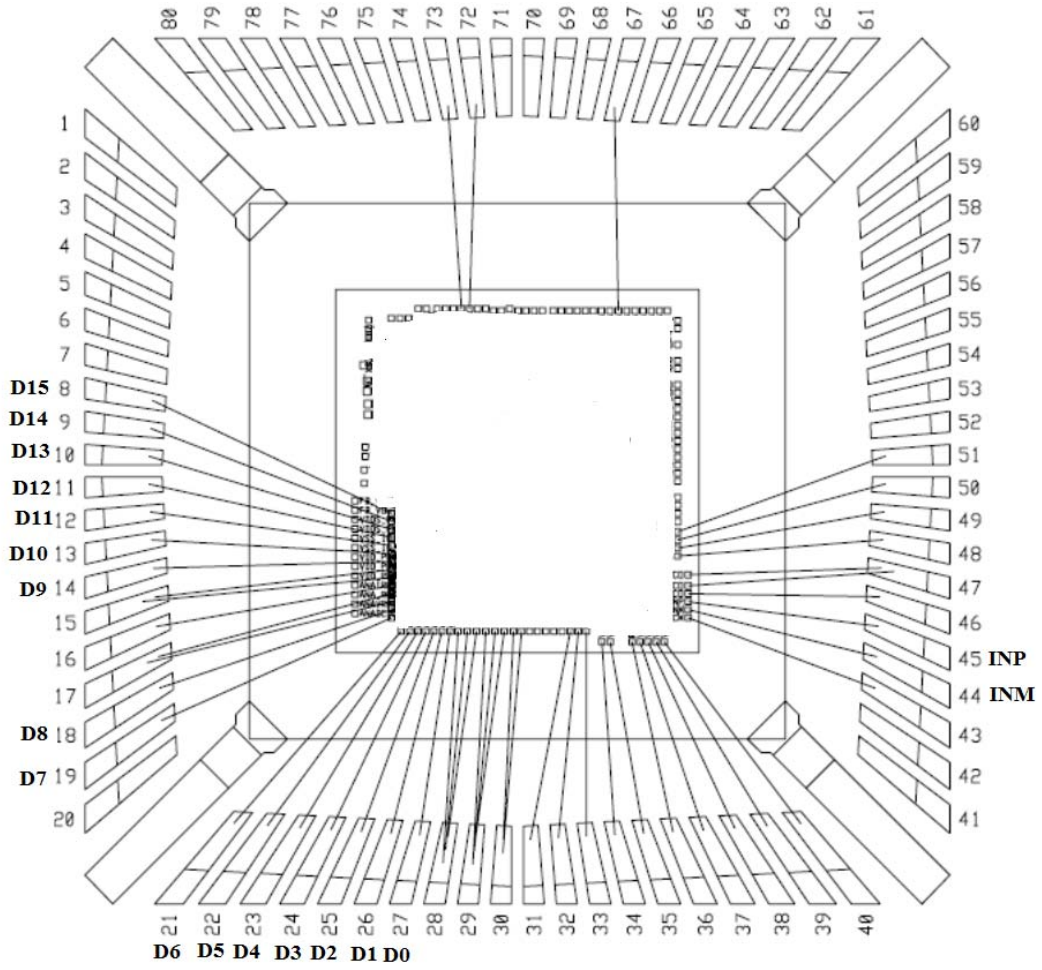


Figure 5.4 Mount and Bond diagram

5.2 Test Setup

To test the prototype chip a four layer board was built. The signals are routed on top and bottom layer. The second layer from top is ground plane and third layer is supply. Figure 5.5 shows a picture of the test board. The socket used on the test board is 80pin TQFP socket from ECT. Figure 5.6 shows a block diagram of the test setup. Hewlett Packard 33120A was used as an input signal source. The output of 33120A was filtered using narrow bandpass filters from TTE Inc to improve the source noise and distortion. The output of the TTE filter is fed to the onboard input drive circuitry built around THS4520 which is a high bandwidth (620MHz) amplifier from Texas Instruments. The reference circuit uses a divider on REF5025 followed by a driver.

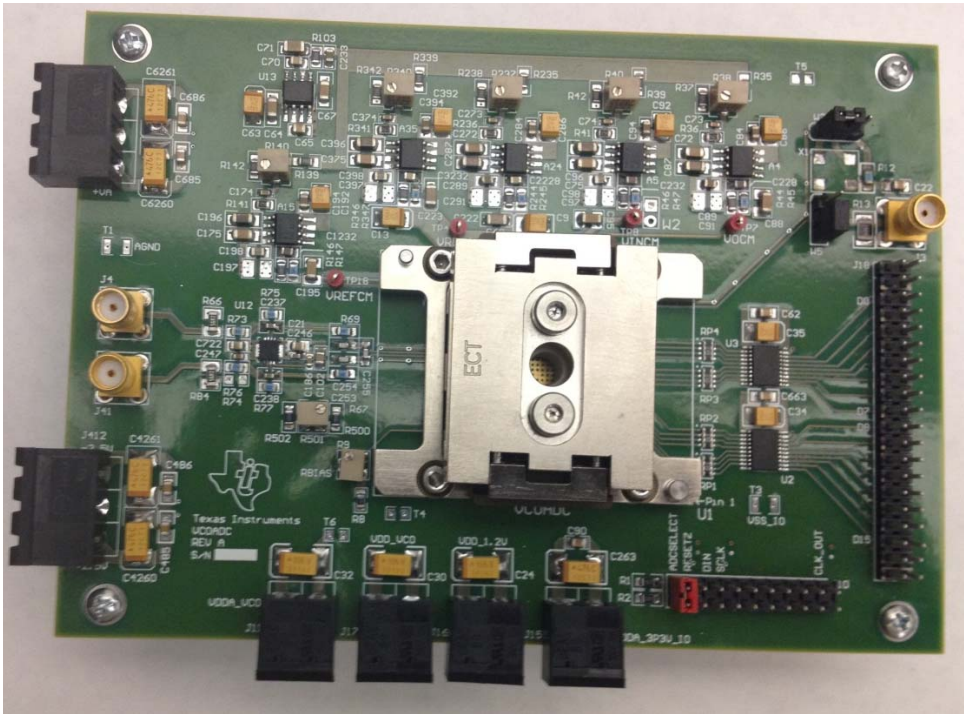


Figure 5.5 The test board

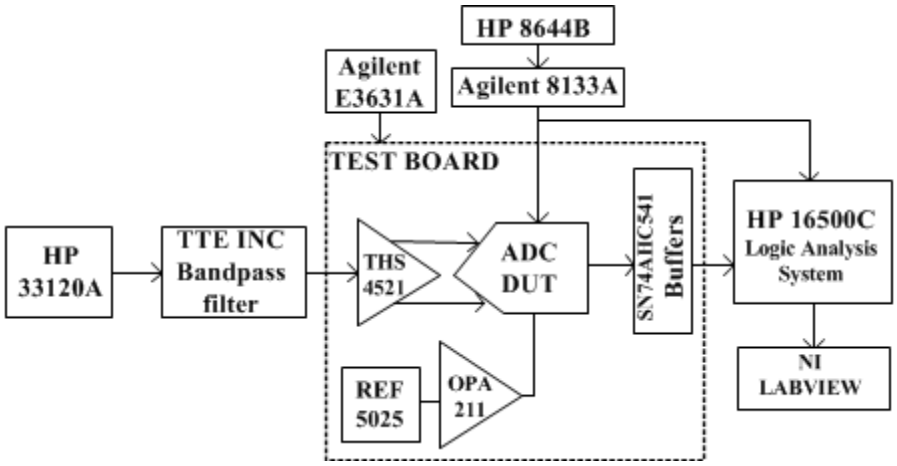


Figure 5.6 ADC Test Setup

The reference driver was chosen as OPA211 for its low noise and high bandwidth (45 MHz). A combination of HP8644B and Agilent 8133A was used as a clock source. HP 16500C Logic analyzer was used to capture the data from the ADC.

5.3 Measured results

Clocked at 20MHz prototype consumes 1.1mW of power of which 0.4mW is consumed by analog blocks (first stage and VCO) and 0.7mW by the digital blocks (mostly counters). The ADC achieves a peak SNDR/SFDR of 63.7dB/76dB in 10MHz bandwidth resulting in an ENOB of 10.3bits and FoM of 44fJ/conv-step. Fig. 5.7 shows the ADC's measured output spectrum for a full scale 2MHz sinusoidal input and a SFDR of 76dB is achieved. Also shown on the plot is SNR/SFDR vs input signal frequency with a minimum SNDR of 63.3dB. Fig 5.8 shows the DNL and INL plot obtained from the prototype. Figure 5.9 shows a plot of VCO nonlinearity obtained from the prototype. A linearity of better than 9 bits is obtained in voltage to frequency transfer function. A summary of chip performance is given in Table 5.1

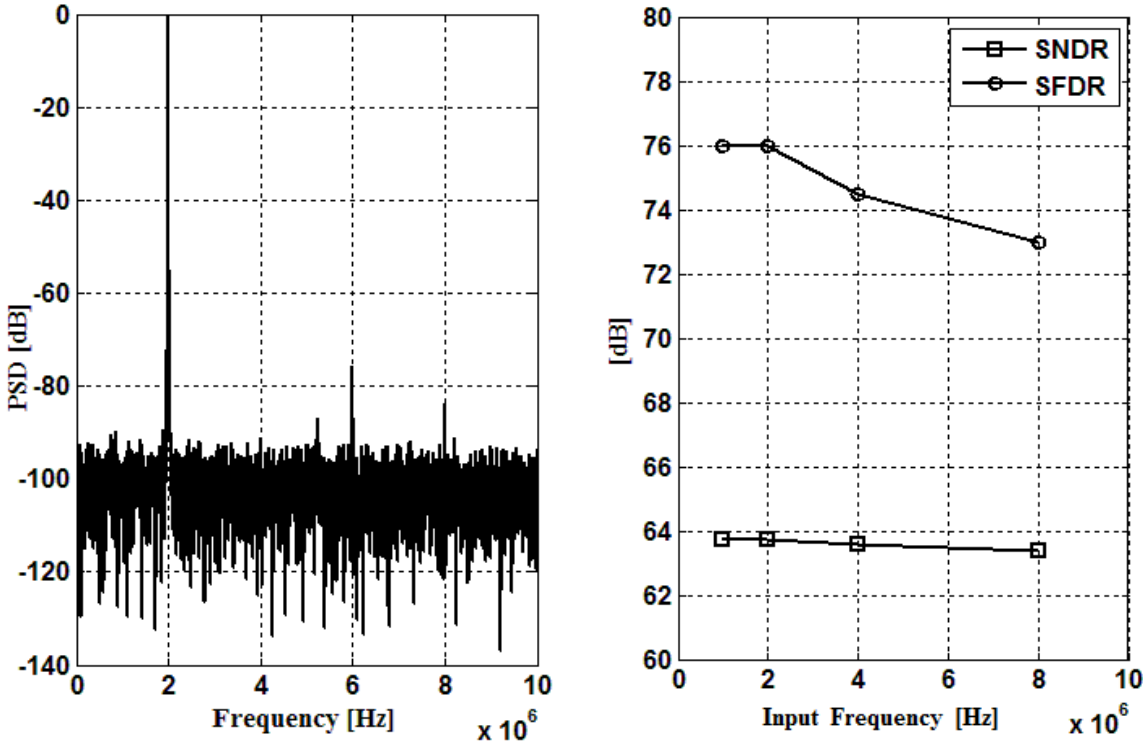


Figure 5.7 ADC output PSD and SFDR/SNDR versus input frequency

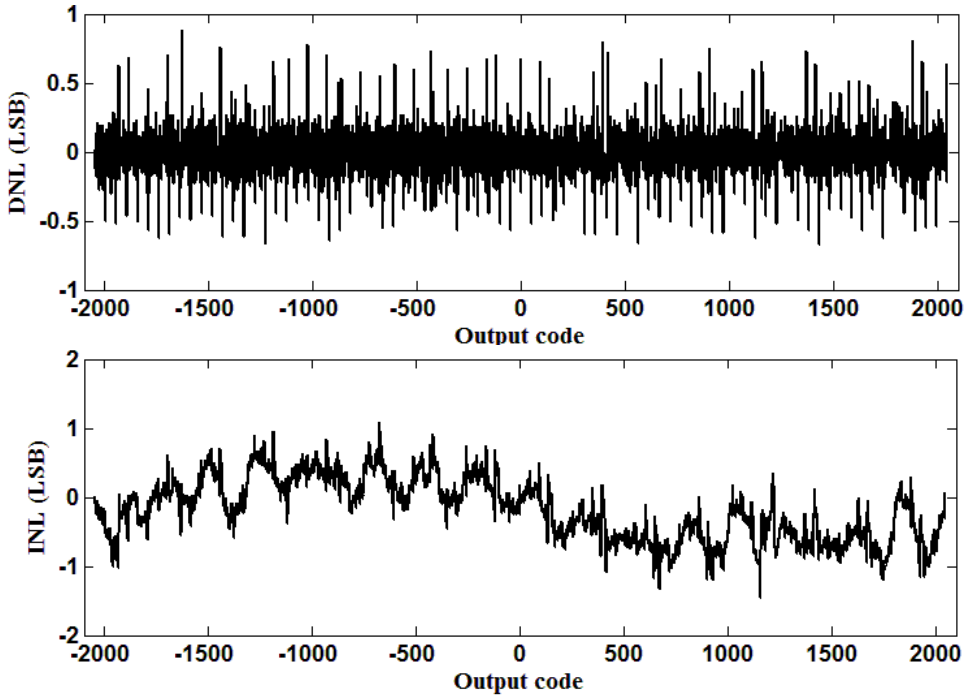


Figure . 5.8: Measured DNL and INL plot at 12 bit level

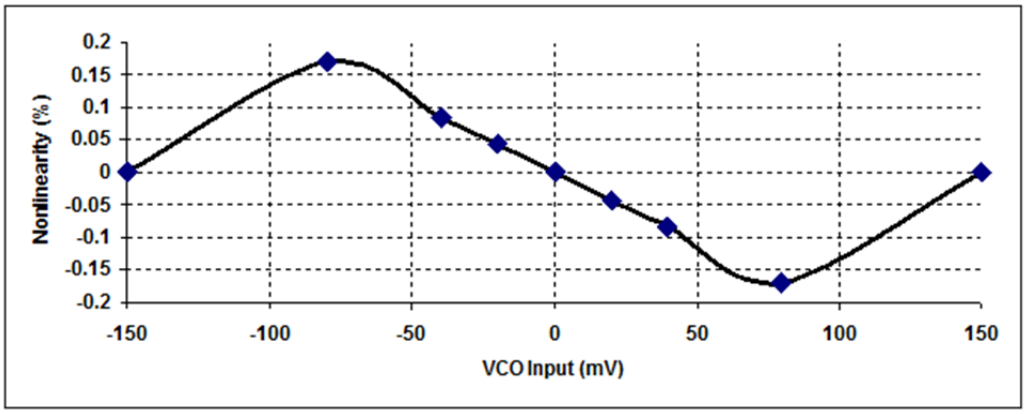


Figure 5.9 VCO nonlinearity plot

Table 5.1 Chip performance summary

Technology (nm)	65
Core Area (mm^2)	0.07
Sampling Frequency Fs(MHz)	20
Bandwidth(MHz)	10
SNDR(dB)	63.7
Power (mW)	1.1

5.4 Comparison with prior art

The ADC performance is compared with the prior art ADC's using a Figure of Merit (FOM) given by

$$FOM = \frac{Power}{2^N * Fs}$$

Where N is the effective number of bits (ENOB) and Fs is the ADC sampling rate.

Figure 5.10 shows a comparison of this work with ISSCC publications from 2010 to 2014 [116]

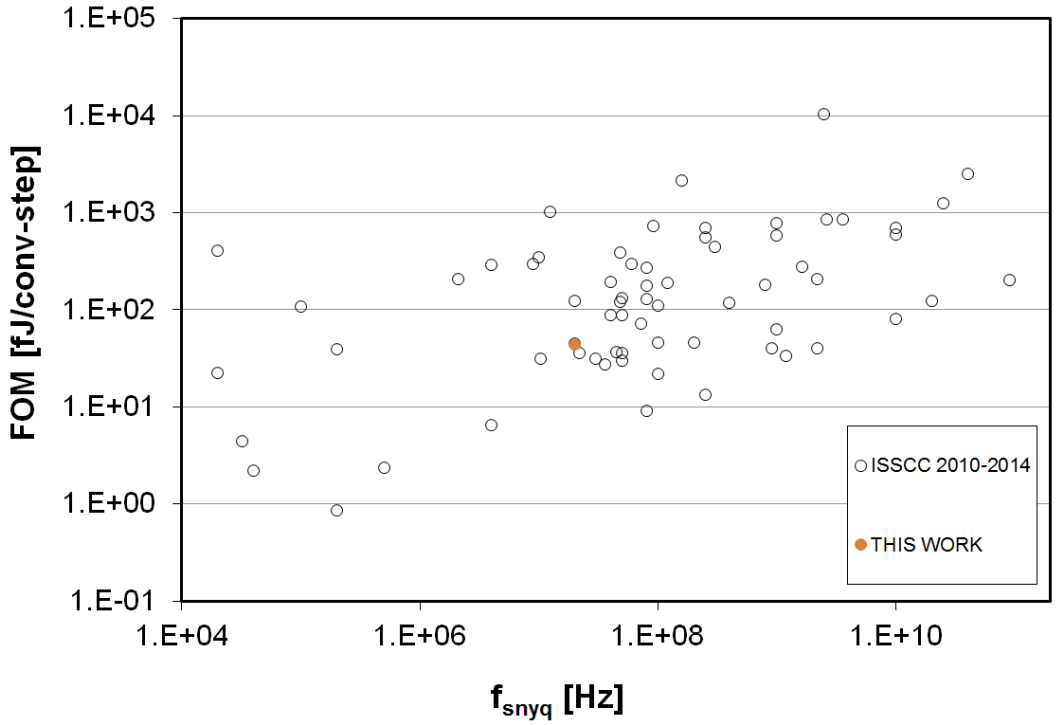


Figure 5.10 Comparison of FOM with ADCs presented at ISSCC

5.5 Conclusion

A fabricated prototype of the proposed architecture achieves 63.7dB SNDR in 10MHz bandwidth while consuming 1.1mW of the power. The majority of the power is consumed in digital counters which should reduce with further process scaling. The VCO based second stage is very area efficient taking only 0.02mm^2 of area.

Chapter 6 Conclusion

In this chapter we look at some of the drawbacks of the proposed architecture. We also present some ideas which can be a basis of future work.

6.1 Limitations of proposed architecture

6.1.1 Speed limitation

One of the key limitations of the hybrid ADC presented in the thesis is that the throughput rate of the ADC is limited by the resolution obtained from second stage at high speed. The prototype achieves an SNDR of 66dB when clocked at 10MHz but the SNDR drops to 63.7dB when clocked at 20MHz because of the reduction in the count obtained from the second stage. The resolution of a VCO based second stage is given by

$$\mathrm{Re}solution = \log_2\left[\left(\frac{F_{osc,\max} - F_{osc,\min}}{F_s}\right) * 2 * k * Np\right] \quad (1)$$

where F_{osc} is the differential oscillation frequency. The factor k accounts for the fact that at most only half of the Fs period is available for phase integration. At very high sampling speeds k can be as small as 0.4 because of the need for non-overlapping phases. VCO based ADC architecture can realize 12-14 bits of resolutions at tens of Msps. However, at higher sampling frequencies the required VCO frequencies cannot be achieved even in advanced CMOS processes. For example, a simple calculation shows that a 12 bit, 200Msps ADC will need a differential oscillation frequency of 136GHz for a ring oscillator with 3 inverters or a time resolution of 1.2ps. In this chapter we present couple of potential method of achieving higher throughput with

the hybrid technique presented in this work.

6.1.2 Differential frequency temperature stability

The full scale COUNT_FS obtained from calibration needs to be accurate to better than 8-bits. Since the value of the COUNT_FS will vary with temperature the ADC needs to be re-calibrated whenever the COUNT_FS deviates from its nominal value by more than COUNT_FS/256. There are two sources of drift in COUNT_FS with temperature. First is the change in finite DC gain of the opamp with temperature. Second factor is the change in VCO gain (GHz/V) with temperature. Both these effects discussed below limit the ADC performance across temperature.

Opamp DC gain variation

Let the finite opamp gain at room temperature be A_0. The error in the residue due to finite gain is given by $1/ A_0\beta$ where β is the feedback factor and is 0.3 for this design. This error due to finite opamp gain is not a concern because of calibration.

Now let $A_1 = (1-\alpha)*A_0$ denote the dc gain at a different temperature. Without re-calibration the error in the residue is given by

$$\varepsilon = \frac{1}{A_1\beta} - \frac{1}{A_0\beta} = \frac{\alpha}{A_1\beta} \quad (2)$$

This error term must be less than $1/2^8$ to get 12bit ADC performance. Since there are other sources of error the aim should be to have this term less than $1/2^{10}$.

Figure 6.1 shows simulated DC gain variation across commercial temperature range of 0C to 70C for the opamp used in this design. The worst case α is 0.1 leading to an error of about $1/2^{10}$. This means that at least in commercial temperature range re-calibration is not necessary. Across a much larger industrial temperature range of

-40C to 125C α increases to 0.25 which will mean that we will need a recalibration at higher temperatures.

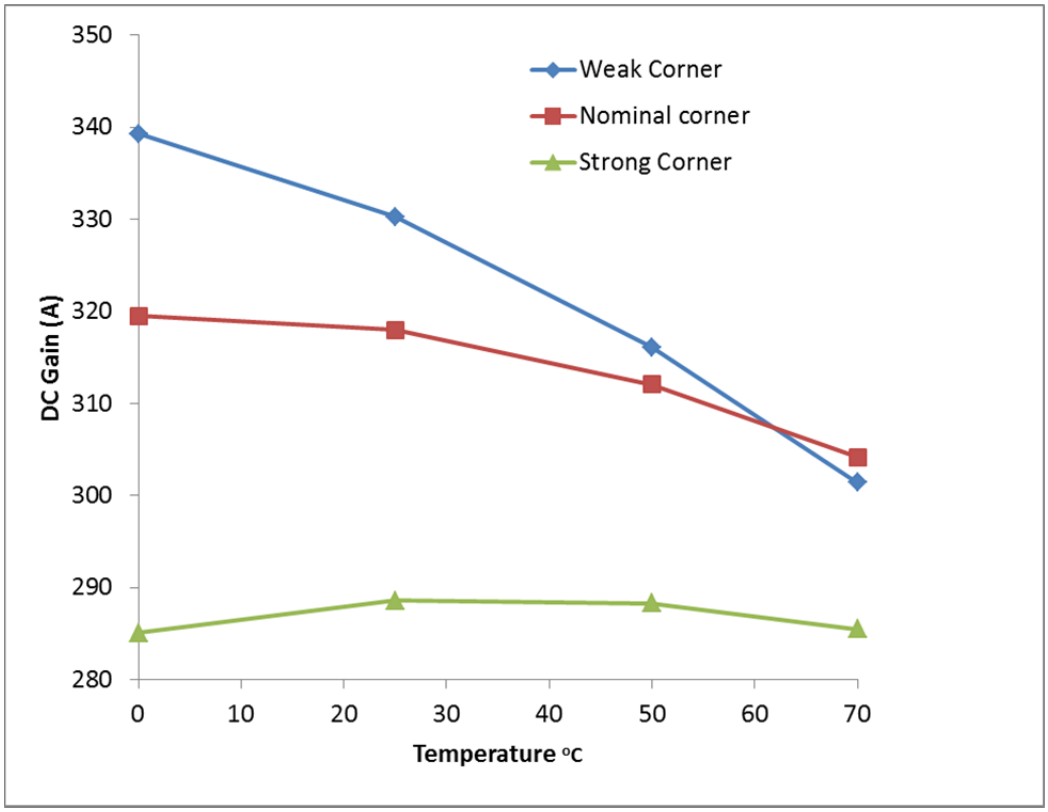


Figure 6.1 Simulated opamp DC gain variation with temperature

VCO Gain variation

For the VCO circuit in Figure 4.10 differential frequency variation with temperature is determined by two phenomenons working in opposite direction. For a fixed reference input, the output current of the differential transconductance pair decreases with increasing temperature, causing the differential output frequency to decrease. For a fixed bias current the oscillation frequency of the current controlled oscillator increases with increasing temperature. This is because of threshold voltage reduction at higher temperature. These two trends cancel out the majority of the frequency drift

across temperature range. Figure 6.2 shows the simulated drift of differential oscillation frequency for typical corner. Across the commercial temperature range of 0 to 70C the drift is about 0.3%. Figure 6.3 shows the simulated drift from room temperature across the process corners. The worst case drift is about 0.46% . This indicates that the VCO design will be good to 11-bit level without any calibration needed for temperature drift. The simulation results indicate that the design will need recalibration if we need to achieve performance better than 11-bit over a wide temperature range. We will discuss how a simple replica circuit can provide the corrected calibrated value without interrupting the ADC conversion flow.

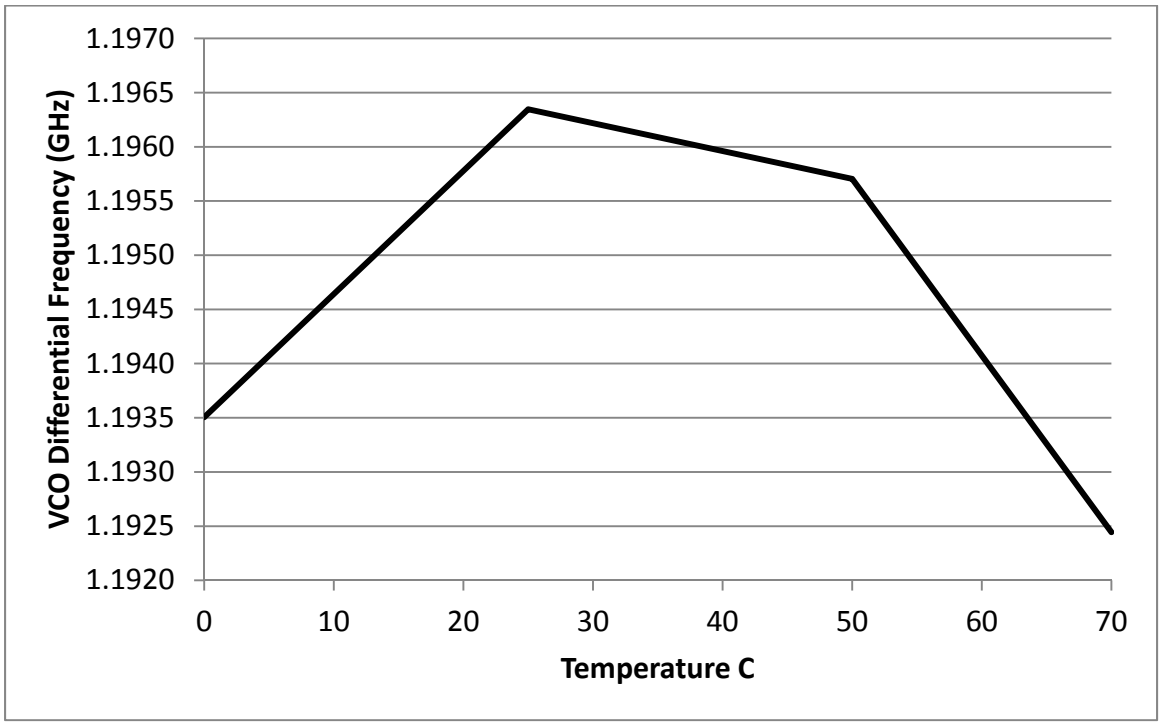


Figure 6.2 VCO differential frequency variations for fixed input

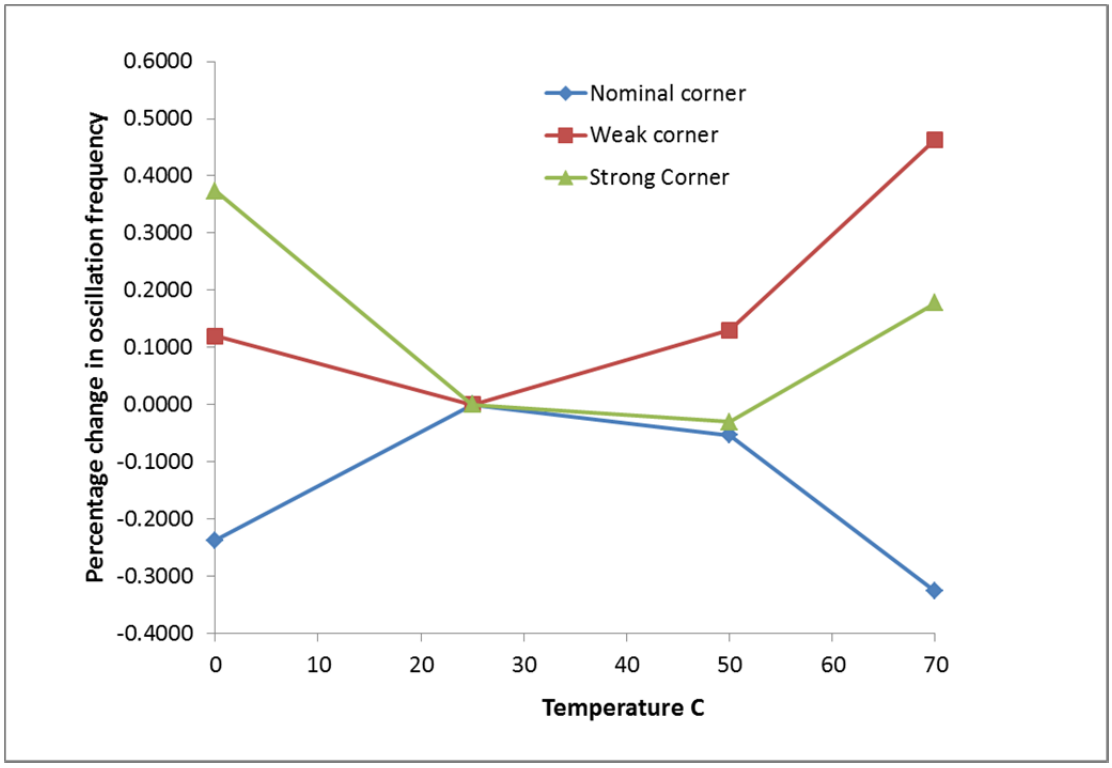


Figure 6.3 VCO differential frequency variation for fixed input across corners

6.2 Improving the ADC speed

We look at two different approaches to improve the conversion speed with this ADC architecture.

6.2.1 Using TDC for phase quantization

The easiest way to improve the time resolution in this design is to increase the number of phases in the ring oscillator. For example we can gain one extra bit of resolution by using a seven stage ring oscillator instead of three stage ring oscillator used in this design. Another option is to increase the oscillation frequency as the design is still not at the edge of process limitations. Both this approaches lead to higher power

consumption. One option to increase resolution without increase power consumption is to use a combination of counters and time to digital converters (TDC) to quantize the VCO phase [117]. The delay cell based TDC discussed in chapter 1 is shown in Figure 6.4(a). TDC measures time interval between the rising edge of START signal to rising edge of STOP signal in units of buffer delay. The counter counts the integer number of cycles of VCO. The fractional count is obtained by the three TDC's as follows. TDC_1 measures the time from rising edge of S to the following rising edge of the VCO, which is denoted as t_1 in Fig 6.4(b). TDC_2 measures the VCO time period t_2 whereas as TDC_3 measures the time (t_3) from falling edge of S to following rising edge of VCO. The fractional count is obtained as $(t_1-t_3)/t_2$. Using TDC's consumes less power than approach just using counters and provides better time resolution (~40ps) in this process.

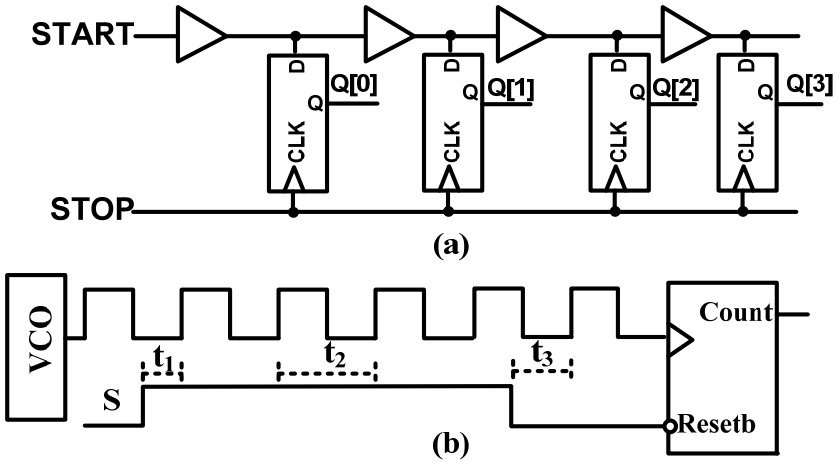


Figure 6.4 (a) Delay based TDC unit. (b) Quantizer timing

6.2.2 Interleaved VCO based ADC

One of the key features of the VCO based ADC is that we can obtain higher resolution by extending the integration time. We can take advantage of this by using time-interleaving of multiple VCOs. Fig 6.5 shows a two channel interleaved VCO based ADC with the associated timing. The two VCOs sample the analog input on 'S' phase which is alternate "high" of Fs signal. The held signal is then integrated in 'H' phase till it is time to sample the input again. This scheme extends the integration time by one full clock period. This leads to an improvement in resolution by a factor (1+ k)/k, which equals 3.5 for k of 0.4. This is a key advantage over traditional interleaving approaches where a two channel interleaving only gives a factor of two improvements. The approach can be extended to interleave more than two VCO based ADC. The biggest improvement is achieved by going from single VCO to two VCO's. Further increase in interleaved VCOs leads to linear improvement in resolution.

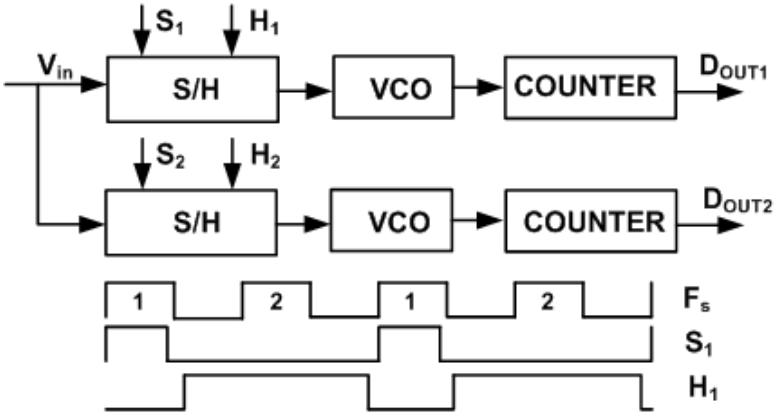


Figure 6.5 Time interleaved VCO ADC

As seen from the timing diagram in Fig 6.6, using four interleaved VCOs extends the integration time of each individual VCO by a factor of (3 +k)/k which equals 8.5 for a k of 0.4. For a fixed resolution this means that ADC can now run at 8.5X faster speed than will be possible with a single VCO. The ring oscillators and counters are digital circuits which tend to occupy very small area in advanced CMOS nodes. This means that interleaving multiple of these VCO's is well suited to advance CMOS nodes.

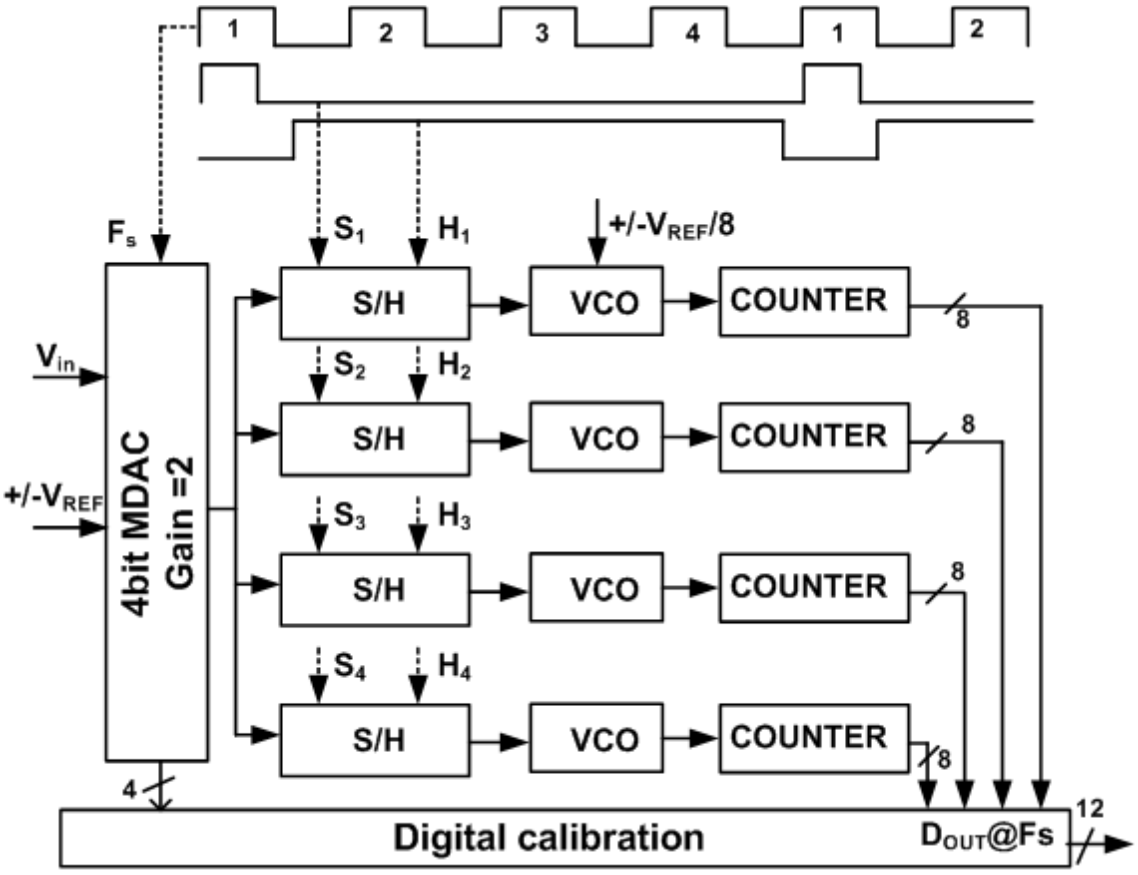


Figure 6.6 High Speed ADC topology

The performance of a time-interleaved ADC degrades because of gain, offset and timing mismatch among the channels [118]. For the VCO based second stage design the digital output is given by

$$Dout = \frac{COUNT\_IN - COUNT\_OFFSET}{COUNT\_FS} \quad (3)$$

As can be seen from (3) the gain mismatch is calibrated out in this architecture because the output is normalized with respect to a COUNT_FS obtained for each channel. The offset is similarly calibrated out for each channel. The timing scheme shown in Figure 6.2 always samples the input signal on the falling edge of master clock so is immune to duty cycle variation on the master clock.

ADC architecture in Figure 6.6 precedes the interleaved VCO stage with a 4 bit first stage with an MDAC gain of 2. The VCO stage quantizes the residue obtained from the first stage. Since the sampling of the input happens in the first stage the architecture becomes immune to the timing mismatch in the interleaved second stage. The second stage sample and hold (S/H) is a passive circuit with a switch and holding capacitor. For a given resolution the 4bits obtained from the first stage extends the speed of the interleaved VCO based ADC described above by a factor of 16. The VCO in this architecture sees only the residue from first stage. This helps to make the VCO more linear and relaxes the linearity requirement on the VCO.

A 12 bit, 200Msps ADC based on topology presented above has been designed in 65nm CMOS process node. The nominal VCO frequency for the design is 3.2GHz. The power consumption for the design is 20mW. The design has been simulated with mismatches introduced in the different VCO stages. Fig 6.7 shows the output

spectrum of the ADC output with a 12.5MHz full scale input signal. The harmonic distortion is better than 80dB and the signal to quantization noise ratio is 65dB.

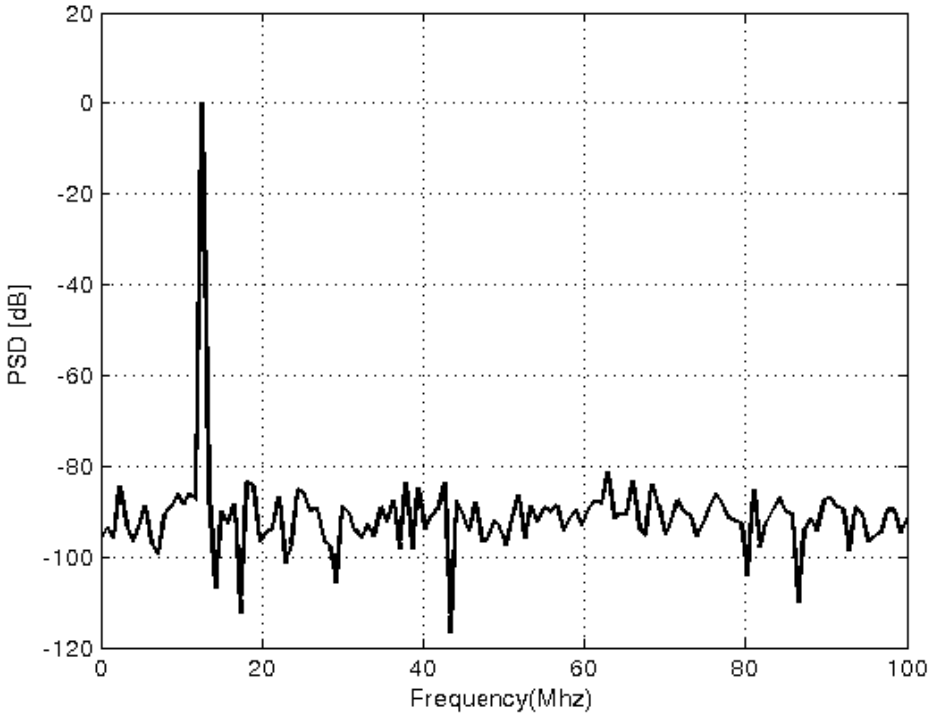


Figure 6.7 Simulated PSD of the high speed ADC

6.3 Improving thermal stability

As discussed in preceding section the design presented in this thesis needs to be re-calibrated for temperature change. This means that the A/D conversion needs to halt periodically to calibrate the ADC. Based on the simulation results presented in previous section calibration may be needed every 20^{o} C to maintain optimal performance. While this may be acceptable in some applications, it may not be suitable for applications which need continuous operation over prolonged period of time. We need a background calibration scheme which can update the COUNT_FS value after initial factory calibration. One of the ways to do this is to use a replica

circuit to generate a secondary COUNT_CAL as illustrated in Figure 6.8. At room temperature COUNT_CAL will be same as COUNT_FS but as temperature varies COUNT_CAL will change. This COUNT_CAL can be used to update the full scale COUNT in real time. The replica circuit doesn't need to be active all the time, so its power consumption will be negligible. The replica circuit also doesn't load the input and the reference loading is a very small fraction of overall ADC loading. Only real penalty of using the replica circuit is extra area needed for its implementation. As discussed in chapter 5 the biggest area contribution in the ADC is the first stage MDAC capacitors followed by the flash ADC. The replica circuit doesn't need the flash ADC and we only need one DAC unit capacitor for determining the COUNT_FS so the number of unit capacitors can be reduced from 48 to 18.

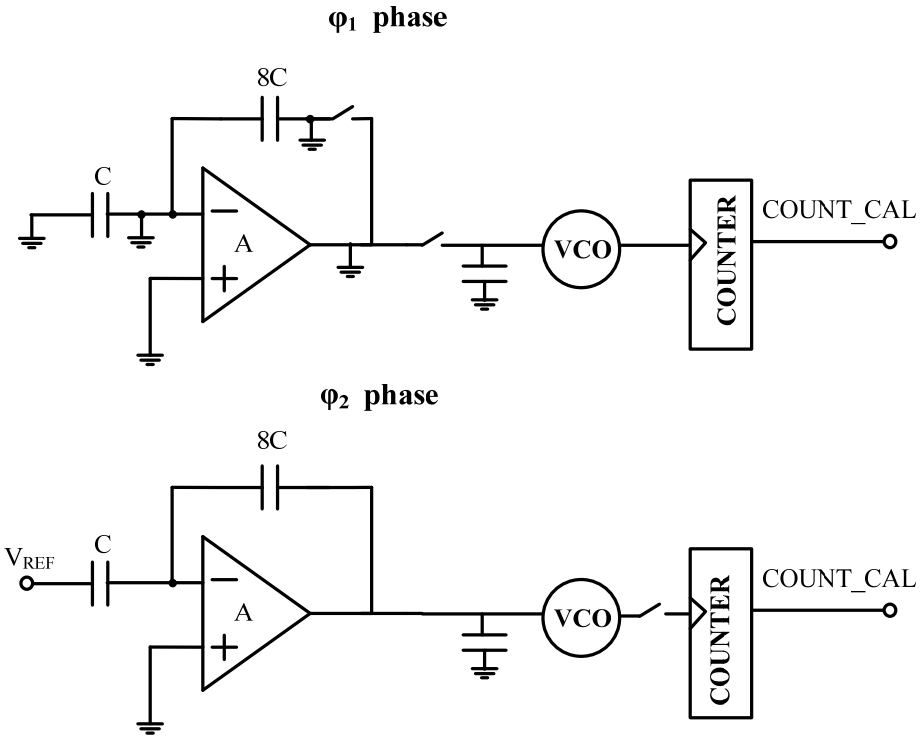


Figure 6.8 Replica circuit used for background calibration

Also since noise in the replica circuit is not important we can use a smaller unit capacitor. Next biggest contributor to area in the current design is the signal dependent boost switches which are also not needed in replica design. We estimate the ADC area to increase by about 30% with the addition of replica circuit.

6.4 Conclusion

In this chapter we looked at the limitations of the design presented in this thesis. We looked at two different topologies which can extend the usable bandwidth of VCO based ADC. A new interleaved VCO topology is proposed in this chapter, which can be basis of future work. We also presented a potential background calibration scheme for the VCO based ADC. The design presented in this thesis shows that a 12 bit Nyquist rate low power ADC can be built with VCO based second stage. The performance of the prototype chip is comparable to the state-of-art in terms of figure-of-merit but this new architecture uses significantly less circuit area. The power consumption of the design is dominated by digital blocks and will reduce in more advanced CMOS technology nodes.

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