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Characterization of Thermal Stresses and Plasticity in Through-Silicon Via Structures for Three-dimensional Integration

Tengfei Jiang[a], Suk-Kyu Ryu[b], Jay Im[a], Rui Huang[b], and Paul S. Ho[a]

[a]*Microelectronics Research Center, University of Texas, Austin, TX 78712*
[b]*Department of Aerospace Engineering and Engineering Mechanics, University of Texas, Austin, TX 78712*

Abstract. Through-silicon via (TSV) is a critical element connecting stacked dies in three-dimensional (3D) integration. The mismatch of thermal expansion coefficients between the Cu via and Si can generate significant stresses in the TSV structure to cause reliability problems. In this study, the thermal stress in the TSV structure was measured by the wafer curvature method and its unique stress characteristics were compared to that of a Cu thin film structure. The thermo-mechanical characteristics of the Cu TSV structure were correlated to microstructure evolution during thermal cycling and the local plasticity in Cu in a triaxial stress state. These findings were confirmed by microstructure analysis of the Cu vias and finite element analysis (FEA) of the stress characteristics. In addition, the local plasticity and deformation in and around individual TSVs were measured by synchrotron x-ray microdiffraction to supplement the wafer curvature measurements. The importance and implication of the local plasticity and residual stress on TSV reliabilities are discussed for TSV extrusion and device keep-out zone (KOZ).

Keywords: 3D integration, Through-silicon via (TSV), Thermo-mechanical reliability, FEA.

INTRODUCTION

Three-dimensional (3D) integration with through-silicon vias (TSVs) has emerged as a potential solution to overcome the wiring limit beyond the 22 nm technology node. The TSV is a critical element that provides short vertical interconnects to improve the electrical performance and power consumption for 3D integration [1-4]. This has generated great interests from the industry to develop 3D integration based on TSV technologies. Cu is widely used to form the TSV using a process compatible with Cu backend integration. The fabrication of TSV structures involves deep etching of Si wafer to form via holes, deposition of barrier and seed layers, and the electroplating of Cu to fill the vias. The TSV structures will undergo further processing during the fabrication of 3D integrated circuits, most of which are carried out at elevated temperatures. Thermal stresses can arise during fabrication, testing and operation of the TSV structures due to the large mismatch in the coefficient of thermal expansion (CTE) between Cu and Si. The stresses are large enough to cause serious reliability concerns even structural failures in the integrated structure, including TSV extrusion, cracking of Si near the TSV and degradation of device performance [5-9]. Management and mitigation of thermal stresses in the TSV structures require proper stress characterization and modeling analysis. This is especially challenging since the TSV geometry, material and mechanical behaviors are distinctly different from that of the traditional back end of the line (BEOL) structures.

Experimental methods have been applied to measure thermal stresses in Cu TSV structures. One widely used technique is the micro-Raman spectroscopy, which measures the frequency shift of the Raman modes caused by strain in the Si surrounding the TSVs [10-12]. Depending on the Si orientation and the Raman system configuration, certain stress components for Si or their combinations can be deduced. However, Raman spectroscopy is limited to measuring the near-surface stresses in Si but lacking the ability to analyze the stresses in Cu. Resolving individual stress components can also be difficult and often requires detailed modeling [12]. More recently, synchrotron x-ray microdiffraction has been applied to measure the stress characteristics for TSV structures [13]. X-ray microdiffraction can measure both Si and Cu but so far only very limited results have been reported. In addition, the method requires special facility that is not easily accessible. Numerical analyses such as finite element analysis (FEA) are commonly used to calculate the magnitude and distribution of stresses in TSV structures [14-16]. This method allows the study of complex structures without special experimental facilities. However, proper material and mechanical properties of the constituent materials are required and experimental validation of the model is important.

Stress Induced Phenomena and Reliability in 3D Microelectronics
AIP Conf. Proc. 1601, 55-66 (2014); doi: 10.1063/1.4881340

In this study, we apply the wafer curvature method to study the stress characteristics of Cu TSV structures during thermal cycling. The results are contrasted with those of on-wafer Cu thin film samples for which different curvature behaviors are observed. As a global measurement, the curvature change reflects the overall effect of the thermal stresses in a periodic TSV array, from which the stress behavior of individual Cu TSV can be deduced by numerical analysis. By comparing to thin film samples, we demonstrate that the TSV structures have distinct triaxial stress characteristics as opposed to the biaxial stress state of thin films. This gives rise to residual stresses in the TSVs during thermal cycling with highly localized plasticity near its top at the Cu/Si interface. The stress behavior is correlated to changes in the microstructures of the Cu vias during thermal cycling, which are analyzed by focused ion beam (FIB) and electron backscatter diffraction (EBSD) techniques. Along with the microstructure analysis, the mechanisms underlying the linear and nonlinear temperature-curvature behaviors of the TSV specimen are discussed. The wafer curvature method is supplemented by synchrotron x-ray microdiffraction to measure the local plasticity and deformation in and around individual TSVs. In particular, the local plasticity was observed near the top at the Cu/Si interface, verifying the FEA results. The local plasticity provides a mechanism for TSV pop-up without the presence of interfacial delamination. The implication of the triaxial stress state on TSV reliability is discussed with a focus on the stress-induced carrier mobility change of devices.

CURVATURE MEASUREMENTS DURING THERMAL CYCLING

The TSV test structures used in this study contained patches of TSV arrays fabricated in 780 μm thick (001) silicon wafers. The Cu vias had a diameter of 10 μm and height of 55 μm and with barrier layers of 0.1μm Ta and 0.4μm oxide deposited at the via/Si interface. The spacing between the TSVs was 40 μm along the [110] direction and 50 μm along the $[1\,\bar{1}0]$ direction. After the TSVs were fabricated, annealing was carried out at 100°C for 30 min followed by chemical mechanical planarization (CMP), leaving an oxide layer of 0.8 μm thick on the wafer surface, which was then mechanically removed for the wafer curvature measurements. For the curvature measurement, the wafer was diced into 5 mm by 50 mm strips with each strip containing periodic arrays of blind vias located near the centerline of the sample, as illustrated in Fig. 1. The volume ratio of Cu to Si was 0.015% for the TSV sample. The thin film sample used as a comparison contained 0.8 μm electroplated Cu film on 780 μm Si substrate with a thin diffusion barrier layer in between and a 50 nm SiN capping layer on top of the Cu film. The thin film sample was cut into strips of the same size for the curvature measurement. The volume ratio of Cu to Si in the thin film sample was 0.103%. Since the amount of curvature depends on the volume ratio of Cu to Si, the measured curvatures of the thin film and the TSV are normalized by the Cu volume ratio to facilitate the direct comparison of their stress characteristics.

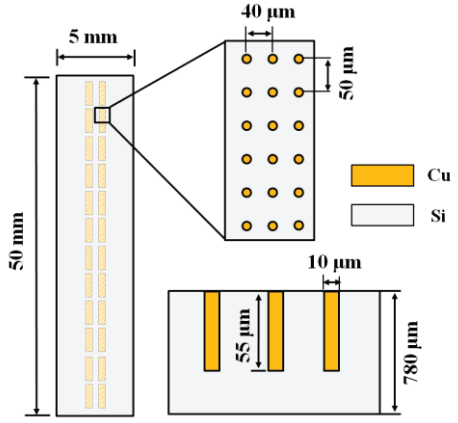


FIGURE 1. Illustration of the TSV sample for the precision wafer curvature measurements.

For the curvature measurements, both samples were subject to six thermal cycles: heating to 200°C and cooling to room temperature (RT) in the first two cycles, followed by two cycles to 350°C and two more cycles to 400°C. After thermal cycling measurements, the same sample was measured again under the same thermal cycling condition with Cu etched off so that a reference curvature, κ_0, can be obtained. By subtracting the reference

curvature, the net curvature changes ($\Delta\kappa = \kappa - \kappa_0$) during thermal cycles for the TSV and thin film samples were obtained and plotted in Fig. 2.

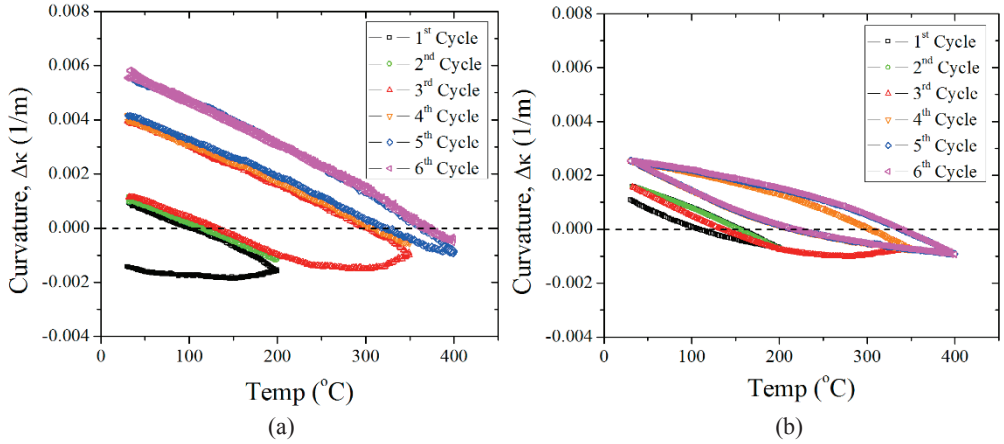


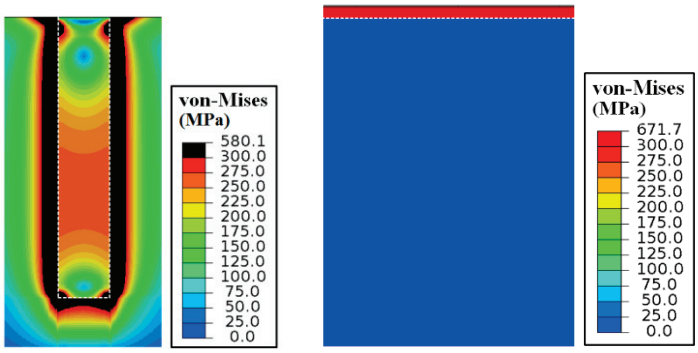
FIGURE 2. Curvature-temperature plots of (a) TSV and (b) electroplated Cu thin film. The curvature of the Cu thin film is normalized by the Cu volume ratio for comparison with the TSV structure.

For the TSV structure, the curvature changed nonlinearly during heating in the first thermal cycle, while during cooling a linear behavior was observed. The heating and cooling curves of the second cycle overlapped with the prior linear cooling curve, where no hysteresis loop was observed. In the third cycle with increased heating to 350°C, the curvature showed a linear behavior until 200°C then resumed nonlinear relaxation to 350°C. During the fourth cycle with heating to 350°C, the entire curvature again followed a linear behavior. A similar behavior was observed for the subsequent two cycles with heating increased to 400°C. The overall behavior was reproducible in that a nonlinear curvature due to relaxation occurred during heating beyond the previous peak temperature, and it is followed by a linear cooling behavior with an increased curvature upon cooling to RT.

The curvature behavior of the TSV structures as a function of temperature is distinctly different from that of the Cu thin film, where hysteresis loops were formed when the sample was thermal cycled, as readily observed in the second, fourth and last cycle in Fig. 2b. For metal thin films, the stress evolution during thermal cycling has been extensively studied with wafer curvature measurements [17-19]. Grain growth, plasticity, and creep are known mechanisms for stress relaxation in Cu thin films to cause nonlinear thermomechanical behaviors, and hysteresis loops are commonly attributed to plastic deformation in the film [19-22]. Detailed studies have been carried out in our laboratory correlating curvature changes with microstructure evolution for electroplated Cu films and the results confirmed that the nonlinear curvature relaxation observed in Fig. 2b can be attributed to such stress relaxation mechanisms [21,22]. Significantly, hysteresis loops were not observed for TSV structures as shown in Fig. 2a, suggesting that large-scale plasticity is not a dominant stress relaxation mechanism. This leads to distinct stress characteristics for the TSV structure, which is analyzed in the following sections.

STRESS ANALYSIS

To analyze the stress characteristics observed for TSV and thin film samples, we focus first on the curvature behavior observed during the cooling cycles where the hysteresis loops were observed only in thin films. 3D FEA models were constructed for both the TSV and thin film structures using a commercial package, ABAQUS (v6.10). For the TSV structure, half of the via was modeled with symmetric boundary conditions in the [110] and $[1\,\bar{1}0]$ directions to simulate the periodic TSV arrays. The material properties used in the model are: Young's modulus, E_{Cu} = 110 GPa, E_{Si}=130 GPa, and E_{oxide} = 70 GPa; Poisson's ratio, ν_{Cu} = 0.35, ν_{Si} = 0.28, and ν_{oxide} = 0.16. The CTEs are α_{Cu} = 17 ppm/°C, α_{Si} = 2.3 ppm/°C and α_{oxide} = 0.55 ppm/°C. The von-Mises stress, which is the effective shear stress driving plastic deformation, was calculated for both structures for a thermal load of ΔT = -270°C, corresponding to 350°C thermal cycling. The results are plotted in Fig. 3.



(a) (b)

FIGURE 3. Distribution of von-Mises stresses for (a) TSV and (b) thin film structures for a thermal load of ΔT = -270oC, corresponding to 350°C thermal cycling.

For the TSV structure, the von-Mises stress distribution was found to be non-uniform as shown in Fig. 3a. With a thermal load of ΔT = -270°C, the stress level in most part of the via was much lower than the yield strength for Cu, which was reported to range from 150 MPa to 300 MPa, depending on the Cu grain size [23-24]. Thus most of the Cu in the TSV behaves elastically during cooling. This behavior can be attributed to the triaxial stress state in the Cu TSV due to the confinement by the surrounding Si, except for a small region at the top and bottom of the via near the via/Si interface. To demonstrate this behavior, we assumed a relatively high yield strength of 300 MPa and as shown in Fig.3a, with a thermal load of -270°C, most of the via behaved elastically while localized plasticity occurred only near the top and the bottom of the TSV. Since the volume fraction of Cu in the TSV sample is already small, the localized plasticity within Cu vias is too small to affect the overall curvature behavior; therefore hysteresis loop is not observed in Fig. 2a. In contrast, the stress in the Cu thin film is uniform and biaxial due to the two-dimensional confinement of the Cu film by the Si substrate. In this case, the von-Mises stress is uniform and large throughout the film. As a result, the entire film undergoes plastic deformation even for an assumed yield strength as high as 300 MPa, as shown in Fig. 3b. Such large-scale plasticity was manifested by the hysteresis loops observed under thermal cycling to 350°C and 400°C as shown in Fig. 2b. Thus the local plasticity in TSV is a key factor in providing distinct stress characteristics for TSV structures. It plays an important role in controlling the residual stress in the TSV during thermal cycling and has significant implications on stress reliability and device performance. These issues will be addressed in the discussion section.

MICROSTRUCTURE ANALYSIS

Next we analyze the curvature behavior observed during the heating cycle. As shown in Fig. 2, both the thin film and TSV samples followed an initial linear elastic behavior upon heating from the room temperature. The curvature behavior of the thin film specimen became nonlinear at a relatively high temperature, which can be attributed to stress relaxation mechanisms such as plasticity and grain growth and has been well studied [19,22]. For the TSV sample, nonlinear stress relaxation was observed after heating beyond the maximum temperature of the previous heating cycle. As discussed in Section 3, the underlying mechanism for the observed stress relaxation is unlikely due to localized plasticity in very small areas in TSVs. To understand the stress relaxation mechanism for TSV samples, the microstructure evolution was investigated. Several samples were subjected to a single thermal cycle to temperatures ranging from 100°C to 400°C with an interval of 50°C. The curvatures observed are similar to that shown in Fig.2a, as summarized in Fig. 4 for samples cycled to 100, 200, 300, and 400°C.

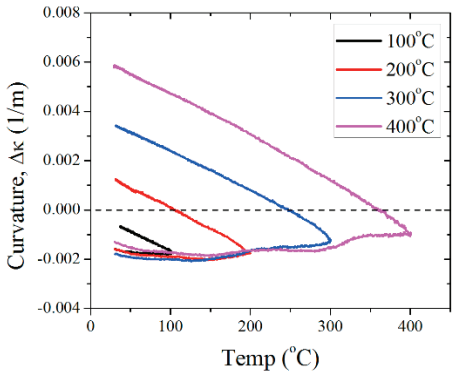


FIGURE 4. Curvature-temperature measurements for TSV samples subjected to one time thermal cycling to temperatures between 100ºC and 400ºC.

After thermal cycling, the TSV samples were cross-sectioned by FIB for microstructure analysis. Fig. 5 shows the ion channeling images of the via cross-sections after thermal cycling, with the as-received sample also shown as a reference. From the image contrast, an increase in grain size was observed with increasing cycling temperature, providing a qualitative measure of grain growth.

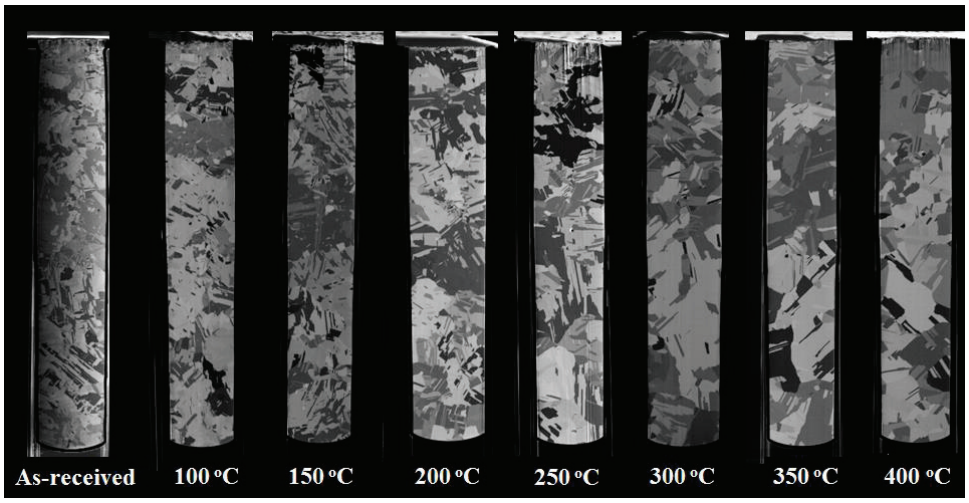
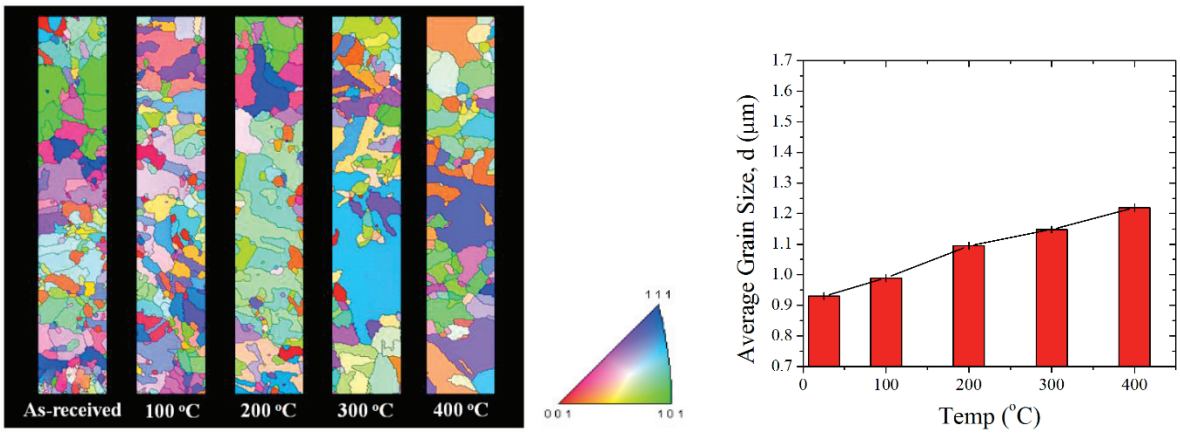


FIGURE 5. Cross-sectional FIB images of TSVs after single temperature thermal cycling measurements. The as-received sample is shown as a reference.

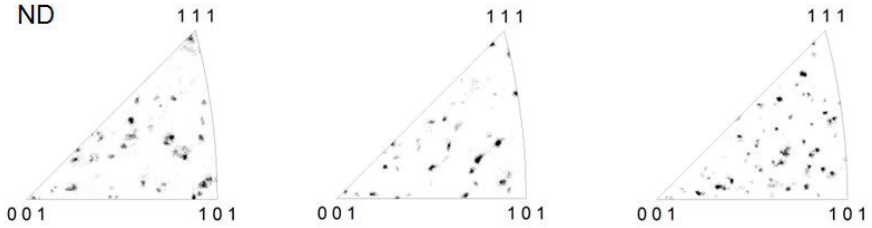
For quantitative analysis of the grain growth of the Cu microstructure, the TSV samples as-received and after thermal cycling were characterized by EBSD. The grain maps of the Cu vias are shown in Fig. 6 as a function of the cycling temperature, with each color corresponding to a particular grain orientation. The average grain size for each sample is measured and plotted in Fig. 6b, clearly showing grain growth with increasing temperature of the thermal cycle.



(a) (b)

FIGURE 6. (a) EBSD grain maps and (b) average Cu grain size for the as-received TSV and TSVs after single temperature thermal cycling.

The grain orientation in the vias was also studied and random grain orientations were found for all samples. Fig. 7 plots the inverse pole figures (IPFs) along the normal direction of the TSV length (ND) for the as-received and thermal cycled samples to 200 and 400°C. The random grain orientation suggests a statistically isotropic Cu microstructure, hence the use of isotropic thermomechanical properties for the Cu vias in numerical analysis is justified.



(a) (b) (c)

FIGURE 7. Inverse pole figures plotted along the TSV axis (ND) for (a) the as-received TSV, (b) a TSV after thermal cycling to 200°C, and (c) a TSV after thermal cycling to 400°C.

For all samples, a prominent peak was observed at 60° misorientation angles, corresponding to the twin boundaries for Cu. Comparing the statistical distributions of the misorientation angles, the fraction of the twin boundaries was large for the as-received sample (Fig. 8a) and remained large after thermal cycling to 400°C (Fig. 8b). This suggests that twinning was already present after TSV processing. Interestingly, twinning did not seem to contribute to stress relaxation in the TSV structures in this study, although it is an effective mechanism for stress relaxation in Cu thin films [22]. The presence of twin boundaries, however, can increase the Cu yield strength and affect other thermo-mechanical properties of the TSVs [25].

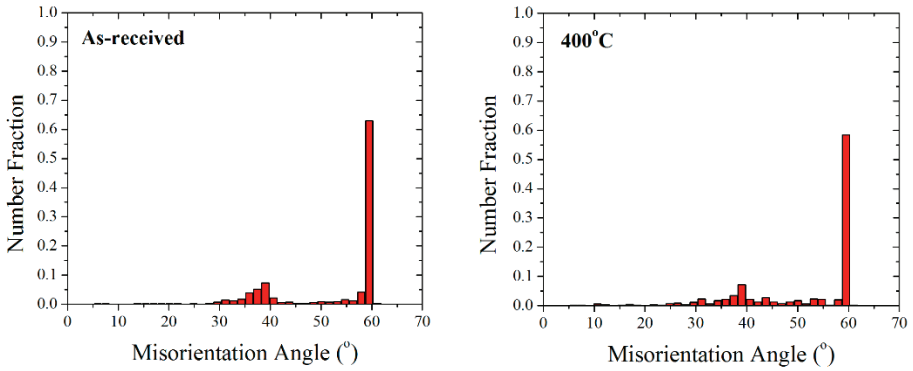


FIGURE 8. Grain misorientation angles for (a) as-received TSV and (b) TSV after thermal cycling to 400°C.

DISCUSSION

Stress characteristics of TSVs

Curvature measurements combined with microstructure and stress analyses allow the stress characteristics of TSV structures to be better understood. A key feature of the TSV structure is the triaxial stress state in Cu, which is distinctly different from the biaxial stress state of thin films. Such a difference in the stress states can be traced to the different confinement effects in the 2D and 3D structures by the Si substrate. For the triaxial stress state, the effective shear stress is relatively low in most of the Cu vias so that the TSV behaves mostly linearly elastic during the cooling cycle. Plastic deformation will occur primarily near the top and bottom of the vias and is localized in nature. During the heating cycle, the stress relaxation in the TSV structure is mainly driven by grain growth. By comparing Fig. 2a and Fig. 4, despite the different thermal cycling conditions, the magnitude of the residual curvature appears to be similar when the same peak temperature was reached. This is because grain growth, and thus the stress relaxation, is largely dictated by the peak temperature in the heating cycle [27-28]. In general, it is the stress relaxation due to grain growth during the heating cycle that determines the residual stress in the TSV structure at the end of the cooling cycle.

For quantitative analysis of the residual stress, it is necessary to convert the curvature to stress. For the thin film structure, the curvature can be converted to stress using Stoney's equation, as shown in Fig. 9b [21]. However, for the TSV structure, because of the triaxial stress state and the TSV array configuration, an analytic solution similar to Stoney's equation is not available. In this study, FEA is used to convert the curvature to stress. A 3D model for a quarter of the TSV sample with a symmetric boundary condition is used to simulate the linear curvature behavior observed in the second cycle of the measurement in Fig. 2a. Cu is assumed to be isotropic and linear elastic, and an average curvature is determined along the centerline of the sample for a thermal load of $\Delta T = -200^{o}C$. The rate of curvature change, $\Delta\kappa/\Delta T$, is calculated and compared with the experiment. The calculated $\Delta\kappa/\Delta T = -1.88\times10^{-5}$ $m^{-1}/^{o}C$ is close to the measured curvature change of -1.47×10^{-5} $m^{-1}/^{o}C$, with the difference possibly caused by the variability of the TSV structures and the uncertainty of material properties. In the experiment, the zero curvature of the sample corresponds to the stress free condition in Cu. This allows a reference temperature to be determined for FEA, and a scaling factor can be obtained by calculating the stress value corresponding to a particular curvature, $\beta = \sigma_{xx}/\Delta\kappa$, which can then be used to convert the measured curvature to stress as shown in Fig. 9a.

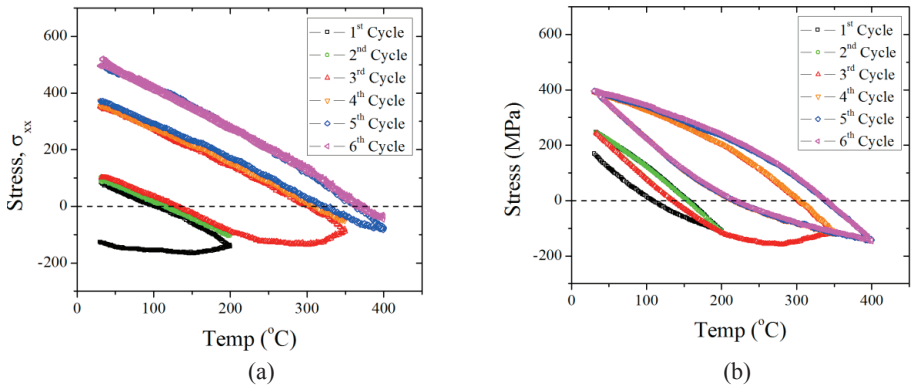


FIGURE 9. Conversion of curvature into stress for (a) TSV and (b) thin film structures.

The residual stress in the TSV structure will increases when the TSV is subjected to heating under thermal cycling. For thin films, while stress relaxation by grain growth during heating occurs, the presence of the large-scale plasticity during cooling significantly reduces the residual stress. The effect on the residual stress can be seen by comparing Fig. 9a and 9b, where the residual stress in the TSV is larger than that in the thin film after the 400°C. Given similar amount of stress relaxation during the heating cycles, the residual stresses at the end of the cooling cycles are significantly higher for the TSV. The residual stress has important implications on the device keep-out zone (KOZ) which will be discussed.

Local plasticity and via extrusion

The local plasticity in the Cu via near the top surface and at the Cu/Si interface plays an important role in controlling the via extrusion during thermal cycling. The local plasticity was directly observed by synchrotron x-ray microdiffraction measurements. The x-ray microdiffraction measurement was conducted at beamline 12.3.2 at the Advanced Light Source (ALS), Lawrence Berkeley National Laboratory (LBNL). The cross-sections of an as-received TSV and a TSV thermal cycled to 400°C were scanned with polychromatic x-rays (white beam) with energies from 5keV to 22keV. The x-ray microbeam is focused to a spot size of 1 μm and the scan step size is 1 μm/step. The measurement generates a Laue pattern for each point in the scan matrix which is analyzed with the XMAS software developed at the beamline [29]. The asymmetric broadening of the averaged peak width (APW) can be correlated to increased density of geometrically necessary dislocations in Cu to provide a measure of the local plastic deformation [30, 31]. This is plotted for the Cu via in Fig. 10. Compared to the as-received sample, the Cu via after thermal cycling to 400°C shows a much larger averaged peak width (APW) near the top Cu/Si interface. The increase in the APW and thus the local dislocation density indicates the localized plasticity, while the rest of the via remains nearly elastic. Details of the synchrotron study will be published elsewhere [32].

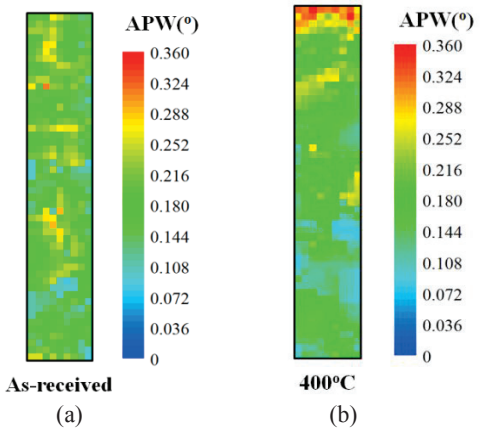
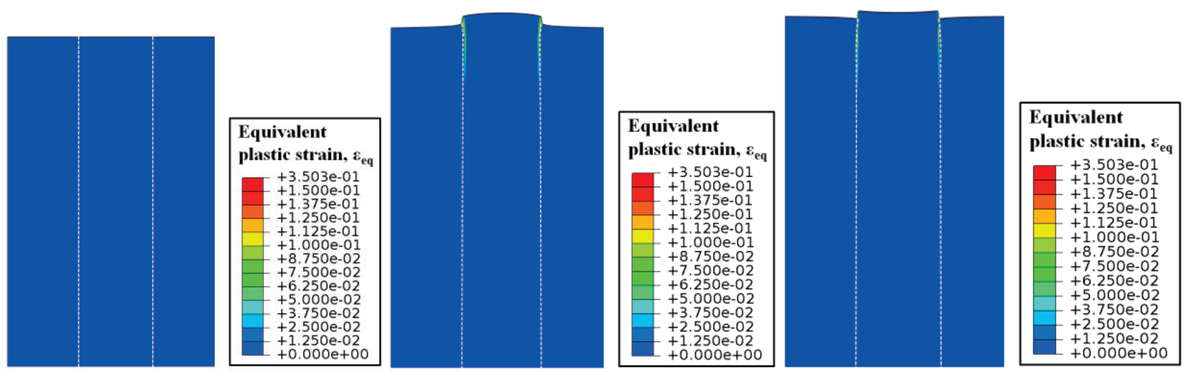


FIGURE 10. Average peak width of Cu via for as-received sample and sample thermal cycled to 400°C obtained by synchrotron x-ray microdiffraction.

The local plasticity has important implication on via extrusion. Via extrusion, or pop-up, is a reliability issue in 3D integration in which Cu extrudes from the wafer surface to damage the interconnect structures above the vias [5]. A previous study has shown that stress-induced interfacial delamination could result in via extrusion [7]. However, in subsequent investigations including this study, via extrusion was observed without evidence of delamination. An alternate mechanism is proposed based on the results from this study that via extrusion is induced by local plasticity in the Cu vias. When the TSV structure is being heated, Cu with the larger CTE will expand but is confined by the surrounding Si. This drives the upward extrusion of Cu above Si. Grain growth will relax the stress, but the stress can still exceed the elastic limit near the top of the via at the interface to induce plastic deformation at an elevated temperature. During cooling, the volume shrinkage of Cu will reduce the amount of the extrusion due to elastic recovery. But as the stress in Cu becomes increasingly tensile, plasticity adds up near the top of the via where the von-Mises stress is largest. The plastic deformation eventually leads to unrecoverable permanent extrusion after the TSV cooled down to room temperature. This process is demonstrated by an elastic-plastic FEA model for a thermal cycle from RT to 350^{o}C. Assuming a yield strength of 250 MPa, the deformation and the equivalent plastic strain of the via at RT, 350^{o}C and after cooling back to RT are shown in Fig. 11. The via extrusion simulated by FEA is consistent with the via extrusion observed in TSV structures [33].



(a) (b) (c)

FIGURE 11. Elastic-Plastic FEA model of via extrusion under thermal cycling from RT to 350^{o}C and back to RT with the equivalent plastic strain in Cu plotted. Deformation at different stages of the thermal cycling: (a) at RT before heating, (b) after heating to 350^{o}C and (c) after return to RT. (scale factor =30).

In order to prevent via extrusion, plastic deformation in the TSV structure need to be minimized during the various processing steps carried out at elevated temperatures. This can be made possible through an optimized annealing process, in which the TSV structure is heated first to a maximum temperature T_m (e.g., ~300-350^{o}C) above that for subsequent processing steps, followed by a one-time chemical-mechanical planarization (CMP) process to remove the extruded Cu. Below T_m, grain growth and reduction of Cu yield strength is largely prevented in accordance with the Hall-Petch relation [34]. In addition, strain hardening may accompany plasticity to raise the yield strength locally near the top of the Cu via [21]. With stabilized grain structure and strain hardening, when the TSV is subjected to subsequent processing at temperatures lower than T_m, the plasticity in the via is limited to minimize further via extrusion [5,6].

Residual stress and keep-out zone (KOZ)

The residual stress determined by the curvature measurement has important implications on the stress reliability of the TSV structures, in particular, the keep-out zone (KOZ) for CMOS devices. In modeling the KOZ, a linear elastic model is used as suggested by the linear curvature behavior, and the reference temperature for zero stress is determined from the zero curvature in the measurement. The Cu in TSVs is treated as isotropic. The elastic model used here is justified since the elastic-plastic analysis described in the previous section shows that the plastic deformation is localized and limited to the Si/Cu interface. Based on the measured residual stresses and the elastic behavior, the KOZ surrounding the TSVs and its dependence on the TSV layout were evaluated based on the piezoresistivity effects of Si. Since Si is anisotropic, the KOZ was found to depend on wafer types and the device channel directions. For the [100] channel alignment, a thermal load of ΔT = -270^{o}C resulted in a much larger mobility changes in n-type Si than in p-type Si. With the KOZ defined by a 5% mobility change, KOZ is found to

reach 15 um for n-type Si, while the mobility change is less than 5% in p-Si. With [110] channel alignment, the stress effect on mobility is reversed, with large mobility change and KOZ in p-type Si but small mobility change and no KOZ in n-type Si. The local plasticity is found to reduce the amount of mobility change and thus the size of the KOZ. More details of the KOZ study can be found in a separate publication [9].

SUMMARY

A wafer curvature method has been developed and used to study the stress characteristics of Cu TSV structures during thermal cycling. The stress characteristics of Cu TSVs were compared to that of Cu thin films and found to be distinctly different. First and foremost, the stress state in TSV is triaxial, while the stress in thin films is biaxial. For Cu thin films, with a biaxial stress state, the von-Mises stress is often sufficient to cause large-scale plastic yielding in the entire film. In contrast, with a triaxial stress state, the TSV behaves linear elastic with only localized plasticity near the top and bottom at the via/Si interface. Hysteresis loops were observed for thin films due to the large-scale plasticity during thermal cycling, while for the TSV structure, the localized plastic deformation had negligible effect on the overall curvature, and hysteresis loops were not observed. This led to a large residual stress in the Cu TSV at the end of the cooling cycle, making significant impact on the keep-out zone for devices. The residual stress was found to be determined by the stress relaxation occurring during the heating cycle, which is controlled in turn by grain growth in the Cu TSV, depending on the peak temperature in the heating cycle. Since grain growth in Cu is primarily controlled by the electroplating process, the results suggest the possibility to reduce the residual stress in TSV by optimizing Cu electroplating, particularly its chemistry.

Another important result is the finding of local plasticity at the Cu/Si interface near the TSV surface, which can induce via extrusion without interfacial delamination. Synchrotron X-ray microdiffraction was performed and local plasticity was observed in individual TSVs. This provides a new and distinct mechanism for via extrusion. The result suggests that via extrusion can be mitigated by optimizing the microstructure of the Cu TSV to control the local plasticity. The understanding of the local plasticity and the via extrusion mechanism is important for improved reliability of the Cu TSV structures.

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