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Integrated Temperature Sensors in Deep Sub-Micron CMOS Technologies

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Integrated Temperature Sensors in Deep Sub-Micron CMOS Technologies

by

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Dedication

Dedicated to my late parents,

Mansur A. Chowdhury and Aziza B. Chowdhury

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Integrated Temperature Sensors in Deep Sub-Micron CMOS Technologies

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The University of Texas at Austin, 2014

Supervisor: Arjang Hassibi

Integrated temperature sensors play an important role in enhancing the performance of on-chip power and thermal management systems in today's highly-integrated system-on-chip (SoC) platforms, such as microprocessors. Accurate on-chip temperature measurement is essential to maximize the performance and reliability of these SoCs. However, due to non-uniform power consumption by different functional blocks, microprocessors have fairly large thermal gradient (and variation) across their chips. In the case of multi-core microprocessors for example, there are task-specific thermal gradients across different cores on the same die. As a result, multiple temperature sensors are needed to measure the temperature profile at all relevant coordinates of the chip. Subsequently, the results of the temperature measurements are used to take corrective measures to enhance the performance, or save the SoC from catastrophic over-heating situations which can cause permanent damage. Furthermore, in a large multi-core microprocessor, it is also imperative to continuously monitor potential hot-spots that are prone to thermal runaway. The locations of such hot spots depend on the operations and instruction the processor carries out at a given time.

Due to practical limitations, it is an overkill to place a big size temperature sensor nearest to all possible hot spots. Thus, an ideal on-chip temperature sensor should have

minimal area so that it can be placed non-invasively across the chip without drastically changing the chip floor plan. In addition, the power consumption of the sensors should be very low to reduce the power budget overhead of thermal monitoring system, and to minimize measurement inaccuracies due to self-heating.

The objective of this research is to design an ultra-small size and ultra-low power temperature sensor such that it can be placed in the intimate proximity of all possible hot spots across the chip. The general idea is to use the leakage current of a reverse-bias *p*-*n* junction diode as an operand for temperature sensing. The tasks within this project are to examine the theoretical aspect of such sensors in both Silicon-On-Insulator (SOI), and bulk Complementary Metal-Oxide Semiconductor (CMOS) technologies, implement them in deep sub-micron technologies, and ultimately evaluate their performances, and compare them to existing solutions.

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Chapter 1: Motivation and Outline

1.1 MOTIVATION

Over the past few decades, the semiconductor industry has seen a revolutionary increase in computing performance due to the dramatic increase of integration following the trend predicted by Gordon Moore [1-2]. With the scaling of technology, today's highly integrated SoCs (System-on-Chips) and microprocessors, integrate more components on a smaller chip; yet they continuously offer more processing power at higher speeds than ever before. Due to the aggressive scaling along with higher level of integration, and increased operating speed, the power consumption per unit area of an integrated circuit (ICs) is increasing very fast, and the projections for future generations suggest a rise in Central Processing Unit (CPU) power [3]. The power of a chip is dissipated mainly as heat. Therefore, increased power consumption can lead to higher junction temperatures, which in turn can affect the device performance, and in case of over-heating the reliability of a chip [4]. The power and thermal management of high-power density chips is therefore becoming imperative; yet it remains costly and challenging.

Dynamic Voltage-Frequency Scaling (DVFS) is an on-chip technique used for many years in both high-performance computing (e.g., servers and desktops) and power-efficient mobile (*e.g.*, laptops and smart phones) applications to manage thermal limits by dynamically adjusting the power consumption levels [5]. Generally speaking, DVFS depends on continuous monitoring of on-chip thermal profiles using on-chip temperature

sensors. As a result, integrated temperature sensors are becoming an integral part of all high-performance SoCs as they are an integral part of any thermal management (and DVFS) system.

While implementation of on-chip sensors is a simple concept, the actual implementation of them in the context of DVFS is extremely challenging. Today's massively integrated SoCs which include millions of transistors include many different functional blocks that consume power very in-homogeneously. Hence, it is common to see a large and time-varying thermal gradient across SoCs. Furthermore, in some specific architecture (*e.g.*, microprocessors), burst operations are common which can result in localized hot spots. Excessive heat from such local hot spots may result in rapid device aging, lower reliability, increased electro-migration, and even total chip failure.

Managing the dissipated heat, and temperature profile of the chips is also important in power-efficient computing platforms. The main reason is that these systems, unlike, desktop, mainframes, and stationary systems; do not have high-performance and reliable heat sinks. To avoid thermal runaway scenarios that can cause irreversible damage, the temperature across the chip in these applications should also be continuously monitored by deploying multiple temperature sensors, and adjusting the performance accordingly.

It is important to recognize that independent of the application or platform, in all SoCs with DVFS, temperature information is not used for managing the heat dissipation only, but it is also being leveraged to maximize the overall performance. For example, in multi-core microprocessors, the workload is continuously shuffled between different

cores before the temperature rises to a critical level. Alternatively, the clock rate and/or voltage level is dynamically adjusted to boost system performance within a certain thermal budget [6-7].

Since integrated temperature sensors do not participate in the main activities of the SoC, *e.g.*, in the computing operations of a microprocessor, but rather, play an auxiliary role of on-chip temperature measurement, their area should be kept small to reduce cost, broadly defined. In addition, their power consumption should also be very small which will also help to reduce error in temperature measuring caused by self-heating. Such criteria make the design of such sensors difficult as they have a tradeoff with the accuracy and response-time, *i.e.*, larger area sensor with a high power budget exhibit high accuracy and fast response time.

The desired number of sensors in a SoC, their exact coordinates on the die, and their performance, depend greatly on DVFS algorithm, integrated circuit (IC) packaging, and cooling system (if any). The particular application that is targeted in this research is a highly integrated multi-core processor which requires many sensors on multiple locations across the die to monitor the temperature profile of the chip. Particularly, the focus is on the sensor block implementation.

Creating integrated temperature sensors using deep sub-micron Complementary Metal-Oxide-Semiconductor (CMOS) digital processes is not an easy task. Such processes are mainly optimized for logic functions and digital processes, and neither analog nor sensing functions. Therefore, one needs to deal with challenges like reduced voltage headroom, increased process variations, and increased transistor leakage [8]-[9].

In this dissertation, the concept, design, and implementation of an extremely small and ultra-low power temperature sensor are presented. Because of its ultra-small size and extremely low power, many of these sensors can be placed on the chip to reliably monitor the on-chip thermal profile. The general idea is to use the temperature dependent reverse-bias leakage current of a *p-n* diode to monitor the thermal profile of the chip. In this sensor, the diode junction capacitance is first charged to a fixed voltage. Subsequently, the diode capacitance is allowed to self-discharge through its temperature dependent reverse-bias current.

In the first implementation of the sensor in a 32nm Silicon-On-Insulator (SOI) technology, the temperature dependent diode discharge time is measured using a Time-to-Digital Converter (TDC). Finally, a single-bit first-order delta-sigma modulator is implemented in which the self-discharging *p-n* diode is used as the integrator. The temperature dependent reverse-bias current of the *p-n* diode is measured at the output of the modulator with an off-chip digital filter. As the diode reverse-bias current is related to the temperature, so the chip temperature can be extracted if this current is measured accurately. Thus, the accuracy of such a sensor depends on the accuracy of the current measured at the output of the modulator. This implementation was carried out in an 180nm technology. The delta-sigma based sensor is designed with the objective of making it like of a standard cell because of its small size and low power. Hence, it would be very easy to place this standard cell of temperature sensor in the closest proximity of all hot spots. In this implementation, an array of such sensor standard cell is placed on the chip. The goal is to characterize each one of these sensors.

1.2 OUTLINE

Chapter 2 reviews the integrated temperature sensors in the context of their roles in monitoring the on-chip thermal profile of microprocessors with DVFS. The additional role of integrated temperature sensors in managing on-chip power in systems utilizing DVFS is also highlighted in this chapter.

To understand the need for a new approach to integrated temperature sensor design to assist in on-chip thermal and power monitoring, an understanding of existing solutions is required. Chapter 3 studies various temperature sensor design architectures with their merits and demerits.

The design, simulation, and implementation of a sensor with a *p-n* diode in a 32nm SOI CMOS technology are presented in Chapter 4. The post silicon results of this sensor are compared with the existing sensors targeting similar applications.

In order to improve the temperature measurement, we propose a first-order delta-sigma architecture-based sensor. An overview and basics of delta-sigma modulation is presented in Chapter 5.

The design, simulation, and implementation of a sensor based on a first-order single-bit delta-sigma modulator are presented in Chapter 6. The architecture of this design uses a reverse-bias *p-n* diode, and it was implemented in an 180nm bulk CMOS technology. Chapter 7 is dedicated to the summary of this dissertation, and future works.

Chapter 2: Integrated Temperature Sensors

2.1 INTRODUCTION

With the evolution of integrated circuit fabrication, temperature sensors are being integrated on-chip for various applications. Such integrated on-chip temperature sensors are widely used in measurement, instrumentation, and control systems. Research in developing application-specific temperature sensors is currently driven by some key applications. Few examples of such key applications are, monitoring of food, and other perishables with Radio-Frequency Identification (RFID) tags [10]-[13], temperature compensation of Micro-Electro-Mechanical Systems (MEMS) resonators in integrated clock reference chips [14]-[16], and thermal management of large SoCs [17]-[19].

Temperature sensors in RFID tags need to be low-cost, and their power consumption has to be ultra-low. MEMs frequency reference circuits employ temperature compensation based on temperature reading of accurate on-chip temperature sensors. MEMS resonators are designed to provide very accurate clock reference solutions. Thus, high accuracy, and high resolution temperature sensors are needed for MEMs resonators. In the case of on-chip thermal management of large SoCs, the temperature sensors must be able to monitor, and measure the temperature of all possible hot spots in real time. Due to the existence of large thermal gradients across their die, it is important that the temperature sensors reside in the closest proximity of the hot spots to sense, and measure the temperature [17], [20]-[21] accurately. As a result, their physical size must be small enough such that multiple of them can be placed on almost anywhere with little

limitations. Placement of many such small-size temperature sensors can provide better overall system level accuracy. This is despite the fact that small-size sensors are generally less accurate compared to large-size ones. In addition, their power consumption must also be low to limit the overall power budget, and also eliminate measurement inaccuracy due to self-heating.

2.2 TEMPERATURE SENSORS IN MULTI-CORE MICROPROCESSORS

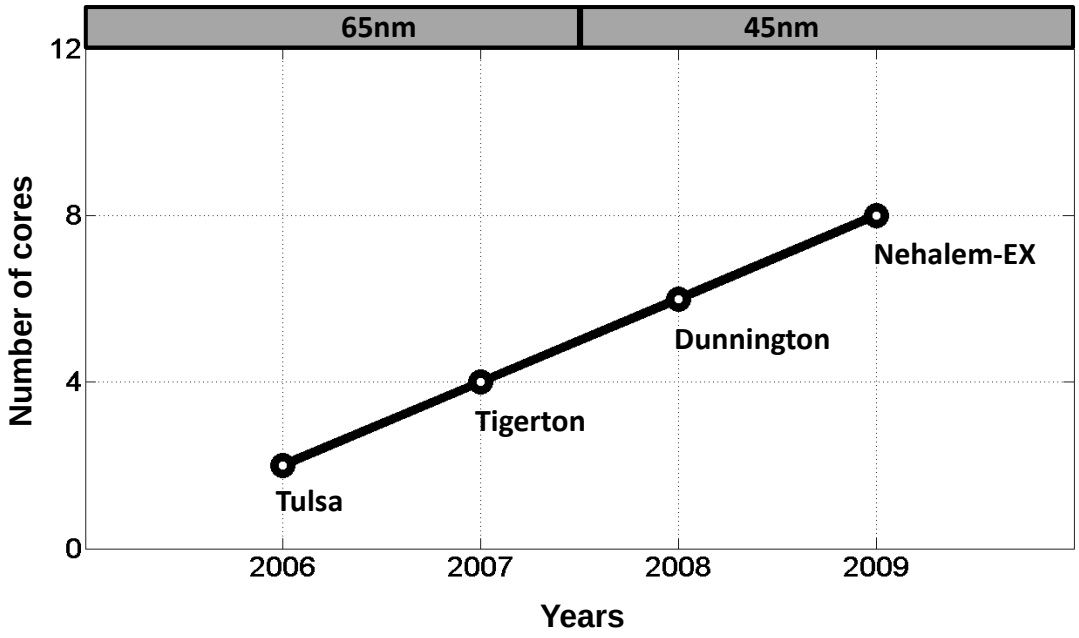

Figure 2.1: Xeon® EX processor core count trend.

In a multi-core microprocessor, multiple central processing units (CPUs) and graphics processing unit (GPU) are integrated onto the same chip. Due to aggressive integration, and technology scaling, the number of cores integrated on the same chip is increasing very fast while the total chip area is also scaling down. As an example, the

core count trend in Intel's Xeon EX processor is shown in Fig. 2.1[22]. It is evident from Fig. 2.1 that the core count per chip is increasing very fast as the technology is scaling down. In a microprocessor each core needs to have temperature sensors. Thus, as the number of cores in a microprocessor is increasing, it requires many sensors to monitor the thermal profile of the entire chip. This also demands that the sensors be very small in size, and their power consumption also be very low.

2.3 SENSORS FOR THERMAL AND POWER MANAGEMENT WITH DVFS

Dynamic voltage and frequency scaling (DVFS) [23]-[25] is a commonly used power management technique where the clock frequency of the processor is decreased to allow a corresponding reduction in the power supply voltage. This reduction of frequency, and supply voltage is typically performed sequentially in multiple steps. During DVFS the (dynamic) power consumption of the processor is significantly reduced which can lead to significant reduction in energy required for a computation. The relationship between dynamic power ($p_{dynamic}$) of a CMOS circuit, power supply voltage, and operating speed (frequency) is [26]

$$p_{dynamic} \propto C_L \cdot V_{DD}^2 \cdot f_{clk}. \tag{2.1}$$

Where, V_{DD} is the supply voltage, C_L is the load capacitance, and f_{clk} is the clock frequency. During the high performance computation the processor temperature can rise significantly due to the high dynamic power dissipation. The high power dissipation has the following disadvantages-

- High power systems tend to run hot, that causes the processor and other system components to fail if no corrective measures like DVFS or cooling (if any) are employed to bring the temperature down. The failure rate of a processor doubles for every 10°C rise in on-chip temperature [27].
- It complicates the cooling solutions of integrated circuits for heat removal, and thus increases the production cost. Intel estimates that more than $1/W per processor chip will be added once the processor power dissipation exceeds 35-40 W [28].
- It increases the operation costs; such as the electricity bills for air conditioning of the computer, and system rooms. 8% of US electricity in 1998 was attributed to the internet, which is projected to grow to about 30% by 2020 [29].
- It shortens the battery or UPS (Un-interrupted Power Supply) life. The processor power doubles every four years, consequently the average battery or UPS life will be shortened [30].

The major processor manufacture (Intel) has announced that the processor power dissipation doubles every four years [29]. Therefore Dynamic voltage frequency scaling (DVFS) is accepted as a technique to reduce power, and energy consumption of microprocessors by sequentially lowering the supply voltage, and operating speed (frequency). From Equation (2.1) it is evident that lowering the supply voltage is an effective way to reduce the power dissipation because of the quadratic relationship between power, and V_{DD}. Again, according to Equation (2.1), lowering only the operating frequency f_{clk} can reduce the power consumption, but the energy consumption remains the same because the computation needs more time to finish. Thus, lowering the supply

voltage, and operating frequency together reduces the power, and energy consumption further.

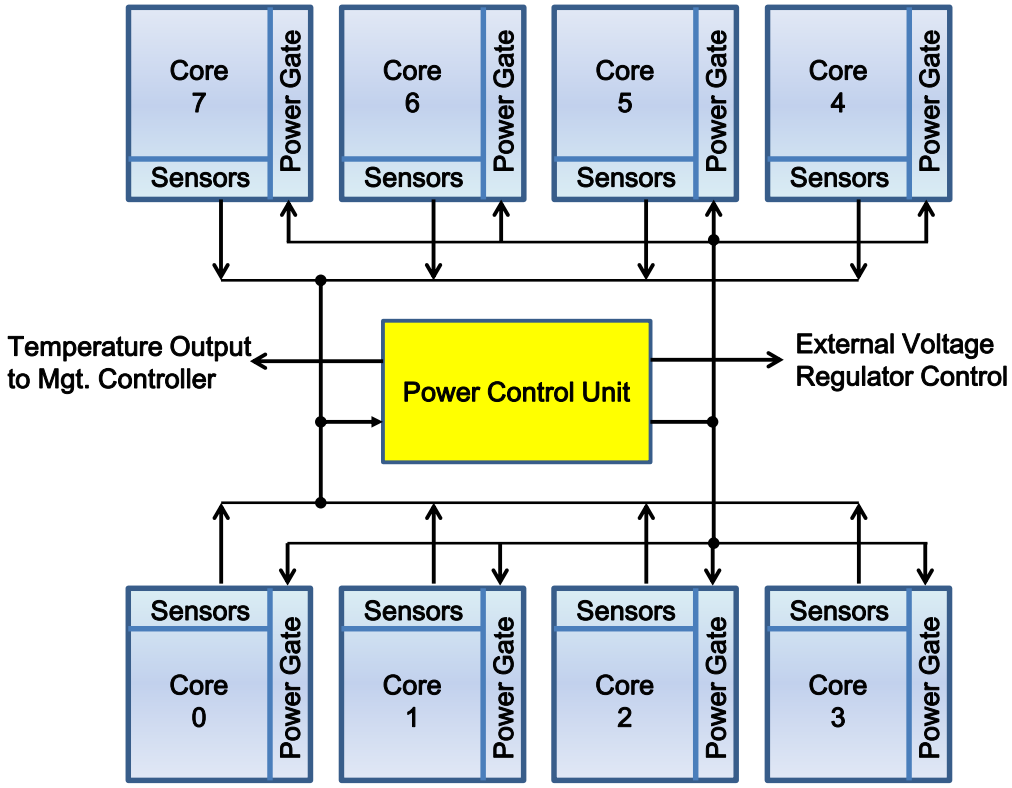

Figure 2.2: An integrated function of power and thermal control unit.

Fig. 2.2 shows an integrated function of power and thermal control units of a multi-core processor where multiple temperature sensors are placed in each core [22]. The temperature information from the sensors is used by the appropriate power and thermal management unit, for example DVFS, within the processor. When the temperature rises to the peak junction temperature of the devices, the sensors throttle the processor which activates the DVFS. The DVFS sequentially reduces the supply voltage, and frequency in steps until the chip cools down to a safe level, and then the processor is

allowed to go into high performance mode again. Fig. 2.3 illustrates the concept of operation of DVFS [22].

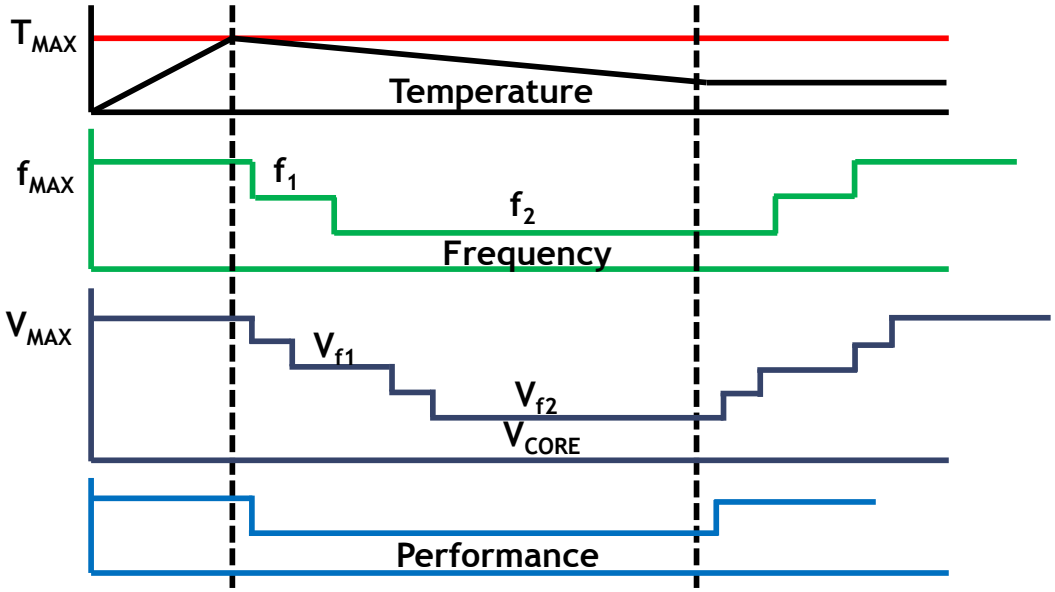

Figure 2.3: An Example of DVFS operation to manage on chip power and thermal profile.

If the temperature of the chip rises to some preset level (T_{MAX}) while the chip is operating at some maximum speed (F_{MAX}), and supply voltage (V_{MAX}), then DVFS reduces the supply voltage level, and frequency gradually until the chip cools down to a safe temperature level. During DVFS the chips operate at lower performance mode. The example of DVFS operation shown in Fig. 2.3 does not show the details of any label on the axes. The purpose of this figure is to simply show the basic concept of DVFS operation without any detailed and accurate information about the axes.

In multi-core SoCs the temperature information from the sensors is also used to manage the power dissipation by work load shuffling between the cores. When a core temperature rises to a dangerous level, then some of the high performance computational work load from it can be shuffled to another core which is not in a high performance mode at that time. Thus, the temperature sensor plays an important role in work load shuffling which balances the load between the cores of a multi-core processor to minimize the temperature gradient across the chip. This protects the cores from getting hot due to excessive power dissipation resulting from high performance work load.

Thus, the temperature sensors in a large SoC with multiple cores play the crucial role of monitoring, and measuring the on-chip temperature. The power and thermal management unit of the processor uses the temperature readings to activate the DVFS and/or work load shuffling to bring the processor temperature to a safe level. In applications with a built in cooling system (like a cooling fan) the temperature reading from the sensors is used to control the fan.

2.4 DESIGN CHALLENGES IN SUB-MICRON TECHNOLOGIES

Integrating temperature sensors into digital platform faces design challenges due to aggressive scaling. Temperature sensors in computing platforms must be fully integrated in a SoC where vast majority of the circuits are digital. Therefore, the sensors would be using the process technology which is aggressively scaled, and optimized for the digital logic. Analog circuit design in such process faces numerous challenges like reduced voltage headroom, increased transistor leakage, and wider process variations. Such challenges demand extra effort, and time to design analog intensive circuits in sub-

micron technologies, especially in deep submicron technologies. One objective of this research is to shift as much design as possible into the digital domain. This design approach can not only simplify the design task, but it can also reduce the design effort, and time.

Another important aspect of design is portability. That means a design is expected to be robust enough such that it can be ported from one technology node to another with minimum design change, and effort. This is very important for minimizing the time to market a product, and is certainly becoming more and more demanding in developing a product in sub-micron technologies. However, while it is much easier to port digital circuits from one technology node to another, the same is not true for analog circuits. Many design specifications, for example gain, bandwidth, stability of an amplifier, may not just stay the same when an analog circuit is ported to a different technology node. Analog circuits need to be re-designed, and re-simulated thoroughly which requires changes of some or all device sizes, even though the same architecture is used.

The primary target application of the temperature sensor of this research is in the digital platform. Therefore, it is expected that, along with the rest of the digital circuit, the sensor must be ready to port from one technology node to another with very little design change, and effort such that it does not become a road block to time to market. A digital design centric architecture for a temperature sensor would be the perfect choice to achieve this goal. As a result, in addition to small size, and low power consumption, the architecture of the temperature sensor of this research has been chosen to be digital centric.

Chapter 3: Existing Architectures for On-chip Integrated Temperature Sensors

3.1 INTRODUCTION

The block diagram of a typical temperature sensor is shown in Fig. 3.1. The temperature sensing circuit (transducer) produces an analog output, generally in the form of an analog voltage, in response to the temperature being sensed. This analog quantity is then converted into digital format through an analog-to-digital converter (ADC). The digital output is further processed and calibrated, if necessary, to produce the final output which represents the temperature being sensed. The detection range and accuracy of a temperature sensor depends greatly on the transducer and the sensing readout circuit which includes the ADC (or quantizer). In this chapter, the previously implemented on-chip integrated temperature sensor topologies are discussed including their achieved performances, merits, and limitations.

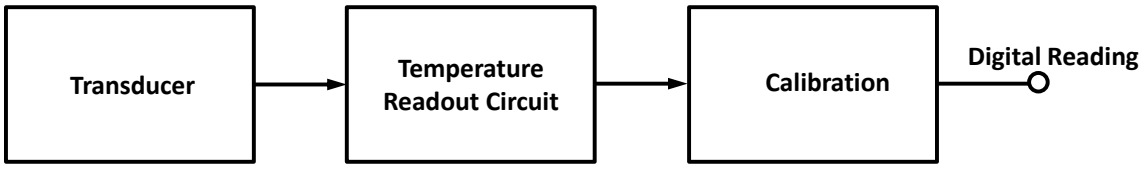

Figure 3.1: A Typical Temperature Sensor Architecture.

3.2 ON-CHIP TEMPERATURE SENSOR ARCHITECTURES

Various on-chip temperature-sensing circuit topologies have been proposed and implemented. Most of these systems rely on temperature dependent properties of integrated devices in silicon VLSI technologies as for their transducer component. Examples are MOS transistors, bipolar junction transistors (BJTs), and resistors. As a result, on-chip temperature sensor architectures and topologies are generally categorized based on their transducers. In the following, we review them in more detail.

3.2.1 Temperature Sensors with Forward Biased Bipolar Junction Transistors (BJTs)

The most widely used architecture for on-chip temperature measurement takes advantage of the proportional-to-absolute-temperature (PTAT) property of the voltage difference between two forward-biased BJTs; a structure which is generally referred to as thermal diodes [31]. In CMOS technology, parasitic BJTs with ratioed currents are commonly used in band-gap circuits to generate a constant reference voltage [32]. The same characteristics can be leveraged to create temperature sensors without requiring any extra fabrication step (or modification) in standard CMOS processes [33]-[35]. The three possible configurations of CMOS BJTs are shown in Fig. 3.2 [17]. The choice between *p-n-p* and *n-p-n* BJT depends on their availability in the process technology. As illustrated, in an NWELL-only CMOS process *p-n-p* BJT is the only choice, and to get an *n-p-n* BJT a triple well process is required.

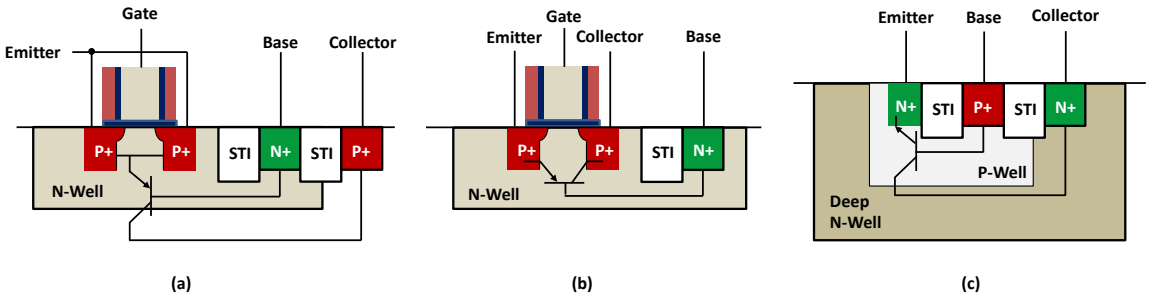

Figure 3.2: CMOS cross-section of (a) vertical *p-n-p* BJT, (b) lateral *p-n-p* BJT, and (c) vertical *n-p-n* BJT.

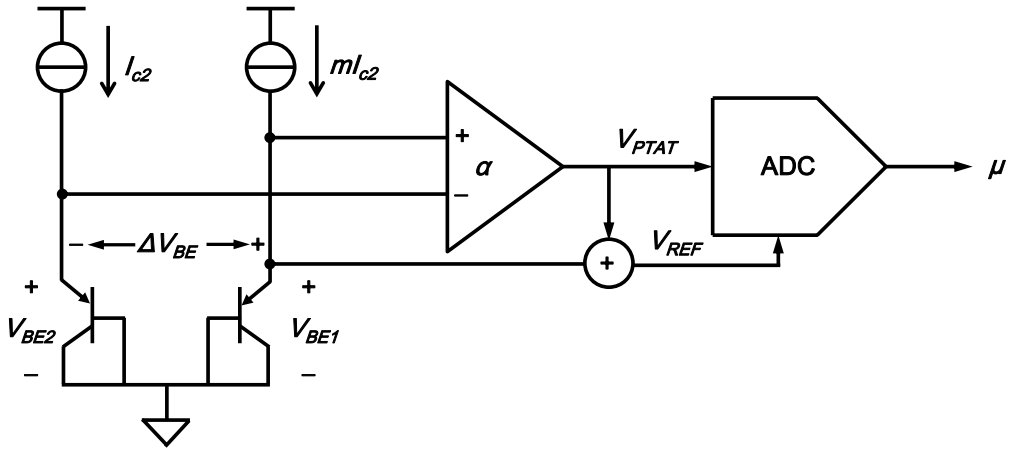

Figure 3.3: Block diagram of a *p-n-p* BJT temperature sensor.

The block diagram of a BJT based temperature sensor is shown in Fig. 3.3 [31]-[35]. A pair of currents with ratio m is used to bias the pair of BJTs having the same emitter area to develop voltages V_{BE1}, V_{BE2}, and ΔV_{BE}. The BJT voltages are expressed as

$$V_{BE1} = \frac{\eta kT}{q} \ln\left(\frac{mI_{C2}}{I_s}\right), \tag{3.1}$$

and

$$V_{BE2} = \frac{\eta kT}{q} \ln\left(\frac{I_{c2}}{I_s}\right), \tag{3.2}$$

Where, k is the Boltzmann's constant (1.38×10^{-23} J/^{0}K), η is the diode ideality factor (≈ 1.0), T is the absolute temperature in Kelvin, q is the elementary electric charge (1.60×10^{-19} Columb), and I_s is the diode reverse saturation current. I_{c2} and mI_{c2} are the two collector (emitter) biasing currents.

From Equations (3.1) and (3.2) it may appear that the diode base-emitter voltages have positive temperature co-efficient due to the presence of the temperature term T. However, the reverse saturation current I_s has a strong positive temperature dependency. As a result, V_{BE} has a negative temperature co-efficient. V_{BE} changes almost linearly with temperature with a slope of approximately -2 mV/^{o}C. Thus, it is possible to design temperature sensor that utilizes V_{BE} as an operand. However, I_s varies with process. The effect of the process variations can be compensated by trimming the bias currents, and thus normalizing the (I_c/I_s) term in the equation for V_{BE}. The diode ideality factor, η, is also a process dependent parameter, and it is typically close to unity.

In contrast, the differential voltage between the two base-emitter voltages is independent of the reverse saturation current, I_s. By combing Equations (3.1) and (3.2)

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = \frac{\eta kT}{q} \ln(m). \tag{3.3}$$

Which demonstrates that the output voltage, ΔV_{BE}, is proportional to the absolute temperature (PTAT), and the current ratio [33]-[35]. Typically, an analog-to-digital converter (ADC) is used to convert this PTAT voltage into digital format. Thus, the

output of the ADC represents the temperature, T. Temperature properties of various voltages of a BJT based sensor is shown in Fig. 3.4 [31].

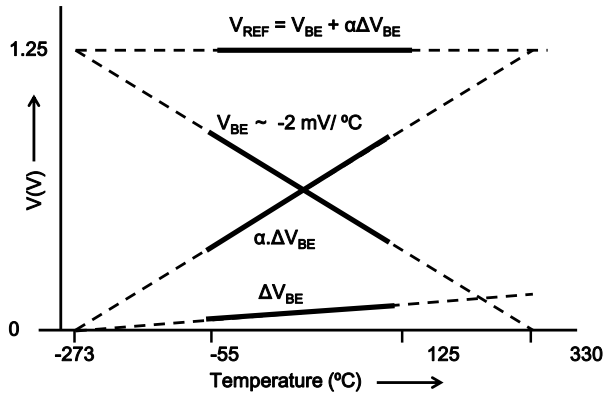

Figure 3.4: Temperature properties of voltages in a BJT temperature sensor.

The thermal sensitivity of the PTAT voltage ΔV_{BE} is very small. For example, for a current ratio of 10, and diode ideality factor η = 1.0, ΔV_{BE} changes by about 200 µV for each degree change of temperature. Thus, this type of sensor needs high precision data converter to accurately estimate the temperature. Typically, a switched capacitor based delta-sigma ADC is used in the sensor built with BJTs [31]. Due to the need for high precision, the ADC used in this type of sensors tends to be relatively large and power hungry.

As shown in Figs. 3.3 and 3.4, an appropriate gain factor α is used to generate a positive temperature dependent voltage V_{PTAT} ($\alpha.\Delta V_{BE}$), and a temperature independent reference voltage, V_{REF}. The delta-sigma ADC acts on these two voltages, and produces a digital output code μ which represents the temperature of the circuit. The reference voltage V_{REF} is approximately equal to the band-gap reference voltage (~ 1.25V).

The accuracy of BJT-based sensors depends on diode ideality factor, and accuracy of the current ratio of the two bias currents. Diode ideality factor is a process dependent parameter. Careful and meticulous layout for good matching alone cannot guarantee the required matching between the individual current mirrors to achieve the desired level of accuracy. Therefore, on-chip dynamic element matching, bias trimming, and post-fabrication calibration techniques are used in this type of sensor to improve accuracy. Any mismatch between the emitter areas of the two diodes contributes to sensor inaccuracy. Typically, bigger physical sizes with multiple unit devices are used to match between the two diodes which increase overall area of the sensor.

The biggest advantage of the BJT based temperature sensors is that the PTAT voltage ΔV_{BE} is directly proportional to the temperature being measured. However, for the aforementioned reasons, while this specific class of on-chip temperature sensors tend to be accurate, they have to be large, and power hungry, resulting in reduced benefit from advanced technology (e.g., below 65nm CMOS).

Standalone BJT based temperature sensors have been successfully implemented [36]-[39]. After on-chip trimming and calibration they can achieve 3σ inaccuracy of a fraction of a degree of temperature [37]. BJT based temperature sensors have also been implemented in large SoCs, like microprocessor in submicron technologies. The 3σ inaccuracy of such sensors can be several degree of temperature [38]-[39].

3.2.2 MOSFET-based Temperature Sensors

Many physical properties of MOSFETs have temperature dependency. As a result, MOSFET-based temperature sensors have been successfully implemented by utilizing the temperature sensitivities of the various MOSFET physical properties.

The relationship between the drain current and gate to source voltage of a MOSFET operating in sub-threshold region can be expressed as [40]

$$V_{GS} - V_{TH} = \left(\frac{skT}{q}\right) \ln\left(\frac{I_D}{I_0}\right). \tag{3.4}$$

I_0 is a process dependent parameter, I_D is the drain current, and s is the sub-threshold slope factor. A VCO based low-power temperature sensor using MOSFET-based sensing devices operating in sub-threshold mode has been recently proposed as an alternative choices to BJT-based sensors [41].

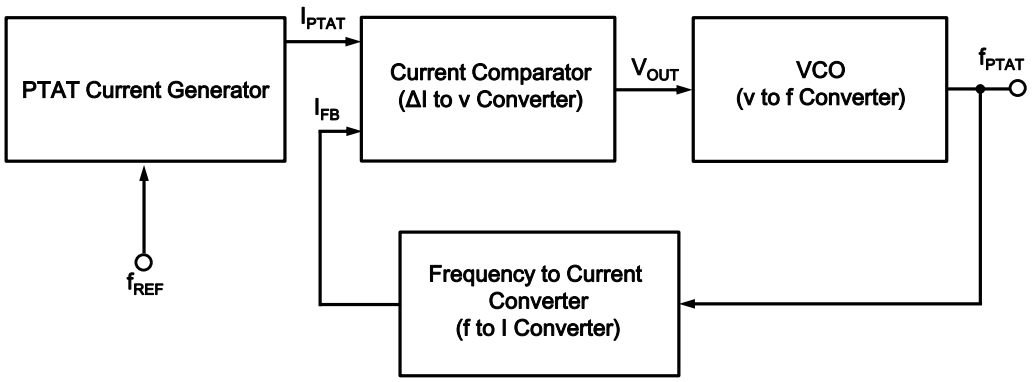

Figure 3.5: Block diagram of a MOSFET based sensor.

The block diagram of the MOSFET based sensor is shown in Fig. 3.5 [41]. The operation is based on creating a PTAT current, which is a linear function of temperature, using the circuit illustrated in Fig. 3.6. It can be shown that PTAT current of this circuit, denoted by I_{PTAT}, is [41]

$$I_{PTAT} = \frac{skT}{qR_{sc}} \ln\left(\frac{K_2}{K_1}\right), \tag{3.5}$$

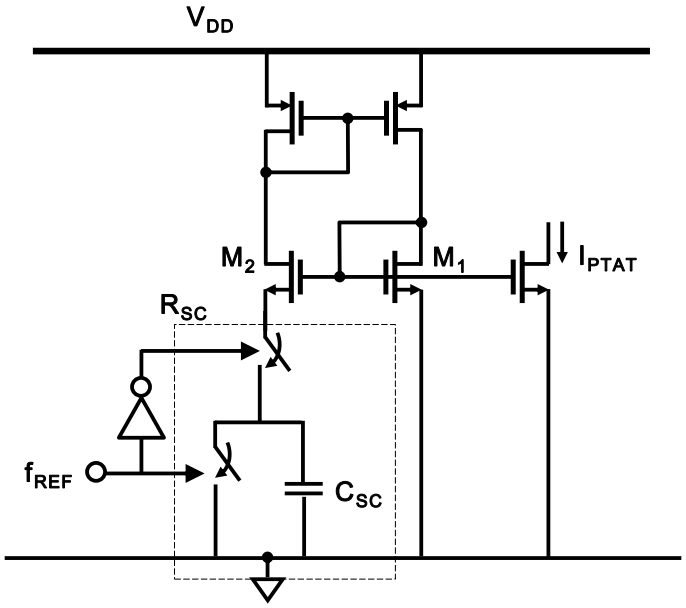

Figure 3.6: The PTAT current generator of the sensor presented in Fig. 3.5.

The resistor R_{SC} is defined as

$$R_{SC} = \frac{1}{f_{REF} \cdot C_{SC}}, \tag{3.6}$$

Using Equations (3.5) and (3.6), finally I_{PTAT} can be expressed as

$$I_{PTAT} = \left(\frac{skT}{q}\right)(f_{REF} \cdot C_{SC}) \ln\left(\frac{K_2}{K_1}\right). \quad (3.7)$$

where, s is the sub-threshold slope factor, R_{sc} is a switch capacitor resistor implemented by using the external clock f_{REF}, and an on-chip switched capacitor C_{SC}, K_1, and K_2 are the aspect ratio of the transistors M_1 and M_2 respectively operating in sub-threshold.

The external reference clock f_{REF} of Equation (3.7) is independent of temperature. Thus, in sub-threshold mode I_{PTAT} is PTAT. The current comparator converts the difference of this I_{PTAT} current and the feedback current I_{FB} into a voltage which is used to drive the voltage controlled oscillator (VCO). When the loop is stable and locked, I_{PTAT} and I_{FB} become equal, and at that point f_{PTAT} represents the temperature. After a one temperature point calibration an accuracy of ±1.8°C was obtained over the temperature range of 10°C to 80°C [41].

In another approach, a time-to-digital converter (TDC) based temperature sensor has been implemented in which the time it takes for the MOSFET sub-threshold current to charge a capacitor to a fixed threshold is measured. After an initial batch calibration, a one-point calibration of individual sensors was performed to achieve inaccuracies of a few degrees over the limited temperature range of 40°C to 90°C [42]. Yet, the size and power consumption of this sensor is too high. The inaccuracy was improved to ±1°C after a two-point calibration over the range of -10°C to 30°C [43]. An auto-calibrated all digital CMOS temperature sensor has been introduced in [44] that utilizes a TDC to generate the final digital output. This sensor is relatively small, and it consumes less power. However, it operates over the limited temperature range of 0°C ~ 60°C with the

measurement error bounded by -5.1°C ~ 3.4°C. Even with calibrations, these types of sensors are not as accurate as BJT based sensors due to excessive process variations, and their temperate range is also very narrow. They require expensive multi-point calibrations to increase their accuracy.

A dual delay locked loop (DLL) based all digital temperature sensor has been proposed to remove the effects of process variations with calibration at only one temperature point [45]. A reference clock with a multiphase delay line is used to generate a fixed delay to calibrate the temperature measurement errors. Thus, the calibration cost at high volume production can be reduced. However, the temperature sensors with dual DLLs occupy too large chip area and they consume excessive power at milliwatt level.

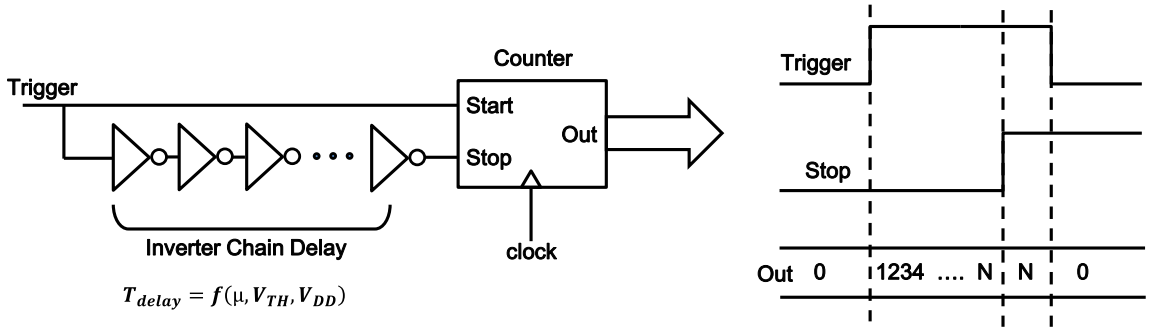

Figure 3.7: Block diagram of a temperature sensor based on the delay of a chain of inverters.

Temperature sensors have also been implemented by using the temperature dependent propagation delay of CMOS inverters. Fig. 3.7 shows the block diagram of

such a sensor [46]. The average propagation delay of a CMOS inverter with equal strengths of PMOS and NMOS devices can be expressed as [46]

$$T_p = \frac{(L/W)C_L}{\mu C_{OX}(V_{DD}-V_{TH})} \ln\left(\frac{3V_{DD}-4V_{TH}}{V_{DD}}\right). \quad (3.8)$$

Where W and L are the width and length respectively of the PMOS and NMOS devices of the inverter, C_{OX} is the oxide capacitance, and C_L is the load capacitance of the inverter. The temperature dependent parameters are the mobility, μ, and the threshold voltage V_{TH}. If the supply voltage V_{DD} is constant and much bigger than V_{TH}, then the temperature dependence of T_p will be mainly determined by the temperature dependence property of mobility. The temperature dependence of mobility is expressed as [46]

$$\mu = \mu_0 \left(\frac{T}{T_0}\right)^{km}. \quad (3.9)$$

In Equation (3.9), T is the actual temperature to be measured, T_0 is a reference temperature, and km is a constant between -1.2 to -2.0. Because mobility has a negative temperature co-efficient as expressed in Equation (3.9), the propagation delay of the inverter in Equation (3.8) has a positive temperature co-efficient.

As evident in Equation (3.8), the propagation delay also varies with the variations of V_{DD} and V_{TH}. In addition, the temperature dependency of the mobility is not fixed (km = -1.2 to -2.0). Hence, the propagation delay of an inverter suffers from variations of process and supply voltage. As a result, temperature sensors built with this architecture require multiple temperature point calibration. The temperature sensor implemented

based on inverter delay has achieved inaccuracies of about ±0.5°C over the range from 0°C to 90°C with a fixed supply voltage and after a two-point calibration [47].

In submicron technologies, the propagation delay is expected to vary more over process variations, and the accuracy of this type of sensor would be worse requiring more rigorous calibrations. Thus, though simple in architecture, the actual implementation of MOSFET based sensors would be costly.

3.2.3 Resistor-Based Temperature Sensors

Integrated temperature sensors have been implemented that use on-chip temperature-variant resistor (thermistor) [48]-[51]. In the implementation of [48] illustrated in Fig. 3.8, a temperature-dependent poly resistor is used to generate a temperature-dependent current. A current-controlled (starved) ring oscillator driven by this bias current is then used to produce a digital output representing the on-chip temperature. The bias current generator of the upper part of the sensor, shown in Fig. 3.9(a), uses a poly resistor which varies almost linearly with temperature. The current starved inverter chain based ring oscillator of the sensor shown in Fig. 3.10 produces oscillations (f_{osc}) proportional to the bias current I_{source} (I_{sink}) given by [48]

$$f_{osc} = \frac{I_{source}}{NV_{DD}C_L}. \tag{3.10}$$

Where N (=5) is the number of inverters in the ring oscillator, C_L is the load capacitance seen by the inverters, and V_{DD} is the power supply. In this implementation, I_{source} and

f_{osc} vary inversely with temperature. This means, the pulse width (time period) of f_{osc} is a linear function of temperature.

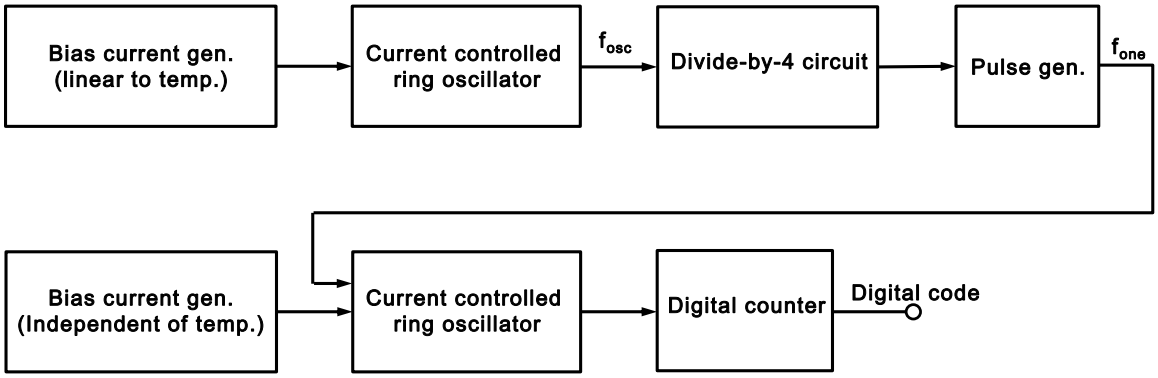

Figure 3.8: Block diagram of a resistor-based temperature sensor.

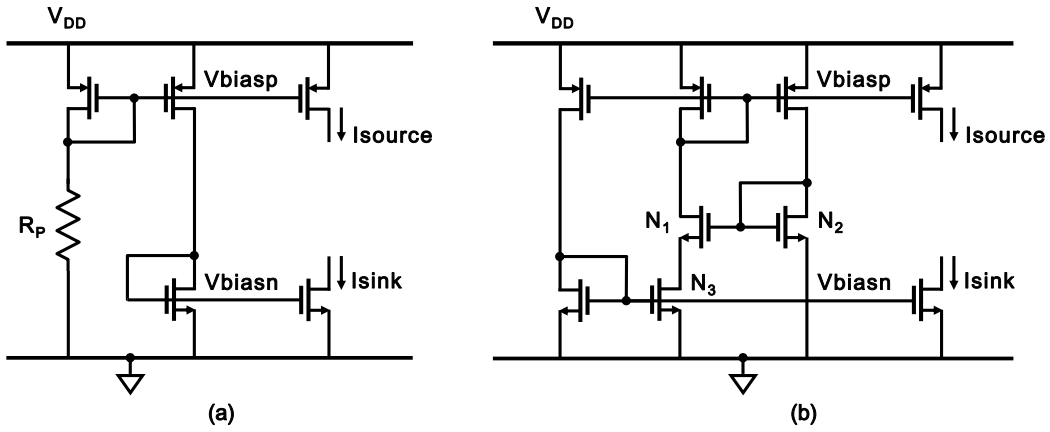

Figure 3.9: Linear to temperature dependent bias current (a) and almost independent of temperature bias current (b).

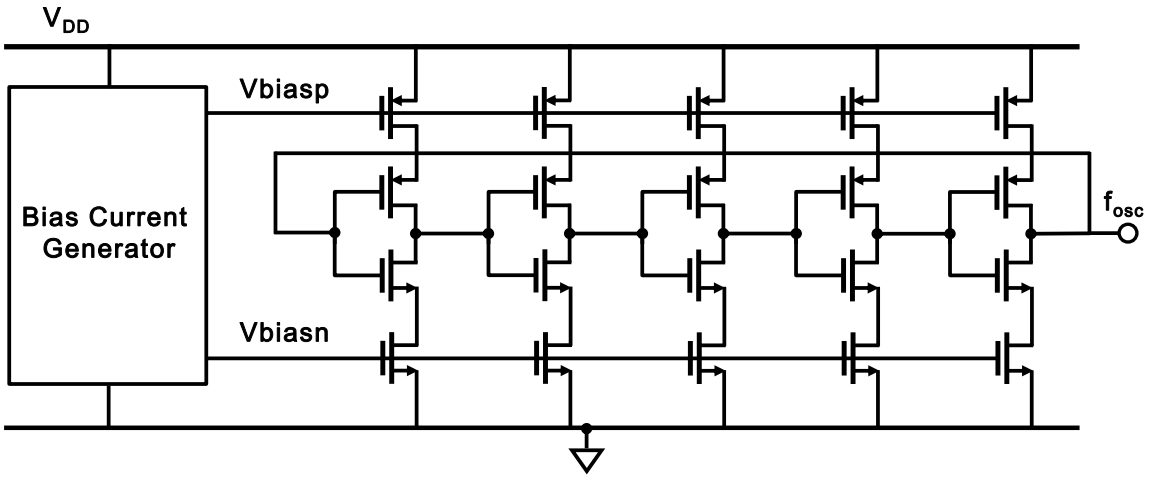

Figure 3.10: Current starved inverter chain based ring oscillator.

The lower part of the sensor in Fig. 3.8 uses the same ring oscillator as the upper part of the sensor. The temperature independent bias current generator is shown in Fig. 3.9(b). To minimize power, transistors N_1 and N_2 are operated in sub-threshold region, and N_3 is operated in linear region. The divide-by-4 circuit in Fig. 3.8 divides down f_{osc} by a factor of 4, and the pulse generator of the upper part selects a single cycle pulse (f_{one}) from this low frequency clock. The ring oscillator of the lower part produces a high frequency clock (f_{out}) that is almost temperature independent, but it is activated only during the time interval of the temperature dependent single pulse (f_{one}). The digital counter counts the temperature independent clocks of the lower ring oscillator during the time interval of the temperature dependent single pulse producing the final digital output corresponding to the on-chip temperature.

Resistor based temperature sensor can achieve relatively good accuracy though they need calibration because on-chip resistor vary with process, and temperature. The physical size of resistor based sensor is high and their power consumption is also high.

In another implementation, a thermistor based temperature to digital converter was implemented to provide accurate and low-noise compensation of temperature induced variation of MEMS resonant frequency [51]. The temperature to digital converter included a tunable switched-capacitor resistor, a multi-bit quantizer, a digital delta-sigma modulator, a Phase Locked Loop (PLL). The temperature sensor in this MEMS-based oscillator was the key component to provide temperature stability better than ±0.5 ppm over a -40°C to +80°C temperature range. However, this level of high accuracy came at the expense of about 13.1 mW of power consumption at 3.3V supply in 180nm CMOS.

3.2.4 Thermal Diffusivity Sensor

Temperature can also be sensed by measuring the thermal diffusivity of silicon which is strongly temperature-dependent [52]. As shown in Fig. 3.11, a thermal diffusivity sensor is created by realizing a heater and a temperature sensor embedded in the same silicon substrate [52]. Electrical signal (f_{drive}) applied to the heater induces local temperature variations in the substrate, through which they diffuse, and after a delay are being detected by the temperature sensor.

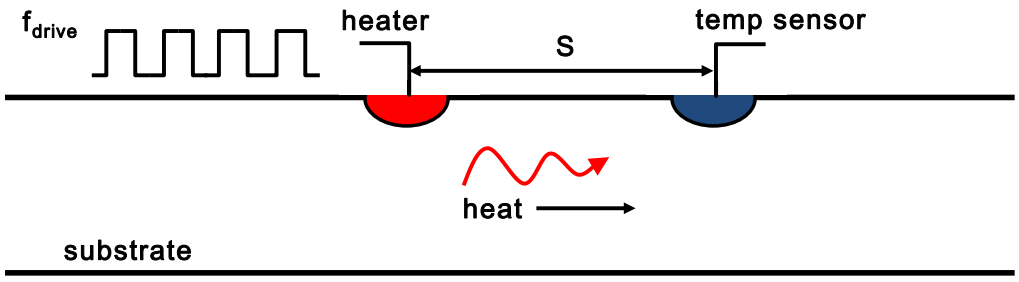

Figure 3.11: Cross-section of a thermal diffusivity sensor.

Thermal diffusivity of pure silicon substrate has a strong temperature dependency which is defined as [52]

$$D_{si} \infty \frac{1}{T^{1.8}}. \tag{3.11}$$

In this implementation, the heater is made up with n^+ diffusion resistor, and p^+/Al (p^+ diffusion and Aluminum) thermopile is used as the temperature sensing circuit inside the sensor. The distributed R-C (resistor and capacitor) of the substrate acts as a low pass filter creating a temperature dependent phase shift of f_{drive} defined by

$$\emptyset \infty S\sqrt{\frac{f_{drive}}{D_{si}}} \quad \infty T^{0.9}. \tag{3.12}$$

Where s is the distance (spacing) between the heater and the sensor. The sensor uses a phase digitizer based on a Δ-Σ modulator to digitize the phase shift and produces the final digital output. Temperature sensors built with this idea [52] reported good accuracy but their size is very big, and they consume too much power.

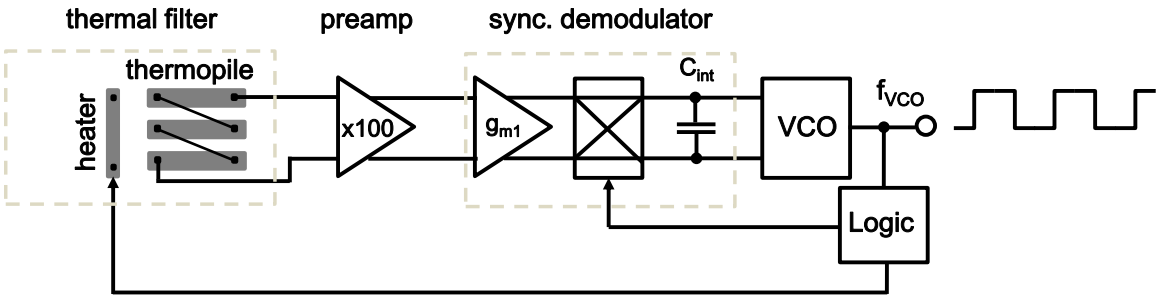

Figure 3.12: Practical implementation of the electro-thermal FLL.

In another implementation, a temperature to frequency converter (TFC) was implemented in which an n^+ diffusion resistor was used as a heater while the temperature sensor was a thermopile realized in p^+ diffusion/aluminum thermocouples [53]. The output frequency is determined by the phase shift of the electro-thermal filter formed by the heater, and the temperature sensor. The filter's phase shift is determined by the geometry of the thermal path between the heater and the sensor, and by the temperature dependent rate at which the heat diffuses through the substrate. The filter was used as the frequency-determining component of a frequency-locked loop (FLL), whose output frequency is then a well-defined function of temperature. Using this approach, a TFC with an inaccuracy of ±0.5 C (3σ) over the industrial temperature range (-40°C to 105°C) has been realized in a standard 0.7 μm CMOS process. The practical implementation of this sensor is shown in Fig. 3.12, and it consists of a preamplifier with a gain of 100 [53].

The output of the preamplifier is then applied to a synchronous demodulator consisting of a transconductor, g_{m1}, a chopper, and an integrating capacitor C_{int}. Finally the VCO (voltage to frequency converter) produces the final frequency output f_{VCO}. In the practical implementation, the preamplifer, synchronous demodulator, and two electro-thermal filters were implemented on a 2.3 mm^2 chip. The on chip electronics dissipates (excluding the heaters) 2.5mW power from a 5V supply. VCO and the heater driver logic were implemented off-chip [53].

3.3 REMOTE AND DISTRIBUTED ON-CHIP TEMPERATURE SENSING

MOSFET-based sensors typically consume less power, but they depend on the temperature dependent properties of transistor threshold voltage, mobility, and biasing current, all of which vary with the process. Thus, they require calibration at multiple temperature points to achieve the desired level of accuracy. Lightly doped N-well and poly resistors (thermistors) are used in the resistor based sensors. But their temperature dependence is not well defined, and they too require calibration at multiple temperature points to achieve desired accuracy. The size and power consumption of the thermal diffusivity sensor is very high. For these reasons, these sensors are not used in microprocessor applications which need many sensors to be deployed across their chips to monitor the temperature.

Existing on-chip thermal monitoring solutions for the multi-core processors employ the technique previously presented in Fig. 3.3 using parasitic BJT devices. Fig. 3.13 shows an implementation of an Intel temperature sensor in 32nm bulk CMOS Hi-K metal gate [54], and Fig. 3.14 [54] shows the circuit used to implement the BJT sense stage. Due to large physical size and power consumption of the sensors their placement close to the hot spots becomes very expensive, and prohibitive. As a result, remote sensing is employed by placing the BJTs close to the hot spots, and by placing the Δ- Σ ADC based core analog circuit in a less congested region. A pair of forward biased BJTs (remote sensors) is placed close to each hot spot. The BJTs are forward biased with a pair of currents from the central bias generation circuits as shown in Fig. 3.14.

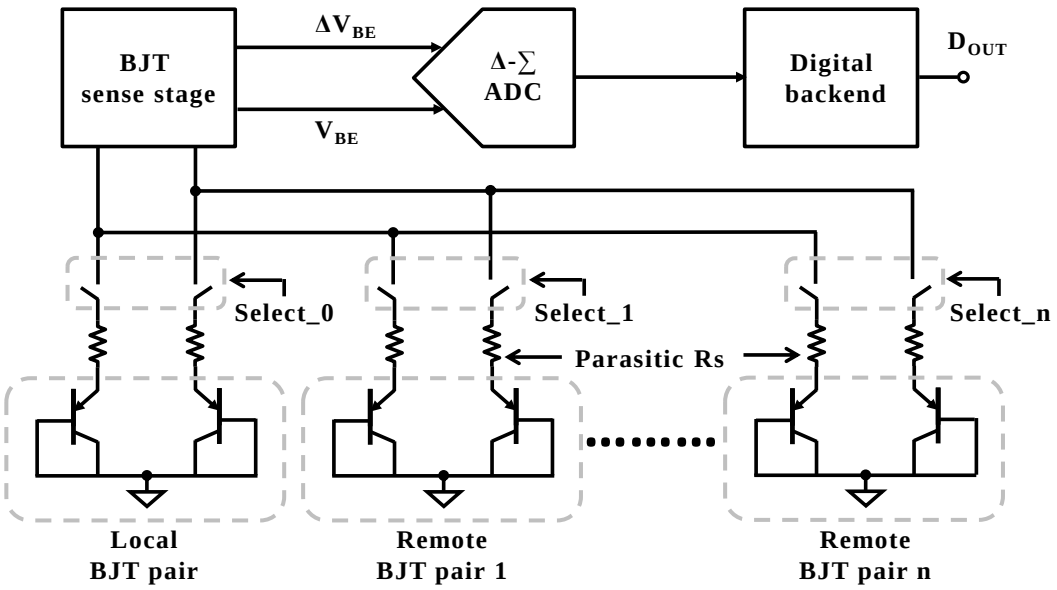

Figure 3.13: Block diagram of a temperature sensor with remote sensing.

The forward biased BJT pair (with a current ratio of say 10) is relatively large in size. The differential voltage ΔV_{BE} across the pair of the remote sensor diodes is digitized by the ADC. Typically a delta-sigma (Δ-Σ) ADC is used as shown in Fig. 3.13. The ADC in Fig. 3.13 has to measure the voltages (V_{BE}, and ΔV_{BE}) of all the remote sensors.

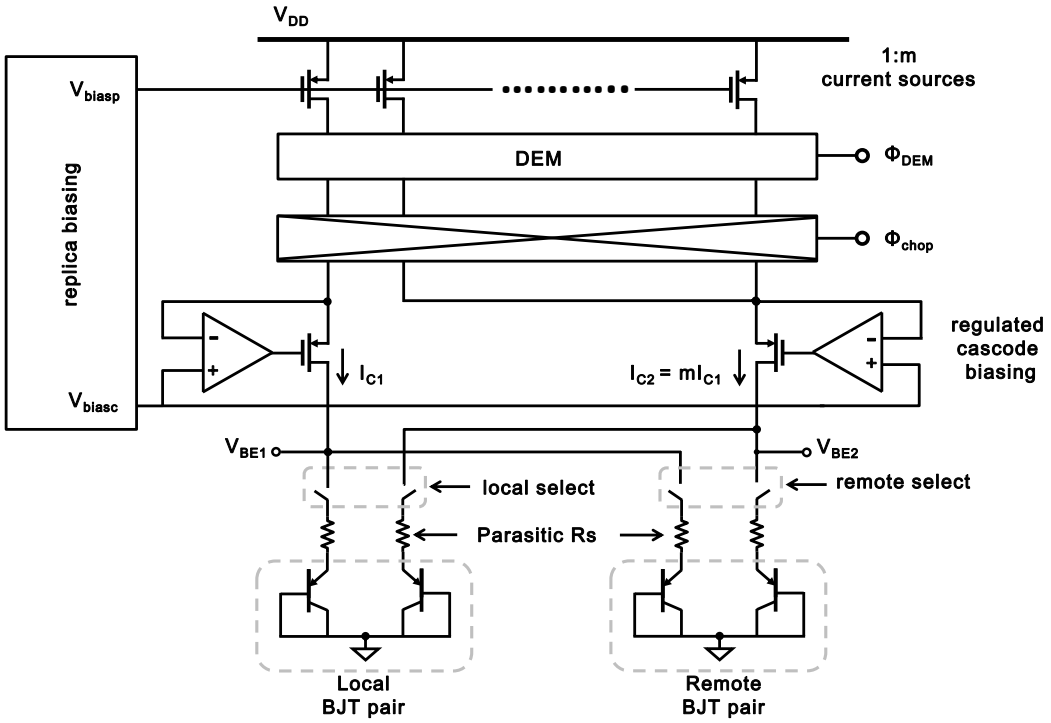

Figure 3.14: Circuit inside the BJT sense stage to provide the biasing currents to the sensors.

Due to the long routes between the BJT sense stage and the remote sensors, the sampling of these voltages by the ADC is slower. In addition, the routings between the sense stage and the ADC can also be quite long. The routing of these analog signals must be done very carefully to avoid possible coupling with the digital signals which are common in a microprocessor. The ADC needs to measure all the remote sensors one at a time, thus the temperature readout speed is low. The total area and power of the thermal monitoring utilizing remote sensing are still very high. As a result due to physical size, power, and complexity of remote sensing, the sensors are not optimally placed close to all possible hot spots. Thus, the overall system level performance of thermal monitoring is still under optimized.

3.4 SUMMARY AND CONCLUSION

Sensor Type	Area (Size)	Power	Accuracy	Design Effort	Limitations / Challenges
BJT	Large	High	Good	Very High	Calibration Trimming
MOSFET	Medium	Low	Medium	High	Aggressive Calibration Curvature Correction
Thermistor	Large	Medium	Good	Medium	Calibration at multiple temperature points, Curvature Correction
Si Thermal Diffusivity	Large	Very High	Good	Very High	Calibration Trimming
Goal of this research	Ultra-Small	Ultra-Low	Good	Low	Calibration, Curvature Correction

Table 3.1: Qualitative comparison of existing thermal sensing solutions

A comparison between the different existing on-chip temperature sensing techniques is presented in Table 3.1. BJT-based sensors are the most widely used sensors as they offer good accuracy, but they require calibrations, trimming, dynamic element matching, and curvature corrections to achieve the desired level of accuracy. As a result, they are large in size and consume more power. Thermistor-based sensors also suffer from large area, and higher power consumption. While MOSFET-based sensors can consume comparatively less power, they are also large in size. Both thermistor and MOSFET-based sensors suffer from process variations, and they require costly calibrations at multiple temperature points to get the required level of accuracy.

Due to process variations, thermistor and MOSFET-based sensors are not used for

integrating into the microprocessor platforms. BJT-based sensors are facing increasing challenges for integration into multi-core processors due to their large size and high power consumption. Thus, there is a need to explore alternative thermal monitoring solutions for today's multi-core processors where temperature sensors can be placed in the closest proximity of all possible hot spots. If these sensors are tiny enough consuming very little power, and providing the final temperature outputs in digital format then they will be the most attractive solutions. They can be distributed across the chip increasing overall accuracy, and redundancy (reliability) of on-chip thermal monitoring. The redundancy is desirable, because if one sensor becomes non-functional or faulty, then the redundant sensor can support temperature measurement. Due to bigger size, and high power consumption of the BJT based sensor, today's multi-core processors cannot afford redundancy in placing extra sensors. Typically, one ADC is used per core to measure the remote sensors in that core, so if this ADC becomes faulty then the thermal monitoring of that core is at risk. This could be avoided if additional ADCs are used as redundant between the cores. However, due to size and power constraints it is very challenging to provide redundancy in today's multi-core processors.

Chapter 4: An On-Chip Temperature Sensor with a Self-Discharging Diode

4.1 INTRODUCTION

In this Chapter, the concept of the proposed temperature sensor using self-discharging diodes is presented. In addition, the design, on-chip implementation, and measurement results are presented. The proposed sensor presented here was built in GlobalFoundries 32nm SOI CMOS technology to be incorporated into a microprocessor system having multiple computing (CPUs) and graphics cores.

4.2 SELF-DISCHARGING DIODE TEMPERATURE SENSOR

This section describes the proposed sensor architecture in details. The architecture presented here is a basic architecture based on the idea of implementing a temperature sensor with a reverse-biased *p*-*n* junction diode. It is important to recognize that the same idea presented here can be used to develop other kinds of sensor architectures utilizing the temperature dependent reverse-bias current of a *p*-*n* junction diode as an operand. For example, Chapter 6 focuses on the implementation of a temperature sensor with a continuous time first-order delta-sigma modulator where the reverse-bias *p*-*n* diode acts as a continuous time integrator.

4.2.1 Basic Concept and Theory of Operation

The basic concept of the proposed sensor is shown in Fig. 4.1 [20]-[21]. The sensing circuit consists of a diode D, a capacitor $\boldsymbol{C_P}$, and a switch $\boldsymbol{S_1}$. The sensor uses the temperature-dependent reverse-bias leakage current of a *p-n* diode to monitor the temperature. In this topology, using the switch $\boldsymbol{S_1}$, the diode junction capacitance is first charged to a fixed voltage (V_C) which places the diode in the reverse-biased region. Subsequently, by opening the switch $\boldsymbol{S_1}$, the diode capacitance ($\boldsymbol{C_P}$) is allowed to self-discharge through the temperature-dependent reverse bias (leakage) current of the diode, denoted by $\boldsymbol{I_D}$. Next, by using a time-to-digital converter (TDC) the discharge voltage, $\boldsymbol{V_D(t)}$, is compared to a fixed voltage, and converted into a temperature-dependent time pulse (T_D) which is finally measured by a digital counter to evaluate temperature.

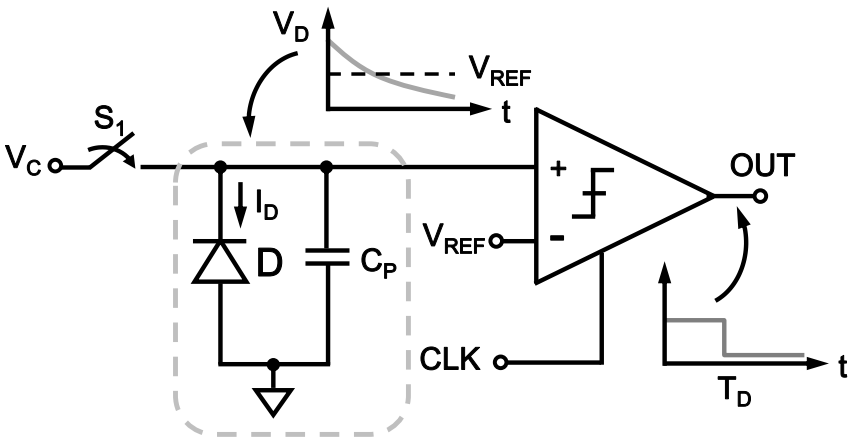

Figure 4.1: Proposed temperature sensor architecture.

4.2.2 Mathematical Formulation

The I_D–V_D relationship of a *p*-*n* junction diode is generally described by the following equation [55]

$$I_D = I_S\left[exp\left(\frac{V_D}{\eta V_T}\right) - 1\right], \tag{4.1}$$

where T is the absolute temperature in degree Kelvin, $V_T = kT/q$, k is the Boltzmann constant (1.38×10^{-23} J/°K), η (≈ 1) is the diode ideality factor, q is the electronic charge (1.6×10^{-19} coulombs), and I_S is the temperature-dependent reverse saturation current. When the diode is sufficiently reverse biased ($V_D/V_T \ll 0$), it can be assumed that $I_D \approx I_S$ (but flowing in the opposite direction). In this case, I_D can be approximated by the following semi-empirical relationship [56]:

$$I_D \approx I_S = AT^m exp\left(\frac{-E_g}{xkT}\right), \tag{4.2}$$

where A, m, and x are device-dependent constants, and E_g is the bandgap energy (*e.g.*, 1.12 eV for Si).

There is an important temperature characteristic for I_D in the reverse biased region. While Equation (4.2) describes a non-linear relationship between I_D and T, it is still monotonic with respect to T, and therefore it can be used to estimate the temperature T by measuring I_D.

Going back to Fig. 4.1, to initiate a temperature measurement, the switch S_1 is disconnected at time t = 0, and C_P starts to discharge by I_D. During this time, the voltage across the diode and capacitor, $V_D(t)$, becomes

$$V_D(t) = V_C - \int_0^t \frac{I_D}{C_P} dt. \tag{4.3}$$

For $V_D(t) \gg V_T$, *i.e.*, having sufficient reverse bias current during the discharge, I_D can be assumed to remain constant for a fixed temperature, and hence Equation (4.3) reduces to

$$V_D(t) = V_C - \frac{I_D}{C_P} t. \tag{4.4}$$

Now, if a voltage comparator continuously compares $V_D(t)$ with a reference (trip) voltage, V_{REF}, then its output will change after T_D seconds defined by

$$T_D = \frac{C_P}{I_D}(V_C - V_{REF} + V_{OS}), \tag{4.5}$$

where, V_{OS} is the offset voltage of the comparator. The comparator changes (flips) the state of its output when $V_D(t)$ discharges from its initial value V_C to the comparator trip voltage V_{REF} if there is no offset. While both V_{OS} and C_P are both weak functions of temperature, I_D is not, and it becomes the only dominant temperature-dependent term in Equation (4.5). Consequently, T_D can be measured using a time-to-digital converter (TDC) like circuit to estimate the temperature.

4.2.3 Time-to-Digital Convertor (TDC)

There are various techniques to convert analog signals into digital data. The most common method is to use an analog-to-digital Converter (ADC). An ADC typically converts an analog signal (voltage or current) into digital data. Recently, time-to-digital converters (TDC) have been developed to convert delay between two asynchronous edges of one or two pulses into digital format [57]-[58]. This approach is very simple, requires small circuitry, and consumes much less power compared to conventional ADCs. Assuming that one can convert the analog signal into time, one can take advantage of TDCs. The downside of TDCs is however, is that they always need an accurate reference clock to quantize time. In the proposed system, according to Fig. 4.3, a TDC has been implemented, which consist of a clocked dynamic comparator along with the self-discharging *p-n* diode. Section 4.3 explains this implementation in great detail..

4.2.4 *p-n* Junction Diodes in CMOS Processes

In today's CMOS technology there are more than one ways to fabricate a *p-n* diode. The cross-sectional views of a bulk CMOS diode, and a SOI CMOS diode are shown in Figs. 4.2(a) and 4.2(b), respectively [59]. The bulk diode of Fig. 4.2(a) is an area diode, meaning the current flow is through the center of the diode. In the poly bounded SOI diode, the current is flowing through the edge of the diode. To pass an identical current through a diode, a poly-bounded diode requires a larger space than a conventional diode in bulk CMOS [60].

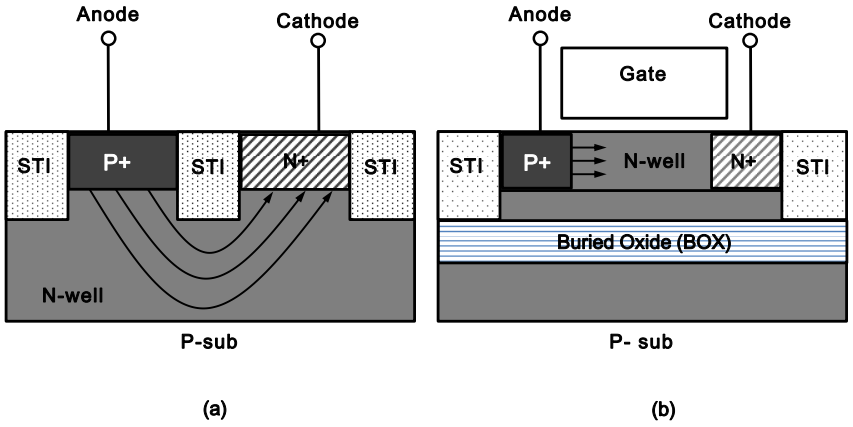

Figure 4.2: Cross-sectional view of a *p-n* diode showing the direction of current flow by the arrows in a (a) bulk diode, and (b) SOI diode.

4.3 CIRCUIT DESIGN OF THE PROPOSED SENSOR

The proposed sensor was first implemented in GlobalFoundries 32nm SOI CMOS process. This section gives the details of the transistor level design of the sensor. In this implementation, to create the first temperature-sensing diode *D*, a 25 μm^2 lateral SOI *p-n* diode is used.

4.3.1 The Transistor Level Schematic of the Sensor

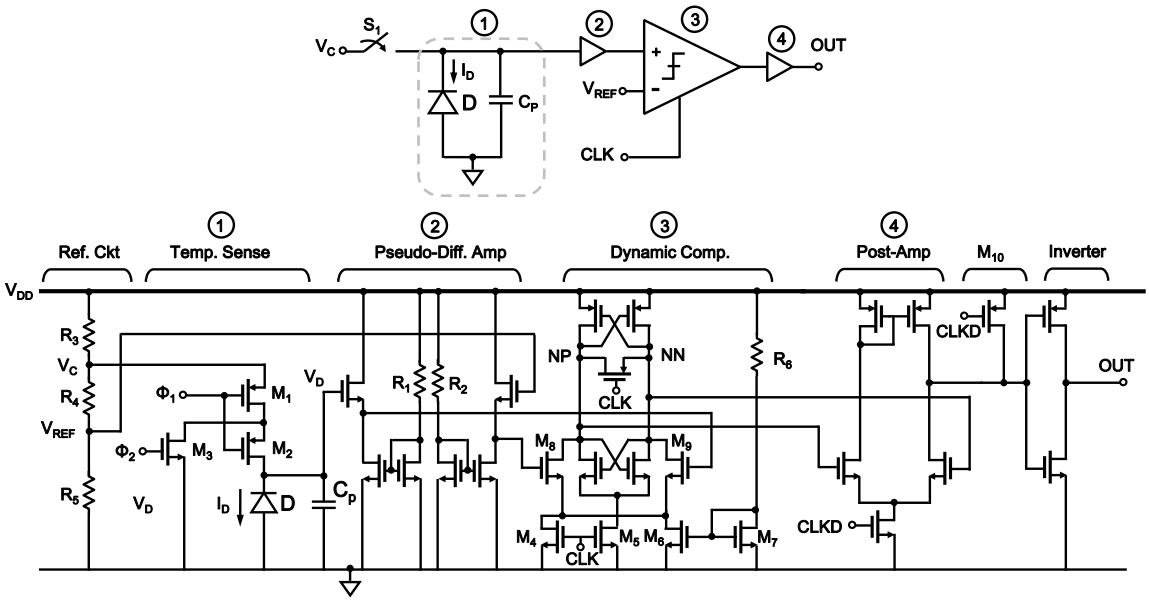

Figure 4.3: The complete transistor level schematic of the sensor.

The complete transistor level schematic of the designed temperature sensor implemented in a 32nm SOI CMOS technology is shown in Fig. 4.3. The sensor takes a clock (CLK), and a single pulse (Φ_1) as external inputs (in addition to power supply), and produces the digital output, OUT. Φ_2 is a delayed version of Φ_1, and it is generated on-chip from Φ_1 with cascaded inverters.

4.3.1.1: Reference Circuit

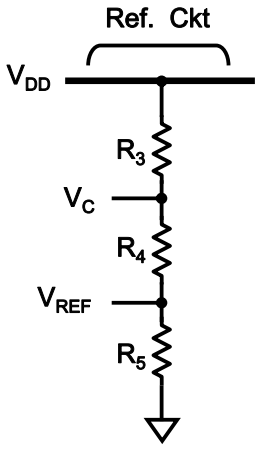

Figure 4.4: The reference circuit of the sensor.

To initiate the temperature measurement, the proposed sensor needs a fixed voltage V_C to reverse bias the sensor diode *D*. A reference voltage V_{REF} is used to set the trip point of the comparator. To start the temperature measurement, the diode is first biased (as well as C_P) with the voltage V_C, and then C_P is allowed to discharge through the reverse leakage current of the diode. The comparator output trips when the diode junction capacitance C_P is discharged from its initial value V_C to the comparator trip V_{REF}. As shown in Fig. 4.4, the reference circuit is implemented with three poly resistors, R_3, R_4, and R_5 connected between the power supply and ground. The voltages of the resistor network can be expressed as

$$V_C = V_{DD} \frac{R_4+R_5}{R_3+R_4+R_5}, \tag{4.6}$$

and

$$V_{REF} = V_{DD} \frac{R_5}{R_3+R_4+R_5}. \quad (4.7)$$

Obviously, voltages V_C and V_{REF} depend on the power supply V_{DD} and the resistor ratios. Yet, due to resistor ratio any process variations of the resistors will cancel out. To minimize the offset induced by the resistor mismatches, matched layout technique is also used and wider than minimum width resistors are selected. In the application of on-chip temperature sensing for microprocessors, the power supply V_{DD} is provided by on-chip regulators, and one can safely assume that V_{DD} remains fairly constant during the operation of the sensor.

4.3.1.2: Temperature Sensing Diode and Sampling Circuit

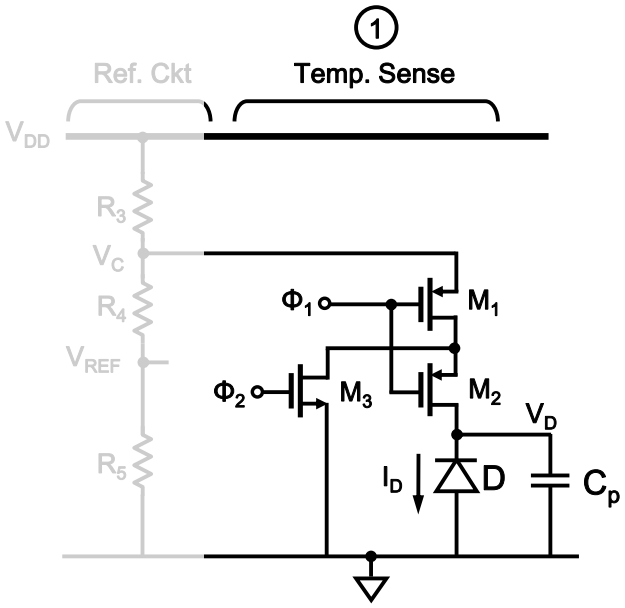

Figure 4.5: Temperature sensing diode, and sampling circuit of the sensor.

The temperature sensing diode, and its sampling circuit are shown in Fig. 4.5. As mentioned earlier, the temperature sensor D in this design is a 25 μm^2 lateral SOI *p*-*n* diode. The charge storing capacitor C_P, shown in Fig. 4.5, is essentially the junction capacitor of the diode, and to minimize the sensor footprint no explicit capacitor was used in this design. While it is a weak function of temperature, the junction capacitance, C_j, of a *p*-*n* diode depends on the diode voltage V_D, and it can be expressed as [61]

$$C_j = \frac{C_{j0}}{\left[1-\left(\frac{V_D}{\varphi_0}\right)\right]^m}, \tag{4.8}$$

where, C_{j0} is the total zero-bias capacitance of the *p*-*n* junction when the voltage across the diode is zero, φ_0 is the built-in potential, m is the gradient coefficient showing how silicon changes from *n*-type to *p*-type, and V_D is the diode voltage. It is evident from Equation (4.8) that the junction capacitance varies non-linearly with the diode voltage V_D. As an example, Fig. 4.6 shows this variation as a function of the diode reverse-bias voltage where it is assumed that C_{j0} = 0.5pF, and m = 0.33.

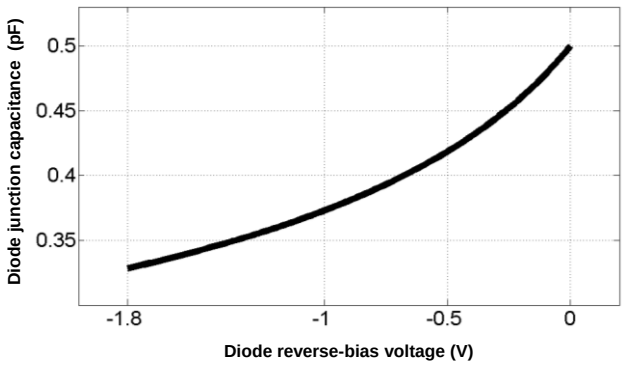

Figure 4.6: An example of diode junction capacitance as a function of its reverse-bias voltage.

As a result, as the diode voltage V_D discharges, the junction capacitor, C_P, varies in a non-linear relationship with the diode discharge voltage itself. This non-linear relationship of the discharge capacitor will introduce non-linearity in the final digital output of the sensor. Yet, it can be minimized by allowing the capacitor to discharge to a small voltage. In this design, the capacitor is allowed to discharge by approximately 200 mV. That means, the comparator trip voltage V_{REF} is set to about 200 mV below initial bias voltage, V_C.

To start the temperature measurement, the switch S_1 is used to first bias the diode D with the voltage V_C. The sampling circuit, responsible for the proper operation of the diode as a temperature sensor, is shown in Fig. 4.5 which consists of three transistors M_1, M_2, and M_3. At the beginning, when Φ_1 is low, the voltage across D is set to V_C through the reset switch, S_1, which consists of transistors M_1 and M_2 in series. In order to minimize switch leakage thick oxide devices are used for M_1 and M_2. When Φ_1 goes high (i.e., discharge time), M_1 and M_2 are turned off, and C_P starts getting discharged by I_D. It is possible to design the switch S_1 with only one transistor M_1. However, in deep sub-micron technology, like the 32nm technology used to implement the sensor, the transistors suffer from higher leakage currents (when they are turned off). Simulations show that during the off state of M_1, the V_{DD}-dependent channel leakage current of M_1 can charge up C_P and counter I_D. To prevent this, S_1 is designed by stacking M_1 and M_2, and the leakage path from V_{DD} into the diode discharge node V_D is bypassed through M_3 by applying Φ_2. While this fixes V_{DD} leakage, it creates an additional leakage path to the ground through $M_{2\text{-}3}$. By proper sizing of M_2 this leakage can be minimized, and in this design have been made negligible compared to I_D, making the discharge independent of transistor leakage and only a function of I_D.

4.3.1.3: The Isolation Buffer (Pseudo-Differential Amp)

The isolation buffer is shown in Fig. 4.7. To attenuate the kick-back voltage from the comparator into the diode discharge node, a self-biased pseudo-differential buffer (Amp) is placed between the diode discharge node and the dynamic latch. If the diode were connected directly to the dynamic (clocked) comparator, then during the clocking and switching of the comparator the diode discharge node (V_D) would be subjected to voltage kick-back from the comparator through the gate-drain capacitance of the input transistors of the comparator.

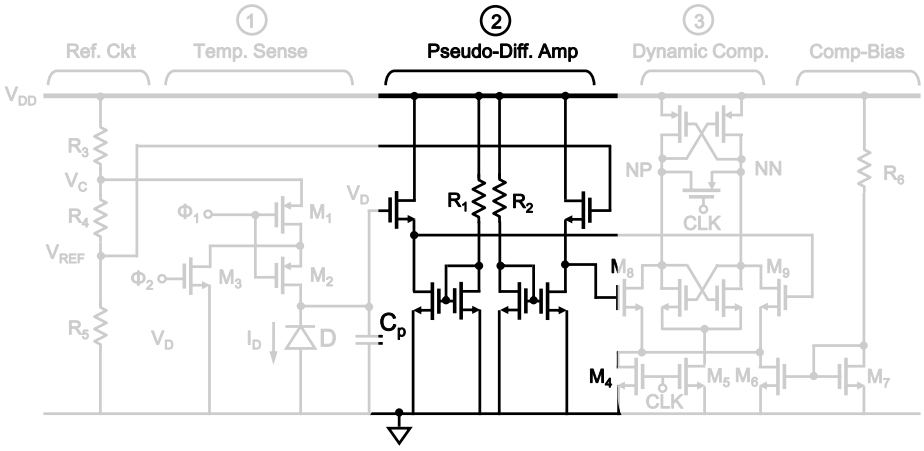

Figure 4.7: The pseudo-differential Amplifier as the isolation buffer.

The pseudo-differential amplifier also acts as a buffer between the diode and the comparator. Two matched resistors, R1 and R2, are used to bias the buffer. The buffer is basically a pair of single-ended source followers. The output of a source follower closely

follows its input, however its output is level shifted. Thus, the reference voltage of the comparator needs to be level shifter as well. This is the reason to use a pair of source follower, to buffer the diode and also the reference voltage, V_{REF}, of the comparator. This also prevents kick-back from the comparator into the reference circuit.

4.3.1.4: The Dynamic Comparator

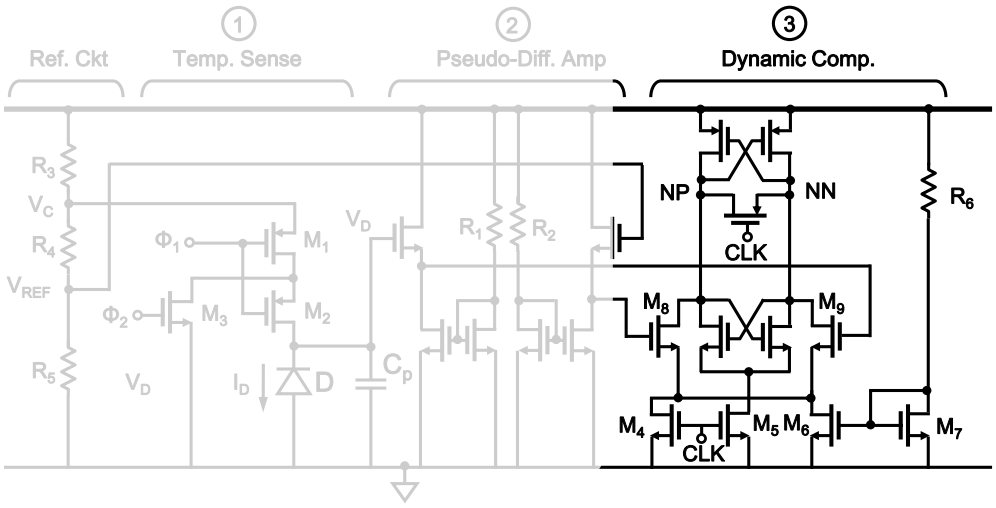

Figure 4.8: The dynamic comparator of the sensor.

A dynamic latch comparator with a transconductance input pair, as shown in Fig. 4.8, is used to compare $V_D(t)$ with the reference voltage, V_{REF}. The comparator consists of an input stage ($M_{8\text{-}9}$), two pairs of cross-coupled transistors, a reset transistor, transistors $M_{4\text{-}7}$, and a resistor R_6. During the reset phase (CLK = low), the outputs of the comparator (NP, NN) are shorted together with the PMOS reset switch to clear the memory effect. During the regeneration phase (CLK = high), the voltage imbalance at the

input of the comparator is amplified by the NMOS and PMOS cross-coupled regeneration loops. Transistor M_5 is turned off during the reset phase, preventing current flow from V_{DD} to ground through the cross-coupled pairs. This saves power by blocking current flow from V_{DD} during the reset phase of the comparator. At the same time, M_4 is also off, and R_6 and $M_{6\text{-}7}$ provide a low current bias for the PMOS cross-coupled pair as well as the comparator input stage that acts as the pre-amplifier.

4.3.1.5: The Post Amplifier (post-Amp)

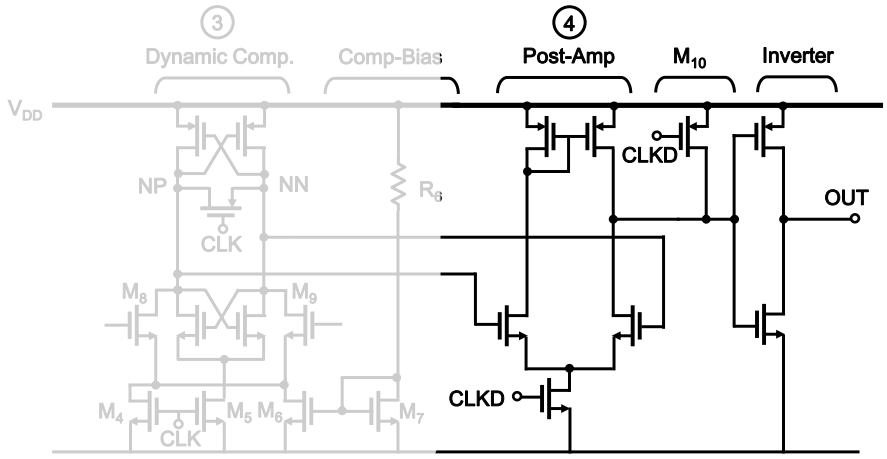

Figure 4.9: The post amplifier (Post-Amp) of the sensor.

The differential outputs of the dynamic comparator are converted into single-ended using a low-power, low-gain (~10) differential to single-ended amplifier (post-amp) which is shown in Fig. 4.9. This post-amp is turned on only during the regeneration phase of the comparator when CLKD is high where CLKD is a delayed version clock of CLK by ~100 psec. CLKD is generated on-chip from CLK using inverter chain to create

the ~100 psec delay. During the reset phase of the comparator, the post-amp is turned off, and its output is pulled high using the transistor M_{10} making the sensor output (OUT) low. OUT remains low as long as $V_D(t)$ is higher than V_{REF}, and it follows CLK after $V_D(t)$ passes V_{REF}. The inverter after M_{10} is used to simply invert the output of the Post-Amp to get the right polarity at the final output.

4.4 TIMING DIAGRAM AND PULSE DURATION

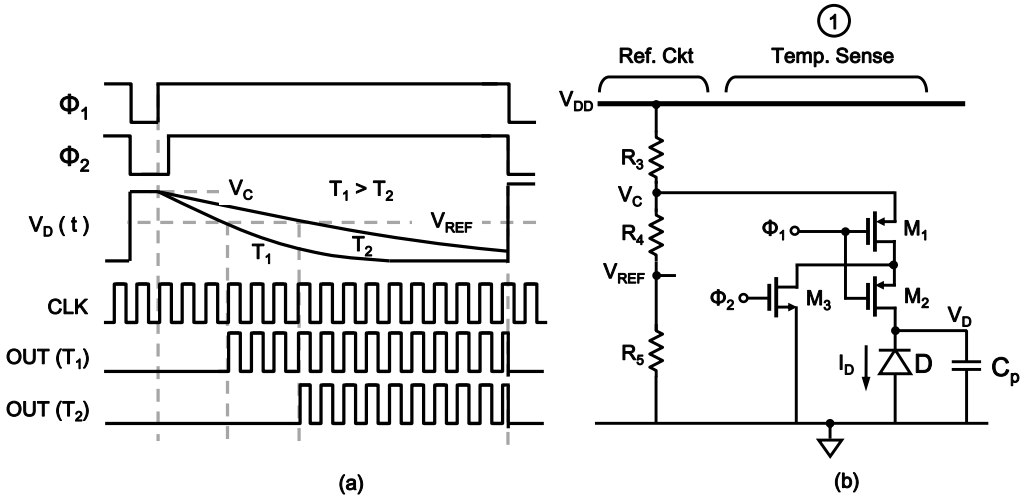

Figure 4.10: (a) The timing diagram of the first sensor in 32nm SOI, and (b) diode with the sampling and reference circuits.

The timing diagram of the sensor is shown in Fig. 4.10(a). To aid in explaining the timing of the sensor, the diode along with its sampling and reference circuits is shown again in Fig. 4.10(b). During the period when Φ_1 is low, the diode is biased with the voltage V_C ($V_D(t) = V_C$) through the sampling switch S_1 which consists of the transistors M_1 and M_2. Then the diode is allowed to self-discharge (when Φ_1 goes HIGH) through its

temperature dependent reverse leakage current I_D. As a result the discharge of the diode is temperature dependent. Fig. 4.10(a) shows the temperature dependent discharges for two temperatures, T_1 and T_2 ($T_1 > T_2$). The output of the sensor (OUT) follows the input clock (CLK) when the diode voltage V_D discharges to the comparator reference V_{REF}. As shown in Fig. 4.10(a), $V_D(t)$ for two different temperatures ($T_1 > T_2$) results in two different pulse density modulated (PDM) signals. The number of pulses in each signal is effectively the digital representation of T_D, and contains the required information to estimate the temperature *T*.

As shown in Fig. 4.10(b), both V_{REF} and V_C are generated on-chip by using V_{DD} = 1.65 V applied to a double-tapped resistor ladder and no "quiet" DC reference voltage is used in this sensor. Based on this topology and Equation (4.5), the diode discharge time T_D can be formulated as

$$T_D = \frac{C_P}{I_D}\left[\frac{(R_4+R_5)V_{DD}}{R_3+R_4+R_5} - \frac{R_5 V_{DD}}{R_3+R_4+R_5} + V_{OS}\right] = \frac{C_P}{I_D}(\alpha V_{DD} + V_{OS}), \quad (4.9)$$

where

$$\alpha = \frac{R_4}{R_3+R_4+R_5}. \quad (4.10)$$

According to Equation (4.9), any uncertainty associated with V_{OS} and V_{DD} will create errors in the temperature measurements. The approach to mitigate the errors caused by V_{OS} is to measure V_{OS} during an initial calibration phase, and then incorporate its value during the T_D-to-*T* transformation. As discussed before, no extra calibration is necessary to deal with V_{DD} variations, since in most SoCs (including the 32-nm

microprocessor here) V_{DD} is a very well regulated analog supply.

4.5 MEASUREMENT UNCERTAINTIES AND ERRORS

The temperature sensor implemented as an open loop system suffers from specific errors and measurement uncertainties that originate from various circuit components. The effects of these errors are minimized by employing certain IC design techniques. The remaining errors are minimized by post silicon calibration. The following section discusses these issues.

4.5.1 Errors Due to Nonlinearity

The following circuit components of the sensor of Fig. 4.3 contribute errors due to nonlinearity.

4.5.1.1 C_P Nonlinearity

The operation of the temperature sensor depends on the discharge of the C_P through I_D. Thus, it is expected that the discharge capacitor remain constant during the discharge so that the discharge is entirely dependent on the temperature. However, C_P is the inherent junction capacitor of the *p-n* diode. This was done to keep the sensor area small and add no extra (extrinsic) capacitor. The junction capacitor of a diode has a non-linear relationship with the voltage across the diode as expressed in Equation (4.8). According to Equation (4.8), and as has been demonstrated in Fig. 4.6, as the diode

continues to discharge its junction capacitance varies non-linearly with respect to the diode discharge voltage, V_D. In this design, the effect of this nonlinearity is minimized by allowing the diode to discharge to about 200 mV. The amount of diode discharge is set by the diode charging voltage V_C, and the comparator reference voltage V_{REF}. The difference between these two voltages is the amount by which the diode is allowed to discharge when a temperature measurement is taken. Even though it was not implemented in this design, this discharge limit can be made programmable with a digital control.

4.5.1.2 Nonlinearity of the Diode Sampling Circuit

The diode sampling circuit is built with transistors as switches. The switch on-resistance is non-linear with respect to the input voltage. In this implementation, the switch input voltage is always the same, which is V_C. As a result, with respect to the input, the switch on-resistance remains the same.

4.5.2 Errors Due to Offsets

Any offset introduced into the circuit will show up as an offset in the final output of the sensor. It is fairly easy to cancel the offset either on-chip, by introducing offset cancellation technique, or by post-silicon calibration in "software". Offsets of the isolation buffer, the comparator, and the post-amp are the main sources of offsets in this design. In order to keep the sensor size small, no offset cancellation techniques (like chopping or auto-zeroing) were used in this design and post-silicon calibration were selected. The sizes of the input transistors of the isolation buffer, comparator, and post

amp are chosen carefully to minimize the offset. Also layouts were done very carefully to provide very close matching of these transistors which also minimizes offset.

4.5.3 Errors Due to Charge Injection

At the end of sampling phase (when Φ_1 goes high) the sampling transistor M_2 will inject some charge into the diode discharge node V_D. This charge injection occurs every time the diode samples V_C (at the end of sampling phase), and it depends on V_C. Since the diode always samples the same V_C the charge injection will be same from one sample to another, and as such it will show up as an offset in the final output. This fixed offset due to charge injection can be calibrated out.

4.5.4 Leakage of the Sampling Switches

The transistors in this deep sub-micron technology have leakage currents when they are turned off. The leakage currents are due to the leakage through parasitic diodes, channel leakage, and gate leakage as well. The most critical transistors whose leakage can affect the accuracy of the sensor are those in the sampling circuit shown in Fig. 4.5. Two circuit techniques were used to minimize the switch leakage. First, thick-oxide transistors were used to make the switch. Thick-oxide transistors have a higher threshold voltage and they are less leaky compared to thin oxide transistors. Second, bigger channel lengths were used for the switching transistors to minimize their leakage.

4.6 LAYOUT AND FABRICATION

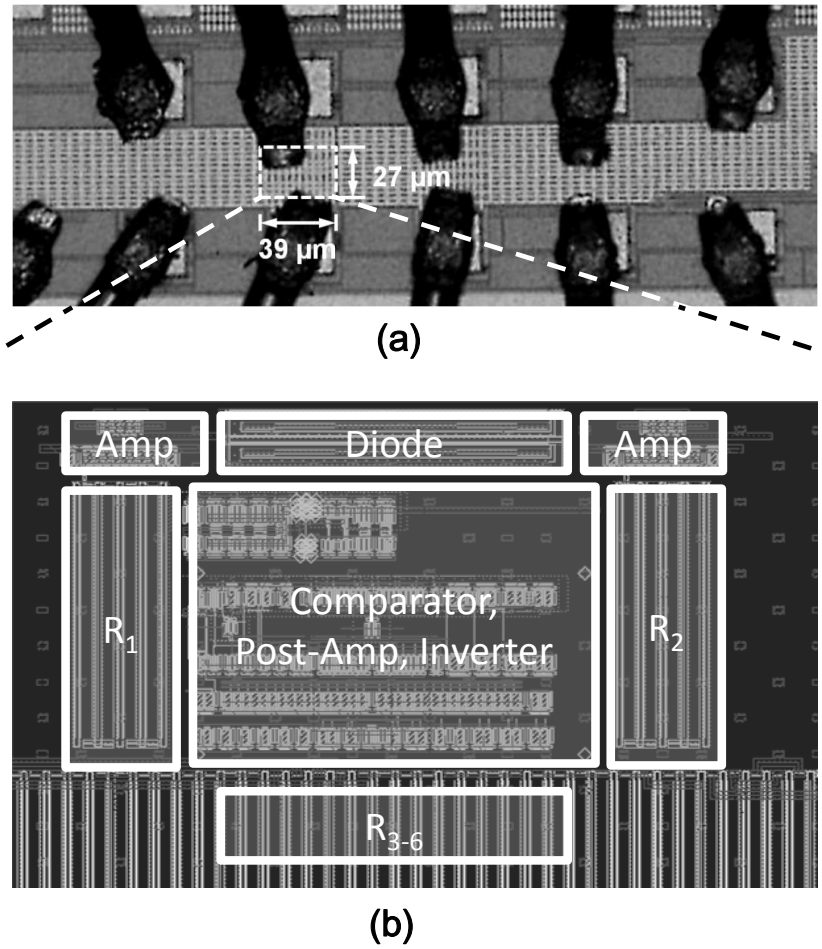

Figure 4.11 (a) Chip micrograph, and (b) layout of the on-chip temperature sensor.

The test chip micrograph, and the layout of the on-chip temperature sensor implemented in a GLOBALFOUNDRIES 32nm SOI CMOS process are shown in Figs.

4.11(a) and (b), respectively. This sensor occupies an area of 39 µm × 27 µm and consumes only ~100µW of power (including all the circuitry shown in Fig. 4.3) using a 1.65V supply when operating at 2.5k samples/sec.

4.7 MEASUREMENT RESULTS

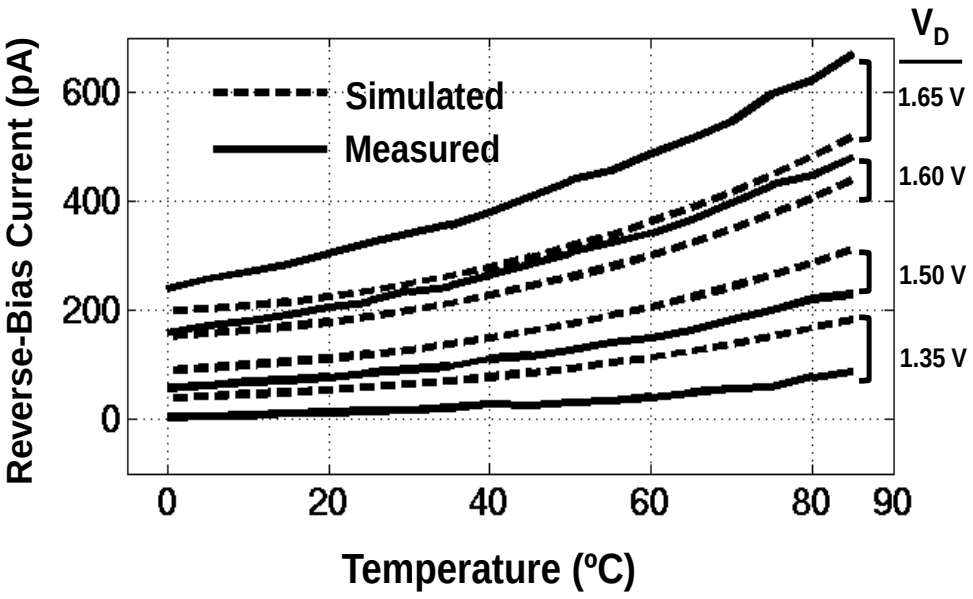

Figure 4.12: Simulated vs. measured diode reverse-bias currents for various V_D.

The packaged temperature sensor was characterized over the temperature range of 0º to 100ºC by submersing it in an oil bath. Temperature oil baths are very good standards in temperature measurements as they achieve very good temperature stability compared to bench top chillers (or heaters). During measurements, the silicon has to be soaked in special and non-conductive oil bath for a long period of time to allow the temperature to be stable and uniform across the oil chamber.

The simulated I_D for SOI lateral diode device and the measured values in a thermal oil-bath for the 0°C to 85°C temperature range are shown in Fig. 4.12. As expected, the measured reverse-bias current has a non-linear relationship according to Equation (4.2). However, there are discrepancies between the measured and simulated currents which are mainly due to modeling inaccuracies of the diode operating under reverse bias condition, specifically the lateral diode's effective surface area in the reverse-bias region.

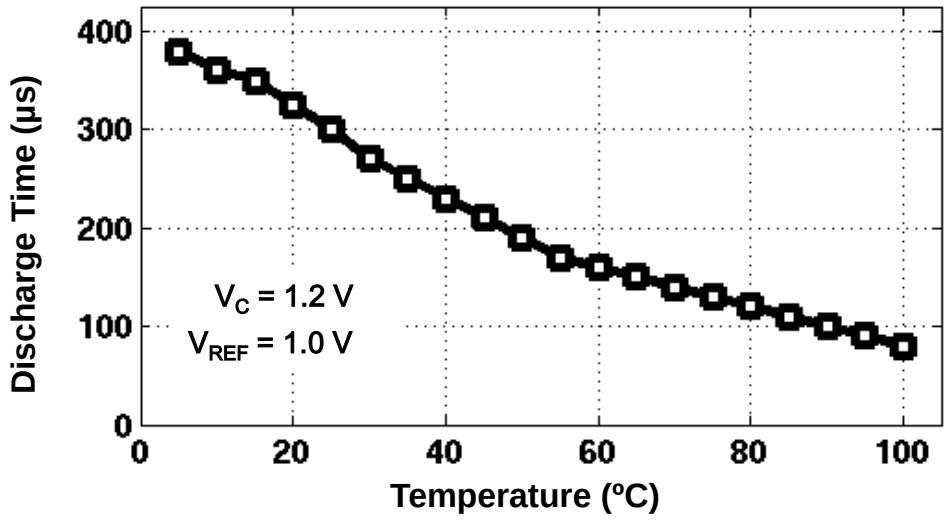

Figure 4.13: Measured discharge time as a function of temperature.

The measured discharge time, T_D for the implemented sensor of Fig. 4.3 in the 5-100ºC range is shown in Fig. 4.13. In this experiment, V_C = 1.2V, and V_{REF} = 1.0 V. Based on this measurement, the slowest response time (limited by T_D at the lowest temperature) is ~0.4 ms. This denotes that the maximum readout speed for this sensor is

approximately 2.5k sample/s. Clearly this can be much higher than the speed requirements for most applications. However, it is straightforward to reduce this by lowering the frequency of Φ_1 and Φ_2 or averaging the measurements through decimation.

In Fig. 4.14, the measurement inaccuracy of three independent temperature sensor chips is presented. In this experiment, packaged silicon chips were immersed in a thermal oil-bath and T_D was measured by a digital counter counting the pulses in OUT after $V_D(t)$ passes V_{REF}. In this setup a two-point calibration was used at 5 ºC and 100 ºC to estimate both V_{OS} and the effective surface area. Also, the nonlinearity of the relationship was corrected through curvature correction based on Equation (4.2). The overall measurement inaccuracies based on this data set is ±1.95 ºC (3σ).

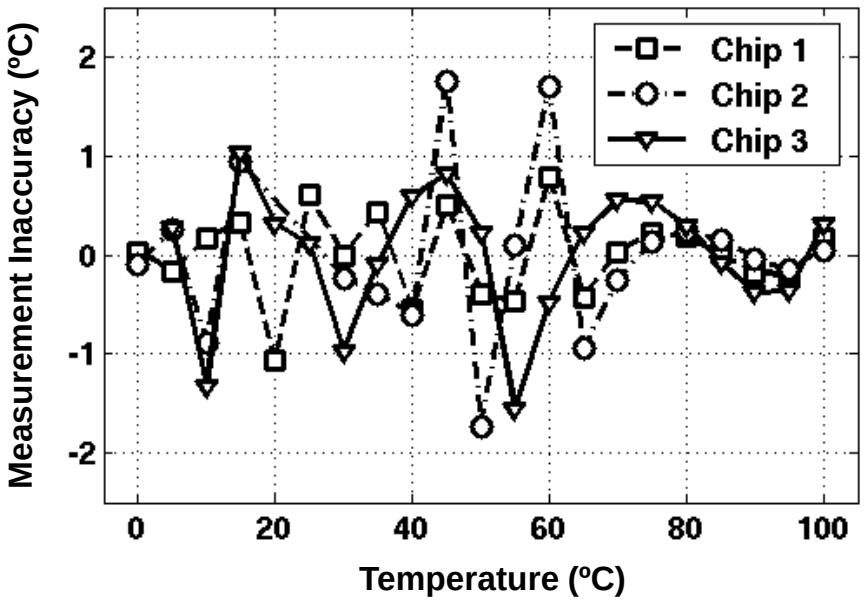

Figure 4.14: Measurement inaccuracy vs. temperature.

The average 3σ inaccuracies for these three chips show ±1.95 ºC where the 3σ lines in Fig. 4.15 shows a peak ±2.6 ºC at 60 ºC. The calibration was carried out off-chip; however it is envisioned that for mass production, the calibration coefficients will be calculated and stored on-chip.

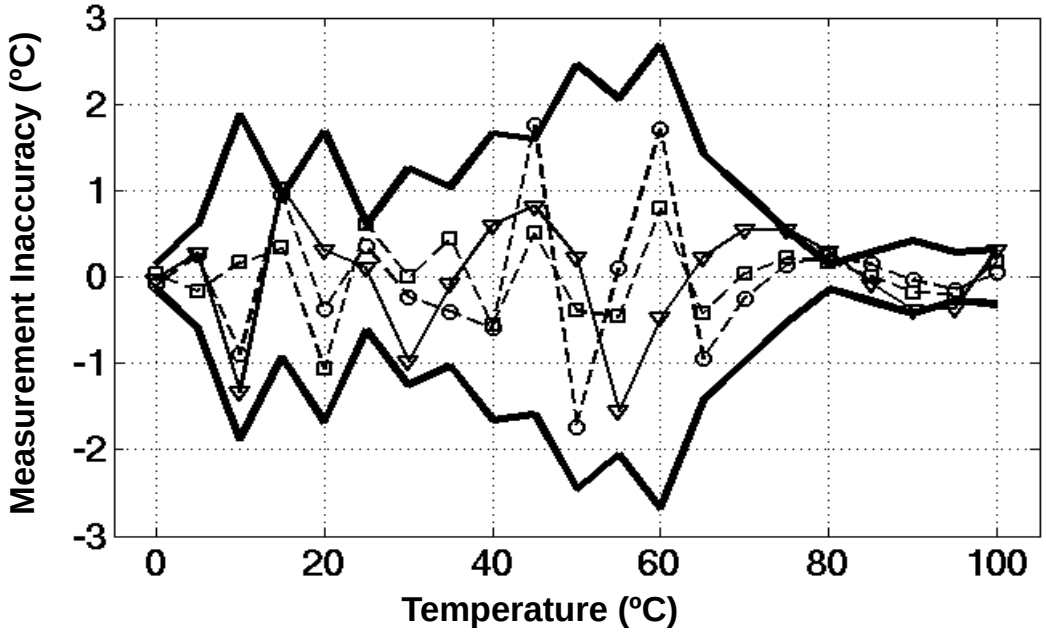

Figure 4.15: Measurement inaccuracy vs. temperature for 3 different chips, bold lines indicate ±3σ values.

4.8 PERFORMANCE COMPARISON

A performance comparison between the sensor reported here and recent on-chip temperature sensors is shown in Table 4.1. As is evident, the sensor presented here is significantly smaller in size than other reported sensors with a digital output while achieving one of the highest conversion rate or readout speed.

Sensor	CMOS Node (nm)	Resolution (°C)	Error (°C)	Range (°C)	Area (mm²)	Power (µW)	Speed (Hz)
[52]	700	0.02	0.2	-70 ~ 225	4600	2500	0.16
[37]	700	0.02	±0.25(3σ)	-70 ~ 130	4.5	100*	10
[62]	350	0.29	±1.3	5 ~ 80	0.049	310#	-
[47]	350	0.0918	-0.25 ~ 0.35	0 ~ 90	0.6	36.7†	2
[63]	180	0.3	-0.8 ~ 1.0	0 ~ 100	0.0324	0.405	1k
[10]	180	0.14 – 0.21	1/-0.8	-10 ~ 30	0.0416	0.119	333
[45]	130	0.66	-1.8 ~ 2.3	0 ~ 100	0.16	1200	5k
[44]	65	0.139	-5.1 ~ 3.5	0 ~ 60	0.01	150	10k
[64]	90	-	-1.0 ~ 0.8	50 ~ 125	$5x10^{-5}$	25†	-
[54]	32	0.45(3σ)	<5	-10 ~ 110	0.02	1600	1k
This Work	**32**	**-**	**±1.95**	**0 ~ 100**	**0.001**	**100**	**2.5k**

without calibration circuits *Average measurement †Sensor with analog output (no ADC)

Table 4.1: Performance Comparison.

4.9 SUMMARY

The sensor architecture presented in this chapter is very simple, and it can be implemented in any technology, SOI or bulk. The measurement results support the feasibility of this architecture while providing consistency with the theoretical formulations. The architecture provides digital output representing the temperature of the chip. The tiny size, very low power consumption, and digital output makes it possible to integrate this architecture in today's multi-core microprocessor to measure on-chip temperature.

Chapter 5: Delta-Sigma (Δ-Σ) Modulation Techniques

5.1 INTRODUCTION

Oversampled delta-sigma (Δ-Σ) modulators are the "gold-standard" for high-resolution data converters. They are common is high-performance mixed-signal applications such as high-fidelity digital audio, instrumentation and measurement, integrated transducer and sensor [65]. The scope of this research is not to design a complete data converter, rather to design, and develop a first-order Δ-Σ modulator using a temperature sensing *p-n* diode to ultimately measure, and monitor the on-chip temperature of a multi-core microprocessor. As such detailed discussion of the data converters and their design are outside the scope of this research.

In this chapter, very briefly, the principles of oversampled Δ-Σ modulation are introduced. The basic modeling and performance of simple first-order Δ-Σ modulators will be discussed.

5.2 BASIC ARCHITECTRUE OF A FIRST-ORDER DISCRETE-TIME Δ-Σ MODULATOR

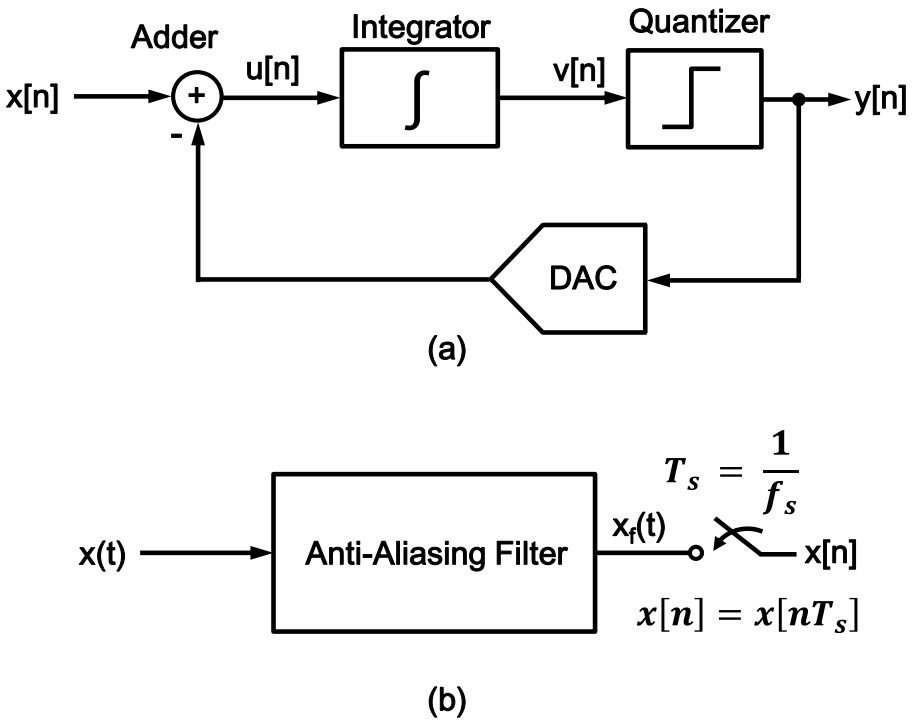

Figure 5.1: Basic architecture of a first-order discrete-time Δ-Σ modulator (a), and front-end anti-aliasing filter and sampler (b).

A general first-order discrete-time Δ-Σ modulator and its front-end anti-aliasing filter with the sampler are shown in Fig. 5.1(a), and (b) respectively [66]-[71]. Here, x[n] represents the samples of the continuous time input x(t), where x(t) is sampled at every sampling clock period T_S. As shown in Fig. 5.1(a), the simplest Δ-Σ modulator is a first-order loop consisting of an integrator, a 1-bit ADC (quantizer), and a 1-bit DAC. The modulator converts the analog input into a quantized digital output, y[n]. The digital

output of the modulator contains a delayed but unchanged replica of the analog input, and a differential version (noise shaped) of the quantization error [70]-[71].

5.3 SIGNAL AND NOISE TRANSFER FUNCTIONS OF THE FIRST-ORDER Δ-Σ MODULATOR

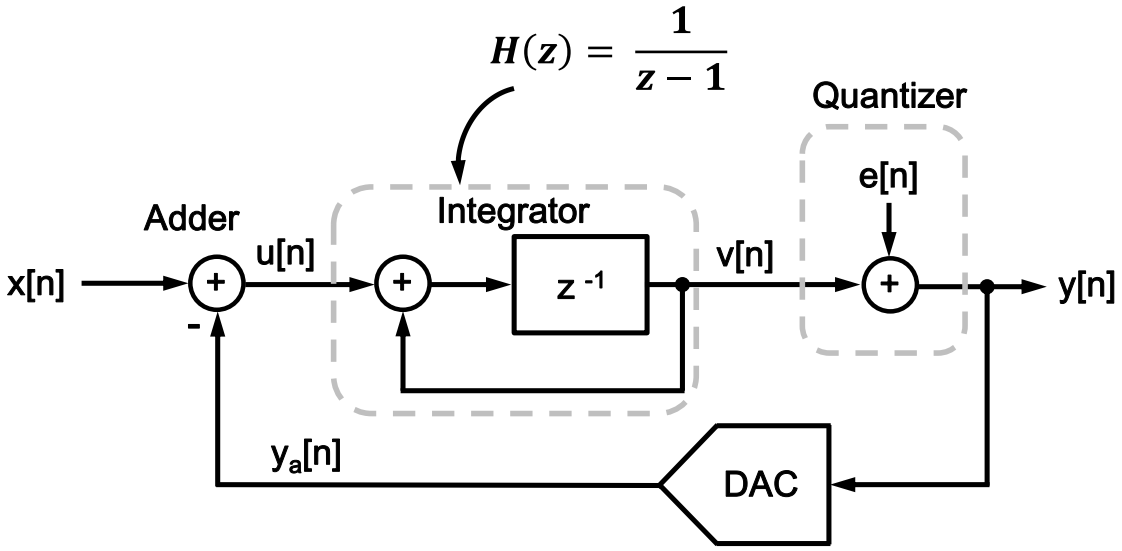

Figure 5.2: Linear model of a first-order discrete-time Δ-Σ modulator.

A linear model of the first order Δ-Σ modulator of Fig. 5.1(a) is shown in Fig. 5.2. In this linear model, assuming the DAC is ideal, it is replaced by a unity gain transfer function. Also the quantizer is replaced with a linear model showing its quantization noise, e[n]. As a result $y_a[n]$ is the exact analog representation of the quantizer digital output, y[n]. Using Fig. 5.2, the output of the modulator can be expressed in z-domain as

$$y(z) = [x(z) - y(z)]\frac{1}{z-1} + e(z), \tag{5.1}$$

This can be rearranged as

$$y(z) = x(z)z^{-1} + e(z)(1 - z^{-1}). \tag{5.2}$$

The signal transfer function (STF) can be deduced from Equation (5.2) assuming quantization noise is zero. Thus, the signal transfer function becomes

$$\text{STF} = \frac{y(z)}{x(z)} = z^{-1}. \tag{5.3}$$

This means that, in a discrete-time modulator, the input appears at the output after a unit delay, and the modulator acts as an all pass filter for the input.

The noise transfer function (NTF) can be deduced from Equation (5.2) assuming there is no signal. Thus, the noise transfer function becomes

$$\text{NTF} = \frac{y(z)}{e(z)} = 1 - z^{-1}. \tag{5.4}$$

As seen in Equation (5.4), the NTF has a zero located at DC frequency. That means, the NTF of the first order Δ-Σ modulator provides zero gain or infinite attenuation, at DC frequency, to the noise injected at the input of the quantizer. The noise gets relatively amplified at higher frequencies. This is called noise shaping in a Δ-Σ modulator [70]-[71]. In order to recover the input, the digital output of the modulator is filtered with a low-pass digital filter.

5.4 CONTINUOUS-TIME Δ-Σ MODULATOR

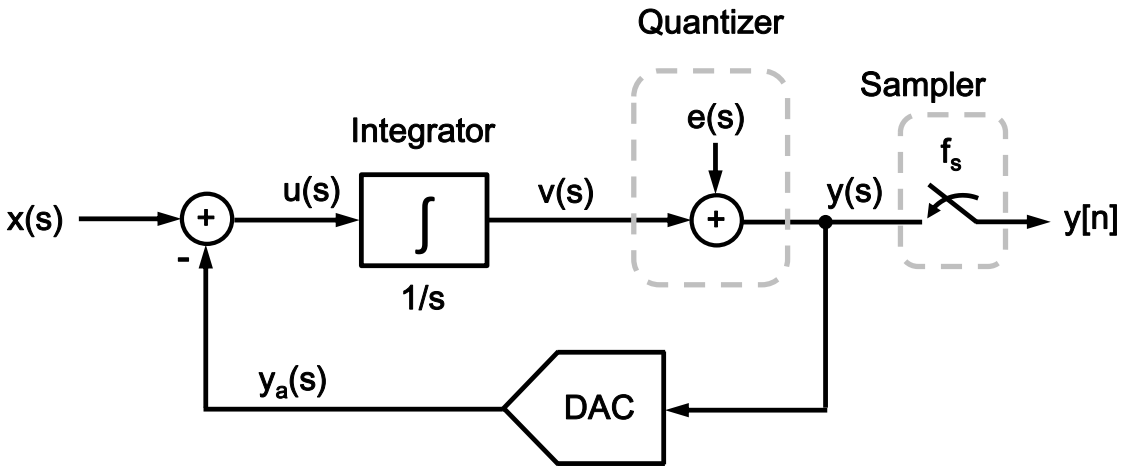

Figure 5.3: Linear model of a first order continuous-time Δ-Σ modulator.

It is possible to implement the Δ-Σ modulator in continuous-time [61],[70]-[71]. The linear model of a first-order continuous-time Δ-Σ modulator is shown in Fig. 5.3 [61]. Here the modulator is modeled in s-domain with an ideal integrator represented with the transfer function, 1/*s*. The 1-bit ADC (quantizer) is modeled as an error source, e(s), and the DAC is considered to be ideal with unity gain such that $y_a(s)$ equals y(s). In this model, it is assumed that f_S is normalized to 1. Therefore, y(s) can be expressed as

$$y(s) = [x(s) - y(s)]\frac{1}{s} + e(s). \tag{5.5}$$

Solving for y(s) yields,

$$y(s) = \underbrace{\frac{1}{s+1}}_{\text{STF}} x(s) + \underbrace{\frac{s}{s+1}}_{\text{NTF}} e(s). \tag{5.6}$$

The signal transfer function (STF) from x(s) to y(s) is a low-pass filter, and the noise transfer function (NTF) from e(s) to y(s) is a high-pass filter with a zero at DC frequency. From the STF it is clear that, as long as the input signal frequency falls within the pass-band of the STF, then it will remain the same at the output.

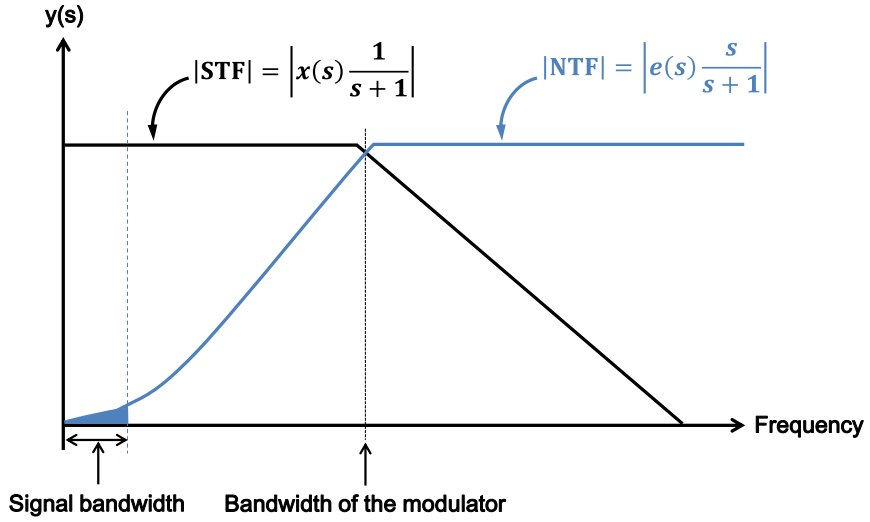

Figure 5.4: Frequency response of a first-order continuous-time Δ-Σ modulator.

As shown in Fig. 5.4, in the frequency range of signal bandwidth the noise has a small value due to noise shaping. The blue shaded area illustrates total noise in the signal band of frequencies. In the signal band of frequencies the modulator has high gain. At

high frequencies, beyond the signal bandwidth, the noise continues to increase. The modulator has essentially pushed the noise out of the bandwidth of the input signal. The out of band noise can be filtered by using a digital filter. From the behavior of STF and NTF the discrete-time and continuous-time modulators are equivalent to one another, and both can be analyzed with the same NTF as the one for discrete-time [71].

5.5 ADVANTAGES OF CONTINUOUS-TIME Δ-Σ MODULATOR OVER DISCRETE-TIME

Most Δ-Σ modulators found today in various applications employ switched capacitor, discrete time integrators, within the modulator to implement noise shaping. The advantage of discrete time Δ-Σ modulators is that the switched capacitor based architectures exhibit good accuracy and linearity [71]-[72]. However, they have a number of disadvantages.

In Switched capacitor modulators as the input signal bandwidth increases the sampling frequency needs to go higher to avoid aliasing, and also to maintain a high oversampling ratio. This requires higher bandwidth integrators to guarantee reliable settling without much error [71]-[72]. That means, the power consumption of the integrators will go up. As a result the discrete time Δ-Σ modulators tend to be power hungry.

Continuous-time Δ-Σ modulators eliminate the settling time issue all together allowing low power continuous time Δ-Σ modulator design. There is no acquisition phase in continuous-time Δ-Σ modulator as the input is continuously sampled, so a high

performance sample and hold stage is eliminated. As a result, power consumption in this type of modulator is comparatively lower [71]-[72]. However, in order to guarantee good linearity their power consumption can go up if the frequency of input signal is increasing.

Another advantage of continuous-time modulators is that they provide inherent anti-aliasing [71]-[72]. From the STF of Equation (5.6), it is seen that STF has a low-pass characteristic which eliminates frequency components from the input signal beyond the bandwidth of STF providing first-order anti-aliasing.

Because of the advantages of continuous-time modulators over discrete-time ones, the architecture of the first-order continuous-time modulator has been chosen to implement the temperature sensor for this research. However, regardless of discrete or continuous type, a lower order modulator may produce unwanted tones at the output if its input is DC or static [71]-[72].

5.6 SUMMARY

Because of the advantages of oversampling and noise shaping the Δ-Σ modulator based temperature sensor architecture is expected to provide better suppression of noise in the signal band of interest, thus providing a better signal to noise ratio. As mentioned, the Δ-Σ modulator can be implemented in discrete-time or in continuous-time. Because of the advantages of smaller size, lower power consumption, and inherent anti-aliasing filtering, the continuous time architecture is more attractive to implement the Δ-Σ modulator for this research. As such, the architecture of a first-order continuous-time Δ-Σ modulator has been chosen to implement the temperature sensor for this research.

Chapter 6: Temperature Sensor with a Self-Discharging Diode within a Delta-Sigma Loop

6.1 INTRODUCTION

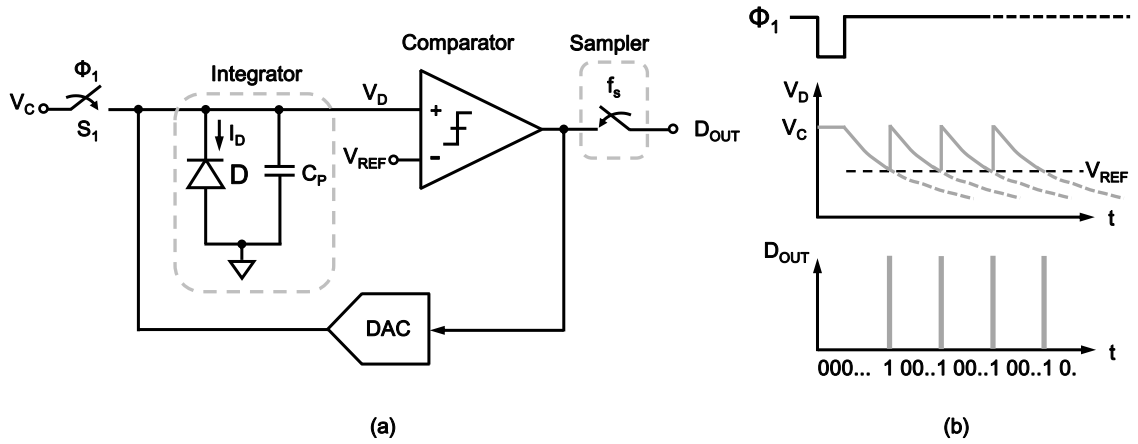

Figure 6.1: Basic concept of the sensor in a delta-sigma loop (a), and timing diagram (b).

The sensor presented in Chapter 4 was implemented in an open loop fashion. This chapter discusses the design and CMOS implementation of a modified version of the self-discharging temperature sensor topology. This new architecture incorporates a delta-sigma loop while providing a direct digital output.

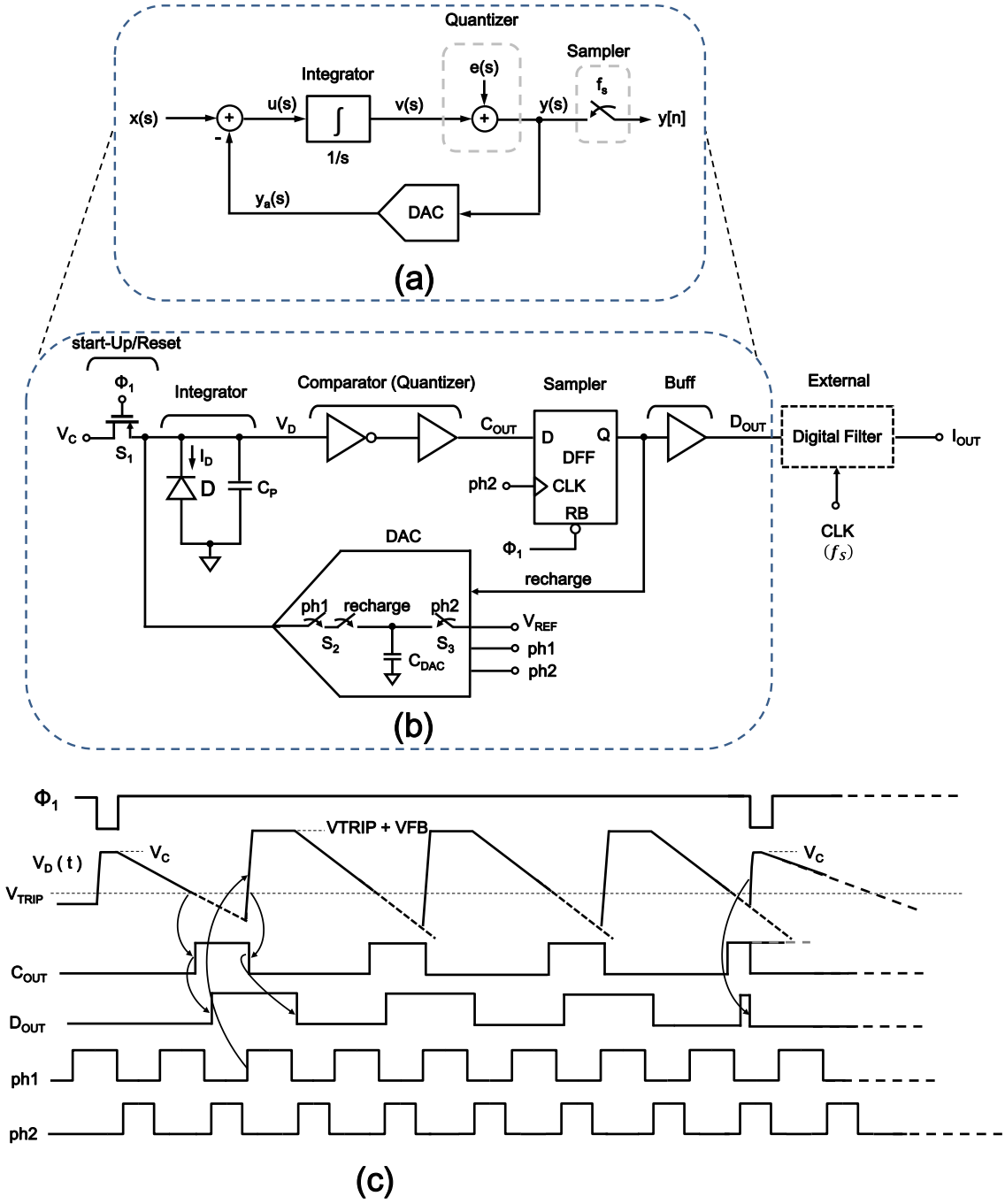

Figure 6.2: Basic block diagram of a first-order continuous-time Δ-Σ modulator (a), basic architecture of the proposed Δ-Σ modulator (b), and its timing diagram (c).

6.2 ARCHITECTURE

The basic concept of the temperature sensor implemented in a Δ-Σ loop is shown in Fig. 6.1(a). Here, the switch S_1 is controlled by Φ_1. At first, switch S_1 closes ($\Phi_1 = 0$) to bias the diode with the voltage V_C to start the temperature measurement. When S_1 opens, the capacitor C_P starts discharging through I_D. The output of the comparator remains low as long as V_D is higher than V_{REF}, and it goes high when V_D discharges to V_{REF}. The output of the comparator is sampled at the input clock rate, f_S. The sampled output, D_{OUT}, is shown in Fig. 6.1(b).

A detailed version of this architecture, along with the basic timing diagram is shown in Fig. 6.2. In the modulator of Fig. 6.2(b), the continuous-time integrator is implemented with the diode D, and its junction capacitance C_P. The start-up (reset) switch S_1 is used to initiate the operation of the modulator, and also to periodically reset the modulator after each measurement. When on, switch S_1 reverse biases the diode with the externally applied fixed voltage V_C.

The timing diagram of the modulator is shown in Fig. 6.2(c). As evident, first switch S_1 opens (Φ_1 goes high) and the diode is allowed to self-discharge through I_D. As discussed before, during this time the diode is acting as an integrator of the delta-sigma modulator, and diode voltage V_D discharges from its initial value V_C as shown in Fig. 6.2 (c). The discharge and integration can be expressed as

$$V_D = -\frac{1}{C_P}\int I_D dt. \tag{6.1}$$

When V_D reaches the comparator trip voltage, V_{TRIP}, then C_{OUT} goes high. The flip flop (DFF) samples C_{OUT} at the rising edge of the clock ph2, and produces the 1-bit digital output, 'recharge' and its buffered version is D_{OUT}, the digital output of the sensor. Every time 'recharge' goes high, the feedback DAC inserts a fixed amount of charge into C_P to push V_D to a voltage greater than V_{TRIP}. The DAC has been implemented with a switched capacitor circuit operating on the two non-overlap clock phases, ph1 and ph2 generated on-chip from the input sampling clock, CLK.

During ph2 its capacitor is charged with an externally applied fixed reference voltage, V_{REF}, and in the next phase, ph1, it resets the diode through charge sharing with C_P if the diode is already discharged to V_{TRIP} which is determined by the logic high state of 'recharge'. As mentioned, switch S_1 can be used to reset the modulator at any time. The reset phase is initiated when Φ_1 transitions from high to low (switch S_1 is turned on). During reset, the outputs of the comparator and the DFF go to low. Depending on the temperature, the rate of discharge of C_P through the diode reverse current I_D will be different which will produce a temperature dependent pulse density modulated output, D_{OUT}, from the modulator. During the active phase of the modulator, the pulse density modulated forms of V_D, C_{OUT}, and D_{OUT} are available which are shown in Fig. 6.3. The temperature dependent current I_D can be calculated from D_{OUT}, and ultimately temperature can be measured from I_D.

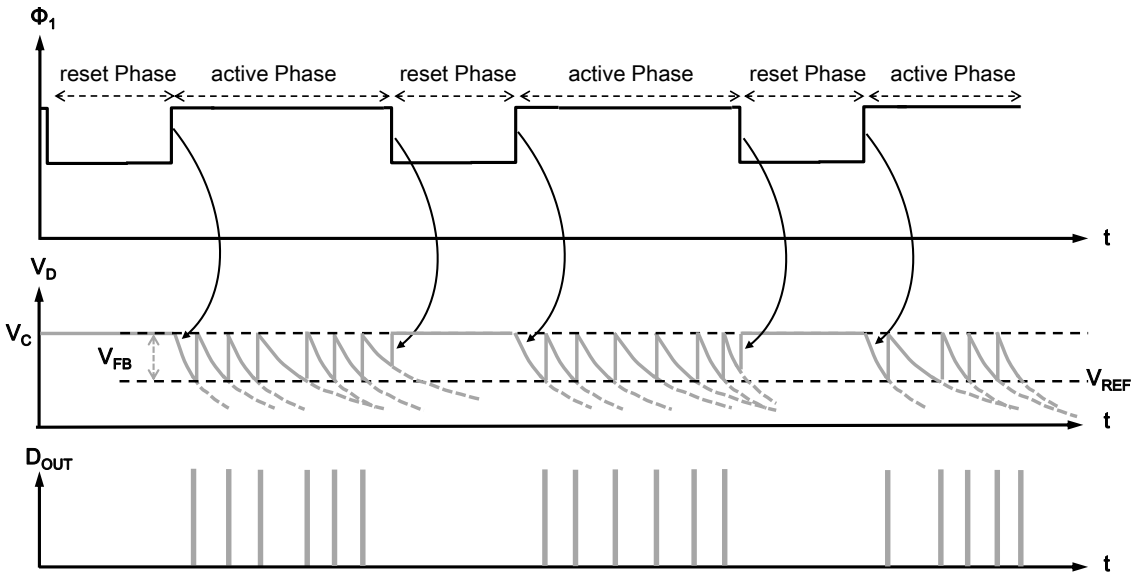

Figure 6.3: Timing diagram showing pulse density modulated output.

6.3 CIRCUIT DESIGN OF THE Δ-Σ MODULATOR

The complete schematic of the proposed Δ-Σ based temperature sensor is shown in Fig. 6.4(b), the corresponding block diagram is shown in Fig. 6.4(a). The System in Fig 6.4 is implemented in TSMC's 180nm bulk CMOS technology. The modulator takes DC voltages V_C, and V_{REF}, and clocks Φ_1, and CLK as inputs, and produces a 1-bit digital output D_{OUT}, which is processed externally by using a digital low-pass filter to estimate I_D. The complete schematic of Fig. 6.4(b) is broken up into different functional sub-circuits, and they are discussed in the following sub-sections.

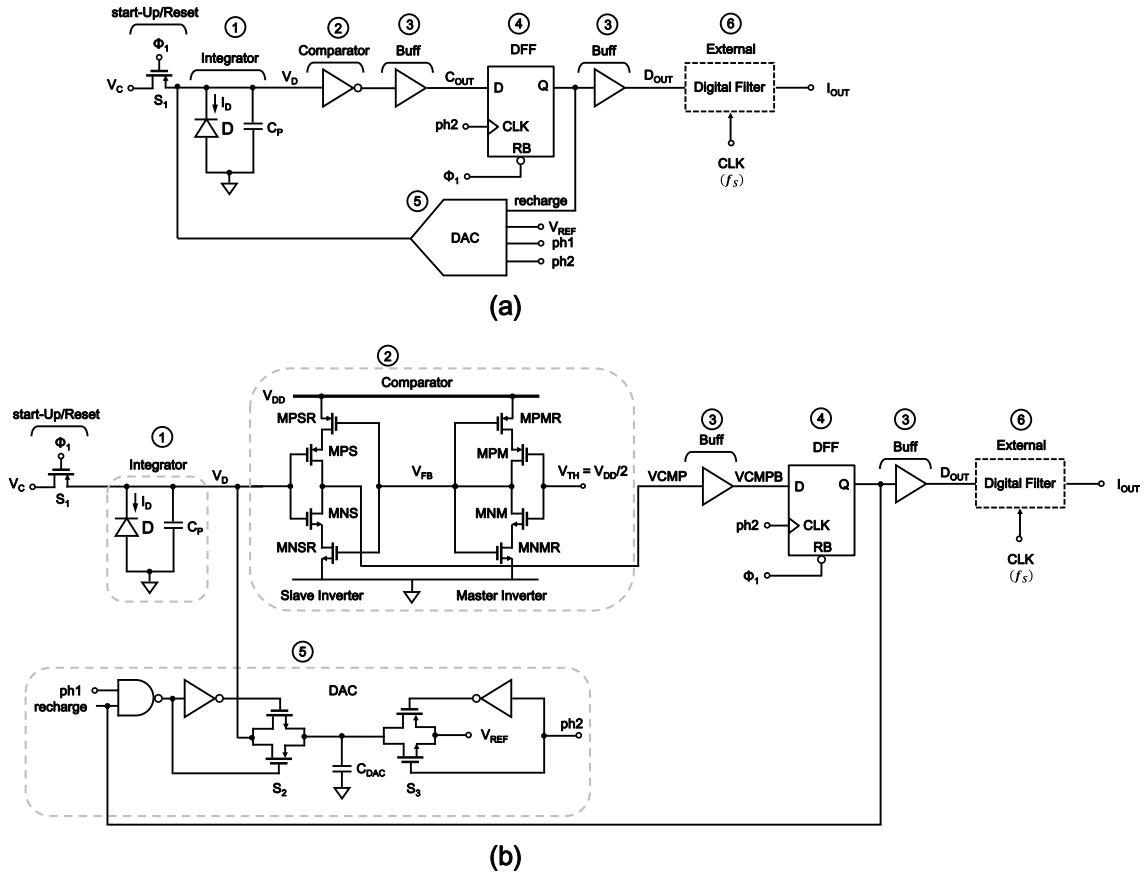

Figure 6.4: The block diagram (a), and complete schematic of the first-order Δ-Σ modulator, (b).

6.3.1 The Start-up/Reset Circuit

The start-up/reset circuit basically starts the operation of the Δ-Σ modulator, and it also resets the modulator. It consists of the switch S_1 controlled by the clock input Φ_1. The start-up/reset clock, Φ_1, is received by the modulator from the thermal management unit of the microprocessor. As shown in Fig. 6.3, every time Φ_1 transitions from high to low, the modulator enters into its reset phase. This causes the outputs of the comparator,

and DFF to go low immediately. When Φ_1 goes high, the modulator enters into its active phase.

6.3.2 The Temperature Sensing *p-n* Diode

In today's bulk CMOS technology, there is more than one way to fabricate a *p-n* diode. Fig. 6.5 shows three common, and widely used methods to implement a *p-n* diode in such process.

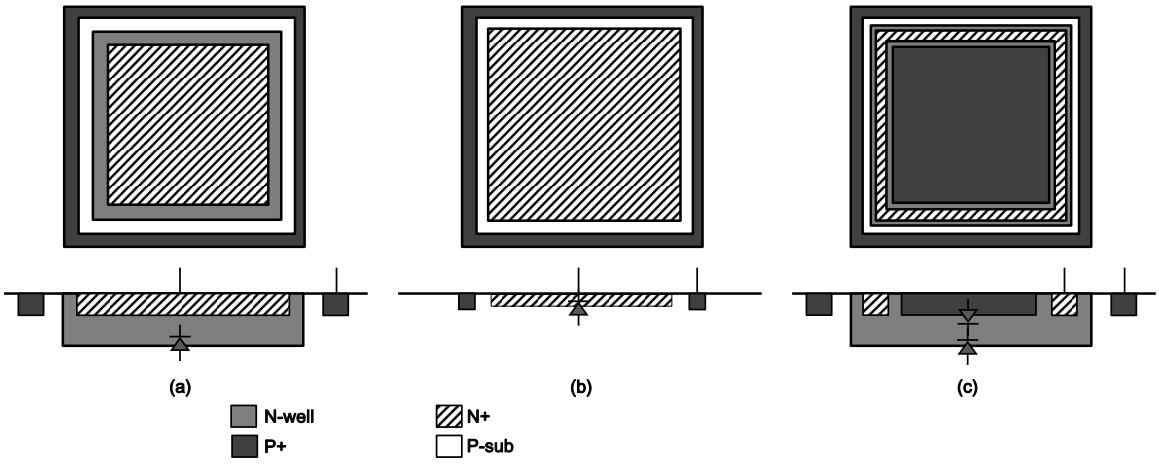

Figure 6.5: Top and cross-sectional views of different *p-n* diode architectures, Nwell/Psub (a), N+/Psub (b), and P+/Nwell (c).

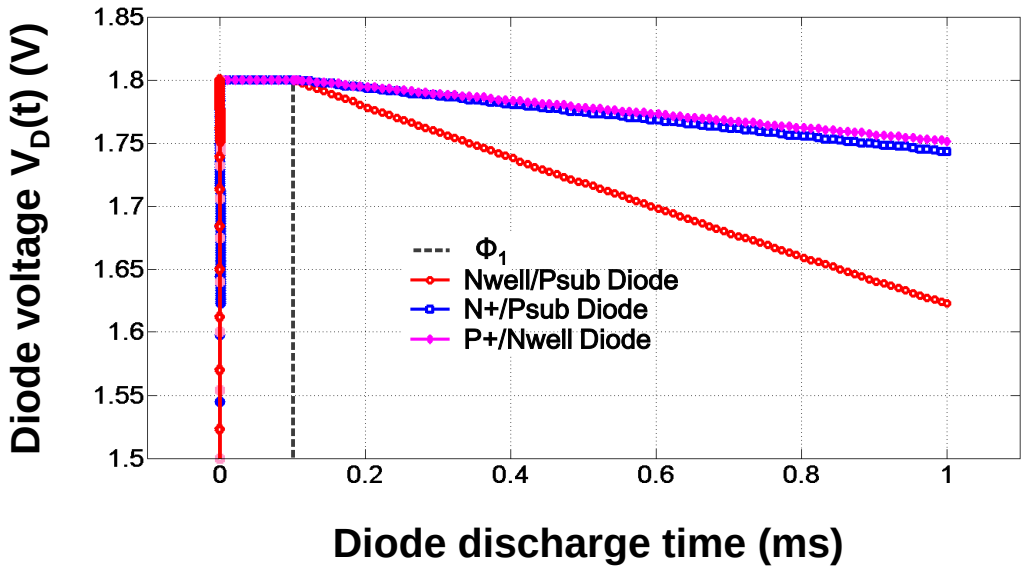

Figure 6.6: Simulation showing the discharges of the three available diodes.

This design uses a 10µm by 10µm size Nwell/Psub diode to implement the Δ-Σ loop. The Nwell/Psub diode has the smallest junction capacitor among the three possible diodes shown in Fig. 6.5. The simulated discharges of the three different diodes of same area (10µm by 10µm) at a fixed temperature are shown in Figs. 6.6. From the simulation results, it is obvious that the response time of the Nwell/Psub diode would be faster in temperature sensing applications. In the simulation shown in Fig. 6.6, first the diodes were reverse-biased with a DC voltage of 1.8V when the switch S_1 of Fig. 6.4 was turned on by applying the switch control logic signal Φ_1 as shown with the dark dotted line. When Φ_1 goes low (S_1 is turned off) then diode junction capacitance starts discharging through I_D. In order to remove any non-idealities from CMOS switch, an ideal switch has been used for S_1 in this simulation. The ideal switch (S_1) is turned on when Φ_1 is logic high, and it is turned off when Φ_1 goes low.

6.3.3 The Integrator

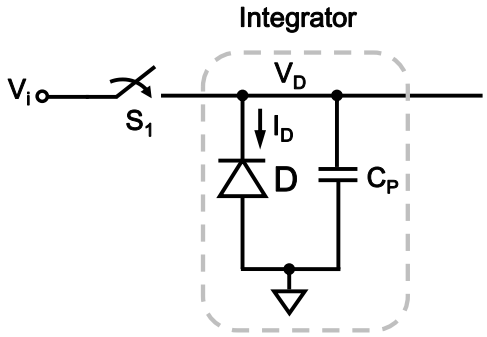

Figure 6.7: The continuous-time integrator of the Δ-Σ modulator.

As mentioned earlier, the continuous-time integrator of the modulator is implemented with a 10µm by 10µm Nwell/Psub *p-n* diode operating in the reverse-bias mode along with its own junction capacitor C_P, as shown in Fig. 6.7. In this implementation, the capacitor C_P is allowed to self-discharge through I_D, of the diode, D.

6.3.4 The Comparator

For the continuous-time Δ-Σ modulator the comparator was chosen to be continuous as well. In the implementation of the sensor presented in Chapter 4, a clocked comparator was used. As mentioned in 4.3.1.3 due to the clocked comparator, an isolation buffer was needed to eliminate transient kick-back noise from the comparator into the diode discharge node, V_D. The isolation buffer needs extra silicon area, and it also consumes power. In this implementation of the sensor in a Δ-Σ modulator, to save both area, and power consumption, continuous-time comparator is designed which eliminates the need for any isolation buffer. The architecture of the comparator is chosen based on the idea presented in [73]. The offset of the comparator is made independent of

process and temperature variations with a built-in continuous-time self-tuning mechanism which requires no dynamic circuit for offset cancellation. The proposed architecture is shown in Fig. 6.8.

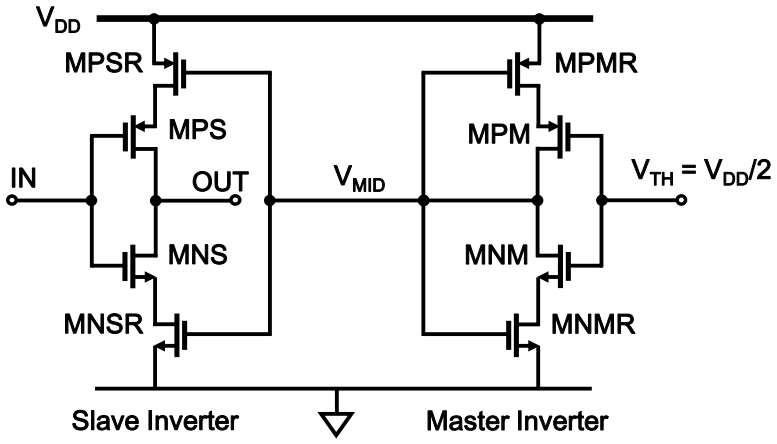

Figure 6.8: Proposed switching voltage (offset) compensated comparator.

The PMOS and NMOS transistors of the inverter comparator of Fig. 6.8 are sized appropriately such that the trip voltage*e* of the comparator at the typical process, and room temperature is at $V_{DD}/2$. The comparator is composed of two inverters, named as master and slave inverters. The input of the master inverter is set externally at its desired switching point of $V_{DD}/2$. The transistors at the two outer rails of the master and slave inverters, MPMR, MNMR, MPSR, and MNSR, are biased to operate in the linear region. The on resistances of these two transistors are controlled by a negative feedback V_{MID} which is also the output of the master inverter. With its input voltage fixed at $V_{DD}/2$, the master inverter will generate the required output voltage V_{MID} to tune the resistance of the two transistors at the supply rails. Through this negative feedback mechanism, the switching threshold voltages of the master, and slave inverters will be maintained at $V_{DD}/2$, independent of process and temperature variations. The transistors of the slave

inverters are designed with the same physical sizes of the master inverter transistors so that the switching threshold voltage of the slave inverter follows that of the master inverter. The widths of all the PMOS transistors were made 1.2µm, and those of the NMOS transistors were 0.4µm. The lengths of the transistors MPSR, MPMR, MNSR, and MNMR were made 2µm, and those of MPS, MPM, MNS, and MNM were 180nm.

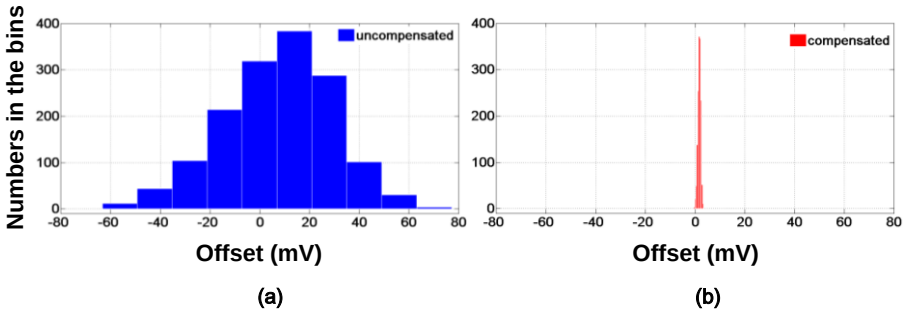

Figure 6.9: Monte-Carlo simulations showing offset voltages of uncompensated comparator (a), and compensated comparator (b).

Type	Mean (mV)	Std. Dev. (mV)	Min (mV)	Max (mV)
Uncompensated	**7.5**	**22**	**-63**	**77**
Compensated	**1.7**	**0.604**	**-0.55**	**3.4**

Table 6.1: Summary of Monte-Carlo simulation results for the offset of the inverter comparator.

Monte-Carlo simulations were run to find out the spreads of comparator offset voltage due to mismatch between the transistors, and process variations. Fig. 6.9 shows Monte-Carlo simulation results for both compensated and uncompensated comparators.

In case of the uncompensated comparator, the master inverter was disconnected from the slave inverter. It is clearly evident that the compensated comparator drastically reduces the offset. The summary of Monte-Carlo simulations is shown in Table 6.1. This table shows mean, standard deviation, minimum, and maximum values of the offset voltages for the compensated and uncompensated comparators.

However, this self-tuning method requires that the master inverter output is biased at $V_{DD}/2$. From simulations, the worst current consumption of the comparator is found to be about 2.4µA which occurs at 100°C for the fast-fast corner at 1.8V supply.

6.3.5 The D-Flip-Flop as the Sampler

As shown in Fig. 6.4(b), to sample the output of the comparator, a D-type flip-flop (DFF) with an active low reset is used. The DFF uses a clock ph2 to latch the output of the comparator. The output of DFF (recharge) is used by the feedback DAC, and a buffered version of the output, D_{OUT}, is sent as the final digital reading of the sensor. During periodic temperature measurement, when clock signal Φ_1 of S_1 goes low, the DFF is reset. The DFF in this implementation was not designed. The schematic and layout of the DFF used in this design have been taken from the standard cell library of the TSMC's 180nm Process Design Kit (PDK).

6.3.6 The Reference Feedback DAC

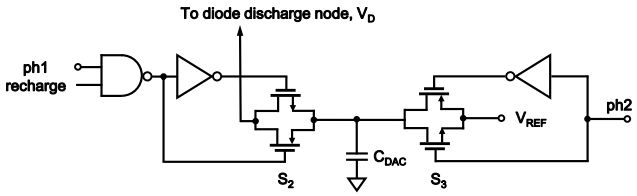

Figure 6.10: The reference DAC of the Δ-Σ modulator.

A switched capacitor based DAC is used in the feedback loop of the Δ-Σ modulator. The DAC provides a capacitive feedback at the input of the integrator. The detail of the DAC schematic is shown in Fig. 6.10. The DAC receives two non-overlap clocks, ph1 and ph2, a reference voltage V_{REF}, and the output of the DFF, recharge, at its input to generate the feedback for the modulator. During ph2 the DAC capacitance C_{DAC} is charged with the reference voltage V_{REF} through the switch S_3. During the next clock phase ph1, switch S_2 connects C_{DAC} to the diode discharge node only if the DFF output (recharge) is high. During this time, through charge sharing, C_{DAC} charges up C_P. The values of the C_{DAC}, and reference voltage are chosen such that the DAC charges C_P to a voltage higher than the threshold voltage of the comparator by adding a voltage V_{FB} to C_P which can be expressed as

$$V_{FB} = V_{REF} \cdot \left(\frac{C_{DAC}}{C_{DAC}+C_P}\right). \tag{6.2}$$

In this implementation, the capacitance C_P consists of the diode junction capacitance, the input capacitance of the comparator, and also parasitic capacitance of the metal routings in the layout, and it was estimated to be about 30fF. C_{DAC} was

implemented with a metal4-metal5 cap of 10μm by 10μm size, and its capacitance value was about 100fF. The modulator was tested with a reference voltage of 1.0V. Thus, according to Equation (6.2), V_{FB} is about 75mV. A NAND gate and two inverters are used to appropriately clock the gates of the two switches, S_2 and S_3. The implementation of these gates is very straightforward, and is not presented here. The size of the capacitance C_{DAC} was made equal to that of the diode D of Fig. 6.4, and to save silicon area it was placed on top the diode with a shield to ground metal between the C_{DAC}, and the diode.

6.3.7 Digital Filter

Typically, in a Δ-Σ modulator the digital output of the modulator is processed by a low-pass digital filter to remove the extra quantization noise beyond the signal band of frequency [74]-[77]. In this implementation, the digital filter is implemented outside the chip. However, the output of the digital filter is further processed off-chip to transform its output voltage into a current which corresponds to the temperature dependent reverse leakage current I_D of the diode. The measurement of I_D was carried out for multiple cycles of the reset clock, and average values of I_D and its standard deviation, σI_D, were measured. Thus, from the calculated I_D and σI_D, inaccuracies of temperature measurement of the chip can be determined. The following section gives an outline of how to extract I_D from the modulator output.

6.4 MEASURING TEMPERATURE FROM D_{OUT}

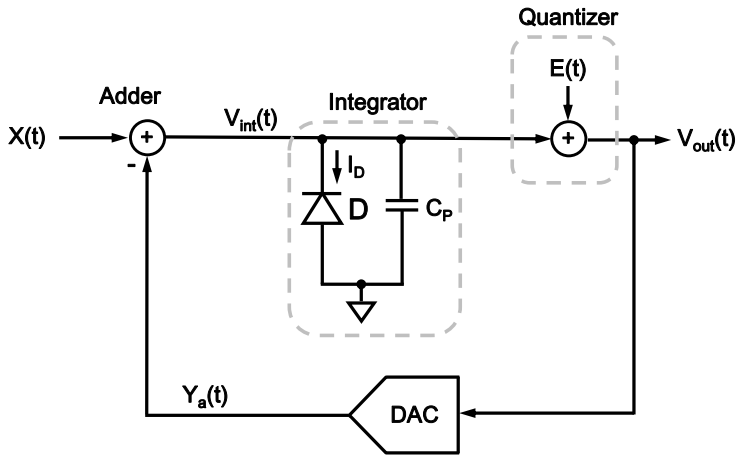

Figure 6.11: The linear model of the proposed modulator in time domain.

In the linear model of the modulator shown in Fig. 6.11, the discharge of C_P can be expressed as

$$V_{int}(t) = \frac{1}{C_P}\int_0^{T_S} I_D dt\,, \tag{6.3}$$

Where, it is understood that the I_D is negative with respect to V_{int}, and $T_S = \frac{1}{f_S}$, is the sampling period. Assuming constant current I_D during the integration,

$$V_{int} = \frac{I_D}{C_P} \cdot \frac{1}{f_S}, \tag{6.4}$$

Assuming, the comparator (quantizer) is linear with unity gain, and also assuming no quantization noise, then V_{out} follows V_{int} such that

$$V_{int} = V_{out} = \frac{I_D}{C_P \cdot f_S}, \quad (6.5)$$

If the output voltage V_{out} is measured, then the diode integrating current can be extracted from the above Equation as

$$I_D = V_{out} \cdot C_P \cdot f_S \cdot 1.8. \quad (6.6)$$

In the above equation, the parameters C_P and f_S are known. So, if the output voltage, V_{out}, can be calculated then I_D can be measured. It has been mentioned previously that, the output voltage of the modulator contains the signal, and noise which is shaped by the modulator. So, a digital low-pass filter can be used to get rid of most of the noise. The output of the filter is an average value of V_{out} which can be used in Equation (6.6) to find out the diode current I_D. If V_{out} is measured periodically while resetting the modulator at the start of each measurement, then using the digital filter, the average value, and the standard deviation (sigma, σ) of I_D can be measured. It is important to note that, V_{out} in Equation (6.6) is based on the 1-bit digital input to the filter which is between the logic levels of 0V and 1V, when captured by a logic analyzer. As a result Equation (6.6) should be multiplied by V_{DD} = 1.8V to get the correct I_D.

6.5 A THERMAL MONITORING SYSTEM USING SELF-DISCHARGING DIODES WITHIN A DELTA-SIGMA LOOP

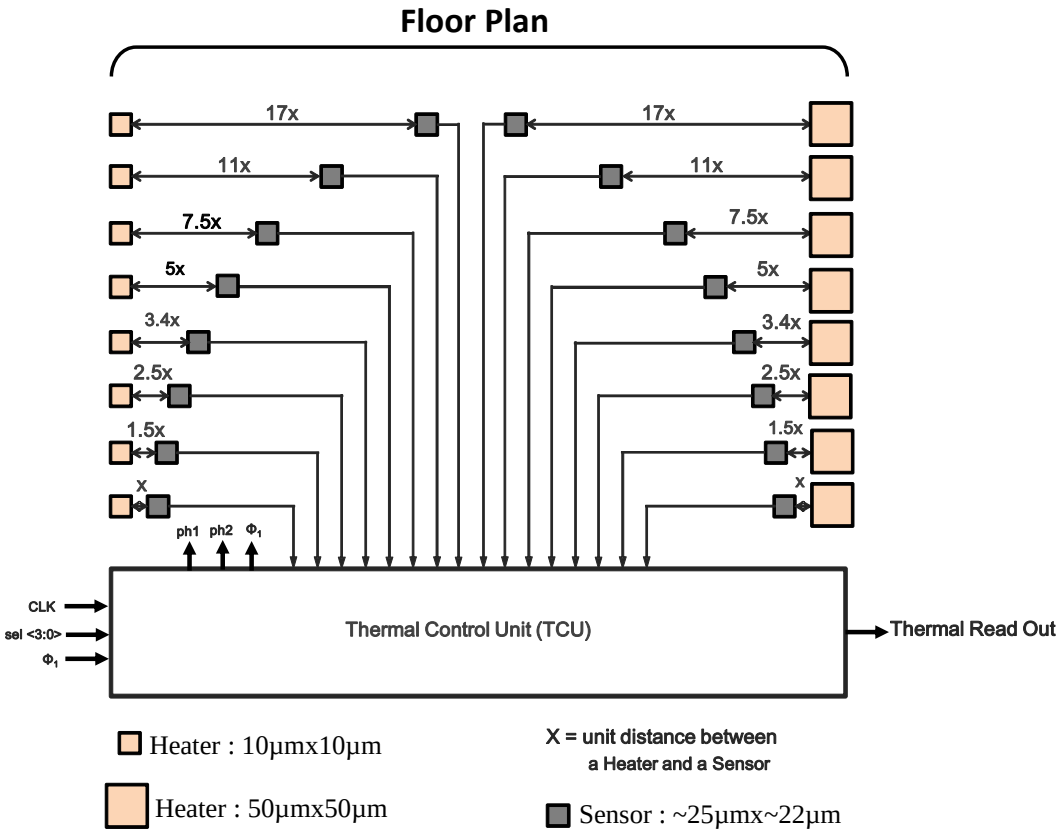

Figure 6.12: Floor plan of the chip showing all 16 sensors, heaters, and thermal control unit.

With the Δ-Σ modulator presented in this chapter, a thermal monitoring system was implemented to measure on-chip temperatures at multiple locations of the chip. The floor plan of the chip, implemented in a TSMC 180nm CMOS process, is shown in Fig. 6.12. The chip occupies an area of about 2.3mm by 2.3mm, and a total of 16 Δ-Σ modulator sensors were placed in the chip. The sensors were placed at different distances from some resistors (heaters) built with p^+ diffusions. The heaters were built as square

units with two different sizes, 10µm by 10µm, and 50µm by 50µm. The 8 Δ-Σ sensors on the upper right half of the chip were placed near the 50µm by 50µm size heaters, the other 8 on the left side were placed near 10µm by 10µm size heaters. During the experiment, when activated, the heaters will diffuse heats non-uniformly because of their non-uniform distances from the sensors. As a result, during the test, the sensors may be under slightly different temperatures from one another.

The thermal control unit (TCU) of Fig. 6.12 provides all the clocks, and other control signals to all the sensors placed on the chip. All the sensors on the chip operate concurrently, however TCU selects the output of one of the sensors at a time. The selected output (Thermal Read Out) is send outside the chip to be processed by a digital low-pass filter to calculate I_D and σI_D.

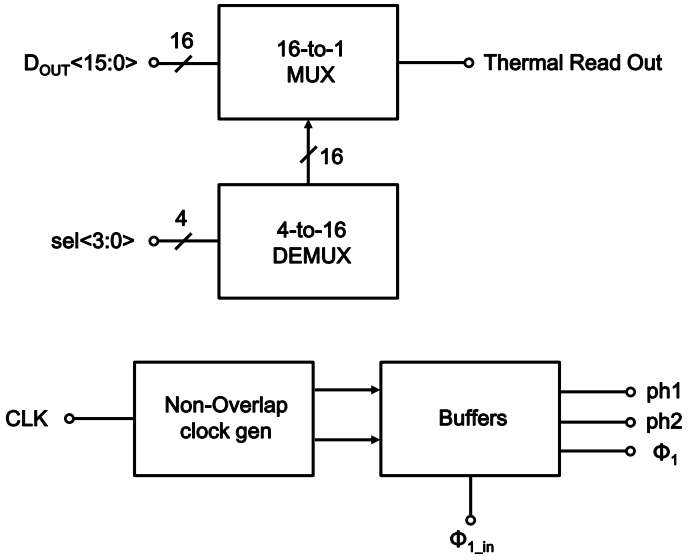

Figure 6.13: Block Diagram of the Thermal Control Unit (TCU).

The block diagram of the TCU is shown in Fig. 6.13. A 4-to-16 de-multiplexer (DEMUX) converts the 4 input select bits into 16 select lines. During temperature measurement, all 16 sensors operate at the same time. However, based on the 16 select lines output of the DEMUX, the output of one of the 16 sensors is selected at the output of the 16-to-1 MUX (multiplexer) in the TCU. Thus, the output, Thermal Read Out, is the 1-bit digital data of the sensor selected by the MUX. The DEMUX and MUX are implemented as shown in Figs. 6.14 and 6.15 respectively.

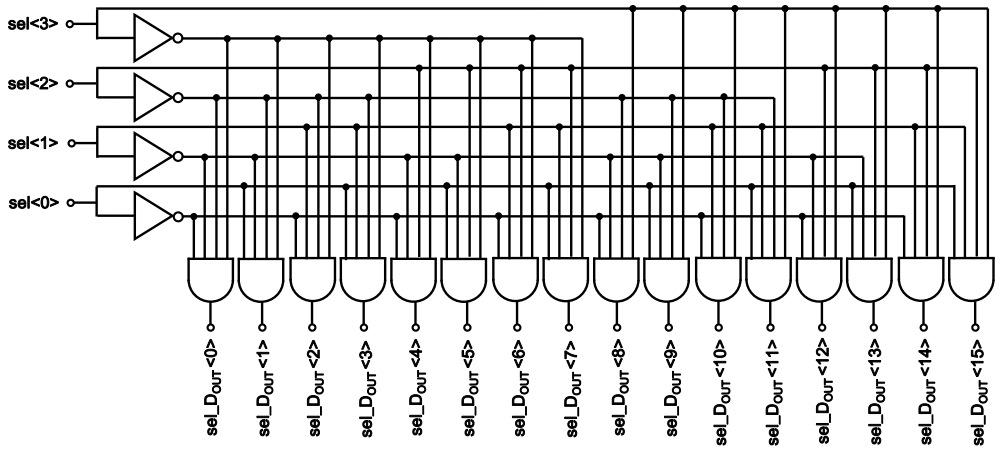

Figure 6.14: 4-to-16 DEMUX of the TCU.

The DEMUX was implemented with custom digital inverters, and 4-input AND gates. In fact, each AND gate was designed with a 4-input NAND gate cascaded with an inverter. The schematics of the inverters and the NAND gates are straightforward, and they are not discussed here.

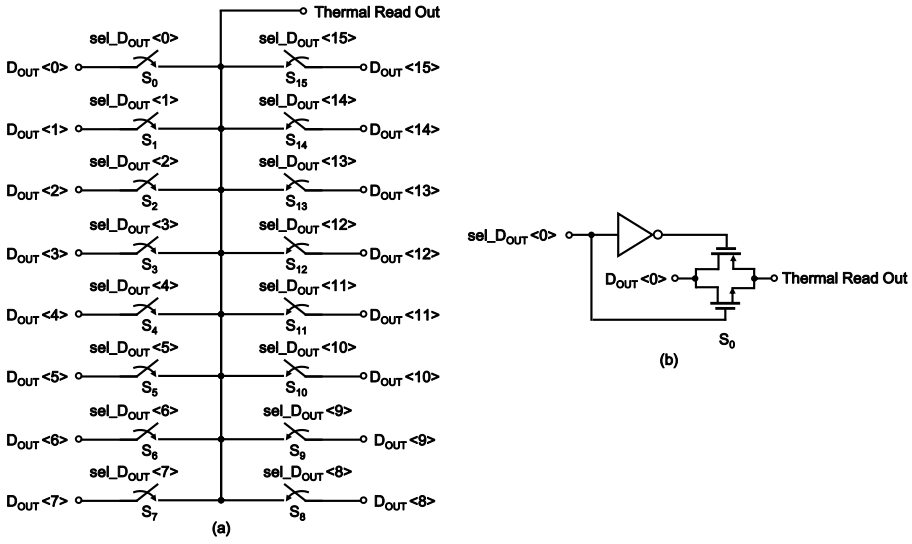

Figure 6.15: 16-to-1 MUX of the TCU (a), and schematic of each switch (b).

The MUX was implemented with CMOS switches controlled by the 16 outputs of the DEMUX. The schematics of all the switches, S_0 through S_{15}, are the same. Fig. 6.15(b) shows the schematic of one of the switch, S_0.

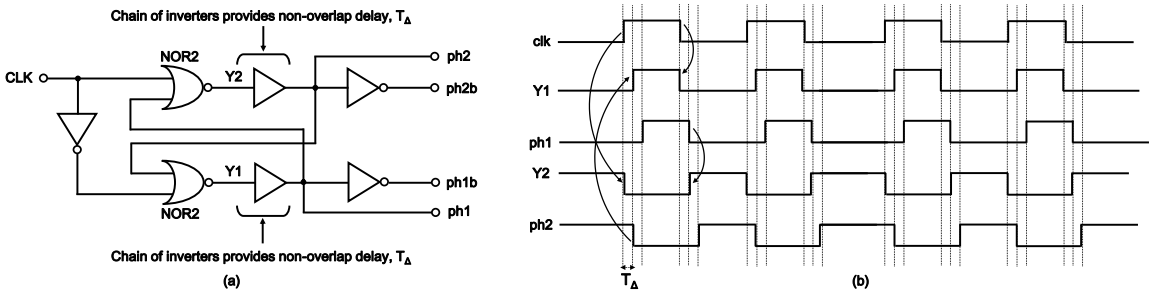

Figure 6.16: The two-phase non-overlap clock generation circuit (a), and its timing diagram (b).

As previously mentioned, the Δ-Σ modulators need two non-overlaping clocks. The circuit diagram of the non-overlaping clock generation circuit is shown in Fig. 6.16(a), and its timing diagram is shown in Fig. 6.16(b). The circuit presented here for the two phase non-overlaping clock generation is very common in delta-sigma modulator, and can be found in reference [77].

6.6 LAYOUT AND FABICATION

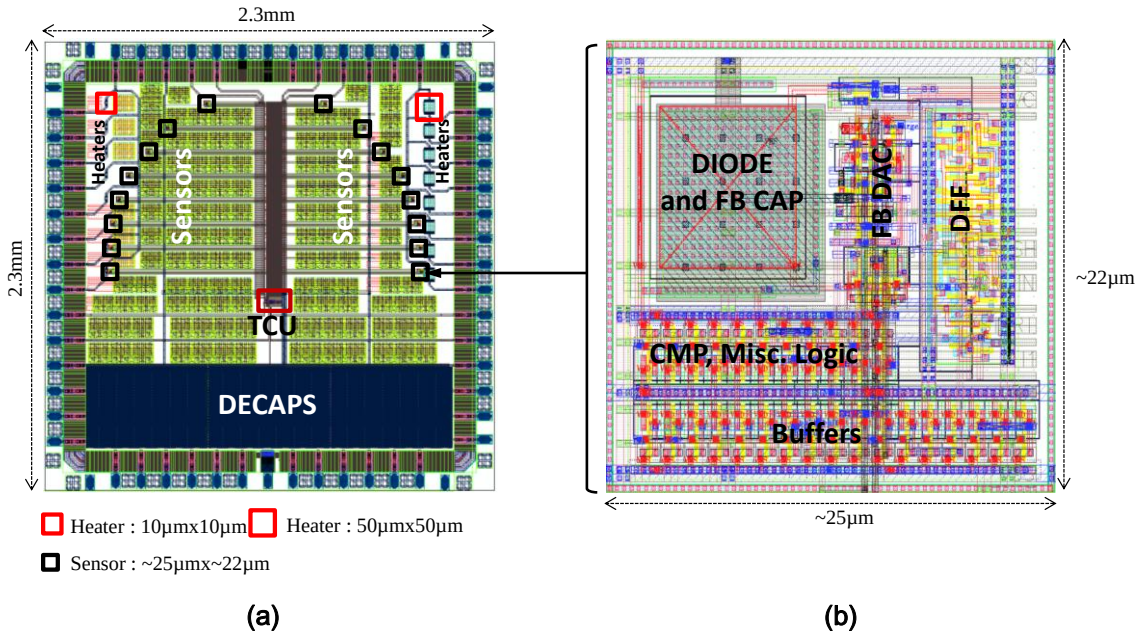

Figure 6.17: The layout of the chip (a), and layout of one Δ-Σ Modulator sensor (b).

The layout of the chip, and one of the temperature sensor, implemented in a TSMC 180nm CMOS process, are shown in Figs. 6.17(a) and (b), respectively. At the bottom of the chip the empty space were filled with MOSCAPs (DECAPS) to filter out the noise of the power supply. As mentioned earlier, in the layout the metal cap for the feedback DAC were placed on the top of the diode to save silicon space.

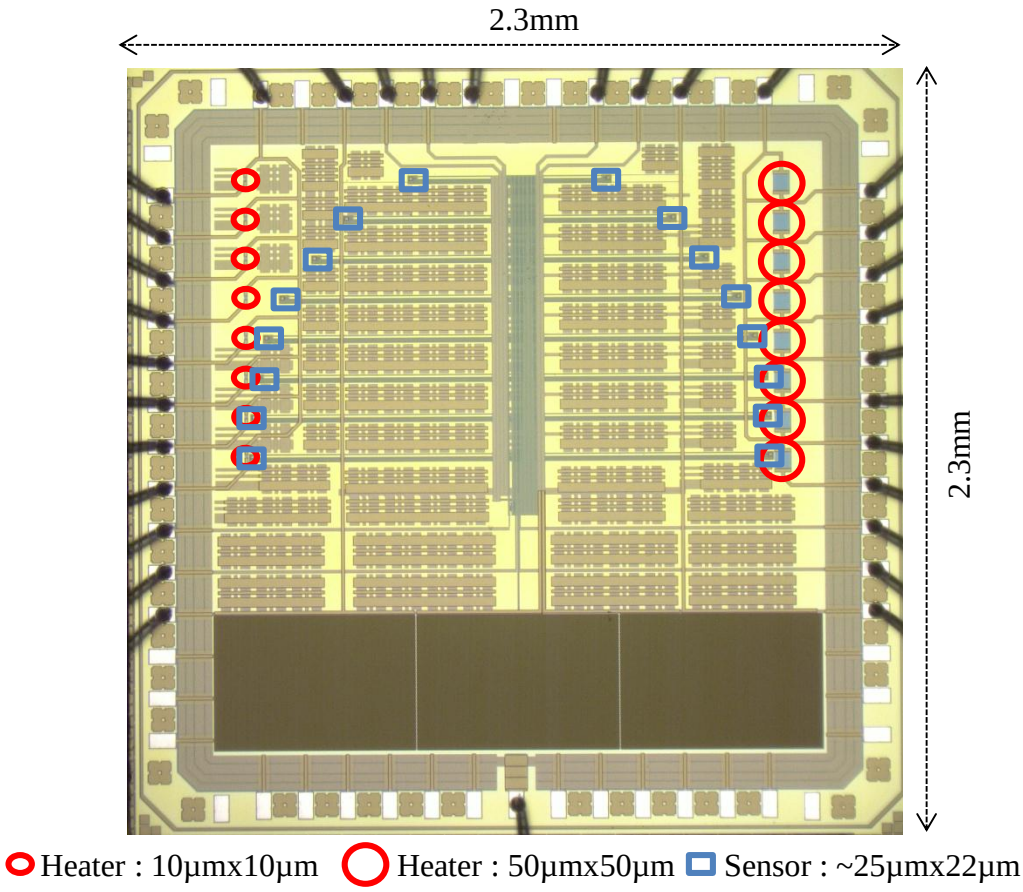

Figure 6:18: Chip micrograph.

The micrograph of the chip is shown in Fig. 6:18. The chip occupies an area of about 2.3mm by 2.3mm, and a total of 16 Δ-Σ modulator sensors were placed in the chip. Each sensor occupies an area of ~25µm by ~22µm, and consumes ~4µW including all the circuitry shown in Fig. 6.4 from a single 1.8V supply.

6.7 SIMULATION RESULTS

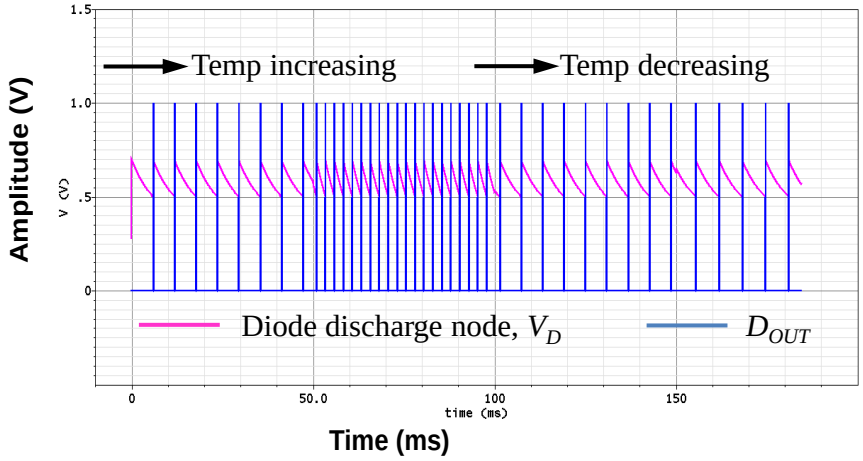

Figure 6.19: Simulation results showing 1-bit data and diode discharge voltage V_D at different temperatures.

The Δ-Σ modulator was simulated at different temperatures to see the temperature effects on the discharge of the diode, and 1-bit data pattern. As the temperature of the chip increases, the diode reverse-bias current increases which causes the diode to

discharge faster. As a result more pulses of 1-bit data are seen at the output of the modulator. This is shown in Fig. 6.19.

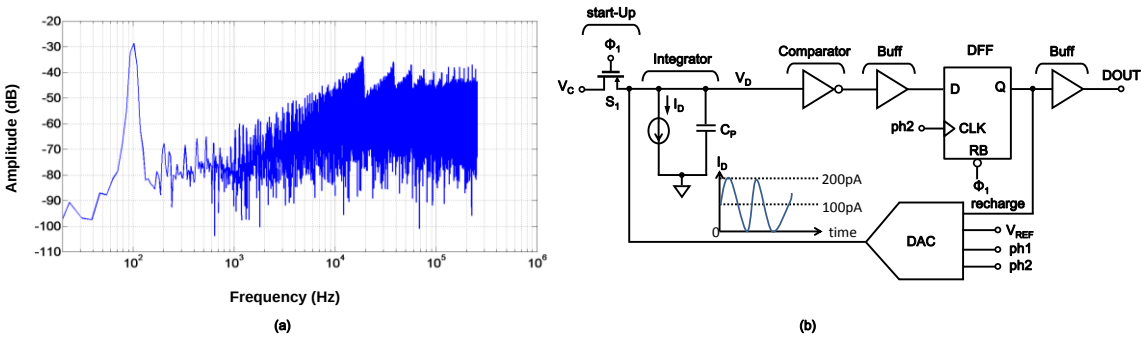

Figure 6.20: Simulation results showing FFT of 1-bit data, (a), and simulation test setup with the diode replaced with a sine wave current, (b).

Next, the modulator was simulated according to the setup shown in Fig. 6.20(b). Here, the diode was replaced with a 100Hz sinusoidal current of 100pA peak amplitude, and a 100pA DC offset such that the total current never changes polarity. Normally, a data converter is characterized with a sine wave input to find out its noise behavior, and SNR. The FFT of Fig. 6.20(a) shows the signal lobe at 100Hz, followed by typical noise shape. These simulation results confirm the behavior of the proposed first-order Δ-Σ modulator. However, simulation also shows tones which are typical in a first-order Δ-Σ modulator with a DC input [71]-[72].

6.8 POST-SILICON MEASURED DATA

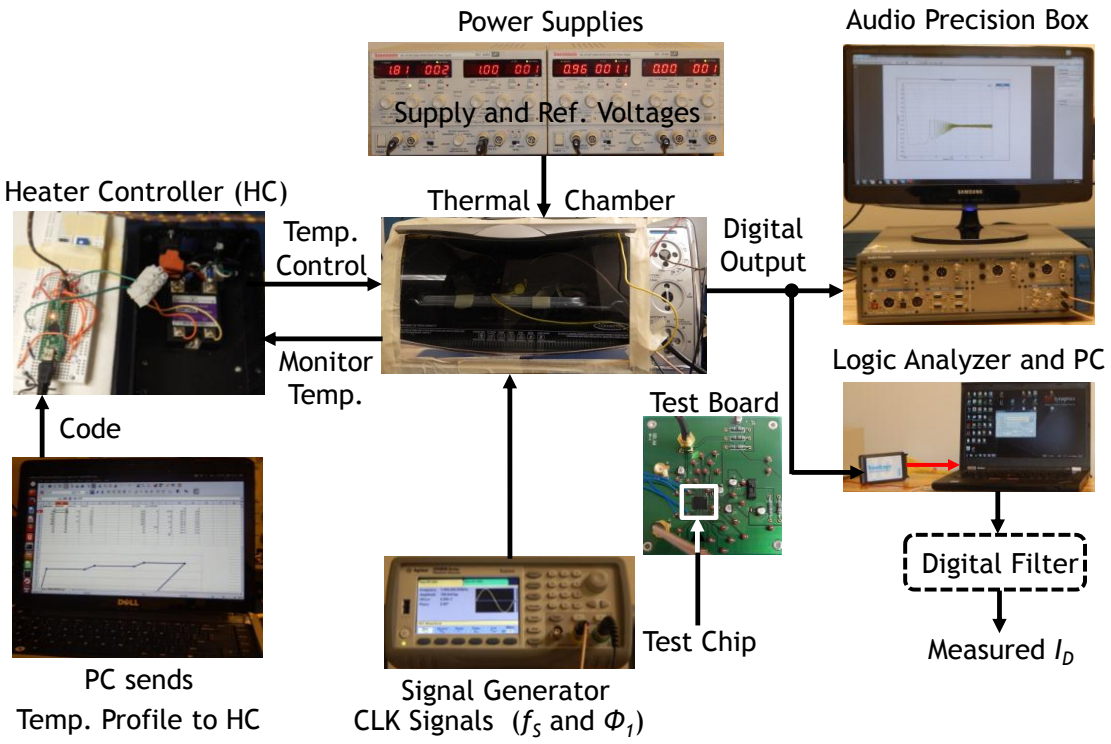

Figure 6.21: Measurement setup.

The measurement setup to characterize the Δ-Σ modulator sensors of the chip is shown in Fig. 6.21. During the measurement, V_C = 1.0V, V_{TH} = 0.9V, V_{REF} = 1.0V, and V_{DD} = 1.8V were applied from external sources to the modulators. The sampling CLK of 100 KHz was applied externally. The modulators were periodically reset with the reset frequencies Φ_1 = 0.5Hz, 1.0Hz, and 2.0Hz. A total of 16 modulator sensors were measured. The test board was placed inside the thermal chamber (heater), and temperature was applied from 30^0C to 100^0C with a step of 5^0C. Thus, for each modulator sensor 15 temperature data were collected for multiple cycles of Φ_1. The

collection of data for multiple cycles of Φ_1 was necessary to calculate the average, and standard deviation of the diode current using the external digital filter. The 1-bit digital data of the modulators were collected with a logic analyzer, and downloaded into a PC. Occasionally, some data were collected using an Audio Precision Box (AP Box). The Audio Precision Box is an excellent tool to characterize data converters, especially Δ-Σ data converters, for audio applications.

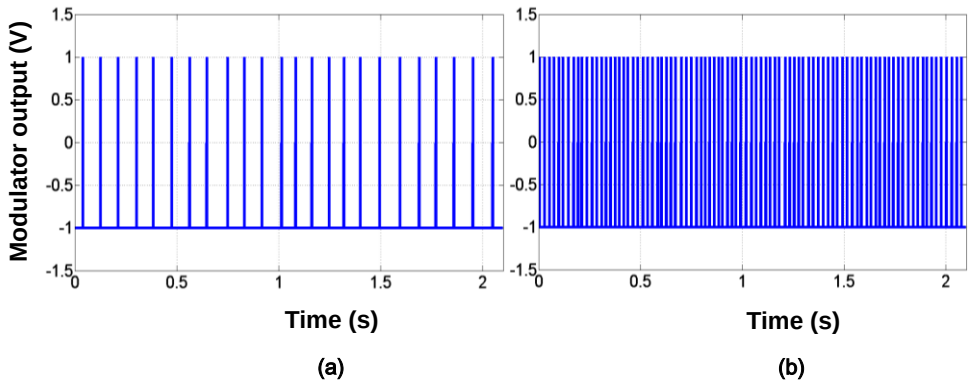

Figure 6.22: Simulation results showing 1-bit digital output of the modulator at 30^0C (a) and at 50^0C (b).

The 1-bit digital output of a modulator, collected using the AP Box, is shown in Fig. 6.22. The data was collected at two temperatures, 30°C and 50°C. The AP Box's internal software interprets data low as -1.0, and data high as +1.0 as opposed to 0 and 1 interpreted by the logic analyzer. These data were collected for an active phase time window of Φ_1. As temperature increases the diode reverse-bias leakage current increases, as a result the diode discharges faster creating more pulses at the output of the modulator during the same time.

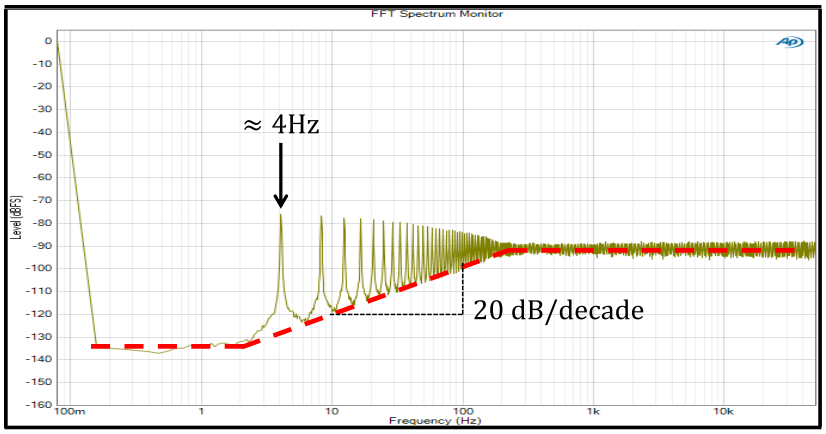

Figure 6.23: FFT spectrum of the 1-bit data at 30^0C with no dither applied.

The FFT spectrum of the 1-bit digital data of Fig. 6.22(a) for 30°C is shown in Fig. 6.23. First of all, the FFT shows the typical Δ-Σ noise shape with 20dB/decade as expected for a first-order modulator with a single pole at its STF as shown in Equation (5.6). Second, the data pattern is almost fixed due to the fact the modulator has little noise to break down the almost fixed pattern of the 1-bit data. As a result, the FFT shows tones, the first fundamental of the tone appears at about 4Hz. If a digital filter is used to filter out the out of band noise, then the bandwidth of the filter must be well below 4Hz. Otherwise, a significant amount of distortions will appear at the output of the filter. A small amount of dither can be applied to the modulator to remove the tones. It is important to mention here that, the FFT plots of Figs. 6.23, 6.24, and 6.25 were taken using the Audio Precision Box shown in Fig. 6.21.

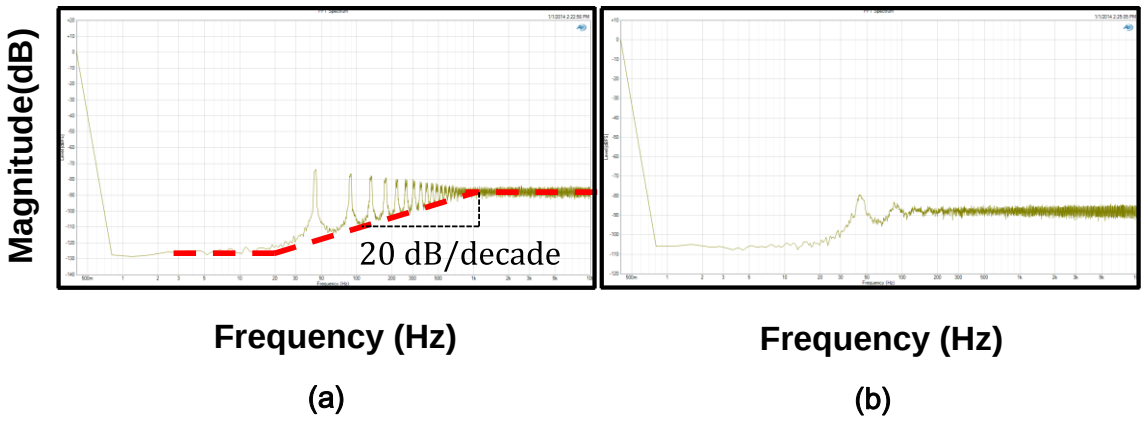

Figure 6.24: FFT spectrum of the 1-bit data at 50^{0}C with no dither applied (a), and with 10mV dither applied (b).

The FFT spectrum of the 1-bit digital data of Fig. 6.22(b) for 50°C is shown in Fig. 6.24(a) when no dither is applied, and (b) shows the same with a 10mV dither applied. If the temperature is increased further, then the tones will move further into higher frequencies. It is clear, that the bandwidth of the digital filter has to be set by the tonal behavior of the modulator at the lowest operating temperature. The FFT of 1-bit data at 100°C with and without dither is shown in Fig. 6.25. The fundamental tone is pushed out further at higher frequency.

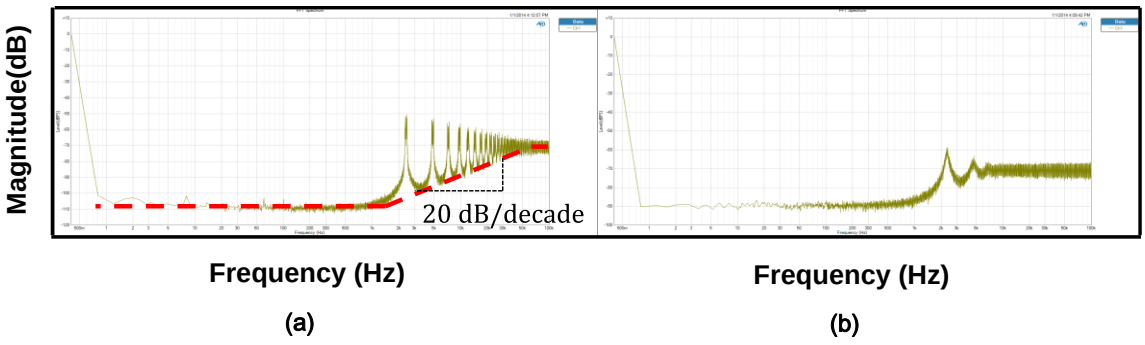

Figure 6.25: FFT spectrum of the 1-bit data at 100^0C with no dither applied (a), and with 10mV RMS dither applied (b).

6.8.1 Selecting the bandwidth of the Digital Filter

Due to the presence of harmonic tones the digital filter to be implemented externally must be designed carefully such that such that no tones fall within the bandwidth of the filter for any of the sensors placed across the die. Otherwise, the measurement of the diode current will be very much corrupted. After characterizing the 16 different sensors placed across the chip, it is found that the filter of the bandwidth must be well below 4Hz.

As shown in Fig. 6.23, the FFT spectrum of the 1-bit data pattern shows harmonic tones with the fundamental at ~4Hz. This is the lowest frequency of fundamental tone seen among all the 16 sensors characterized. As such the bandwidth of the digital filter was chosen 2Hz in this implementation. The FFT spectrum of Fig. 6.23 shows that the noise floor around the tones is raised up. This behavior of tones at the lower frequency is the reason for not having a flat noise floor at the lower frequencies. As the temperature of the chip is increased, the tones of the 1-bit data move at higher frequencies, this causes

the noise floor to be flat at the low frequencies, as seen in the FFT diagrams of Fig. 6.24 for 50°C, and Fig. 6.25 for 100°C. As a result the current measurement using the filter is expected to have some extra noise at the lower temperatures.

6.8.2 Measurement of Diode Current

	Reset Rate 0.5Hz		Reset Rate 1Hz		Reset Rate 2Hz	
temp (^{0}C)	currents (pA)	sigma (fA)	currents (pA)	sigma (fA)	currents (pA)	sigma (fA)
30	0.3552	30.4	0.3534	33.8	0.3523	44.7
35	0.5102	19.8	0.5102	19.7	0.5084	19.4
40	0.8304	5.9	0.8305	6.9	0.8265	10
45	1.1877	13.3	1.1875	13.7	1.1959	12.6
50	1.7599	6.9	1.738	5.7	1.7312	4.5
55	2.5381	5.2	2.5271	9.3	2.5214	8.1
60	3.5269	6.9	3.5218	7.64	3.518	7.8
65	5.6917	9.65	5.667	10.39	5.6559	11
70	8.2003	10.8	8.2329	10.36	8.205	9.9
75	11.84	18.6	11.6965	13.55	11.6052	15.4
80	19.4411	32.95	19.318	33.61	19.0863	30.4
85	27.4567	58.65	27.5904	58.19	27.3319	56.1
90	39.051	75.85	39.7303	71.35	39.7829	74.4
95	63.4885	90.65	64.472	114.34	65.2285	86.1
100	93.2314	131.2	92.594	121.83	92.5501	125.7

Table 6.2: Diode leakage currents and standard deviations (sigma) of a sensor.

A total of 16 sensors were characterized over the temperature range of 30°C to 100°C with a 5°C step. As an example, Table 6.2 above shows the raw data of a sensor for the diode leakage currents, and standard deviations (sigma) of the currents. The sensor was characterized for three different reset rates, 0.5Hz, 1.0Hz, and 2.0Hz. Fig.

6.26(a) shows the profile of this diode current, and Fig. 6.26(b) shows the profile of the standard deviations of the current. The current profile is exponential as expected according to Equation (4.2).

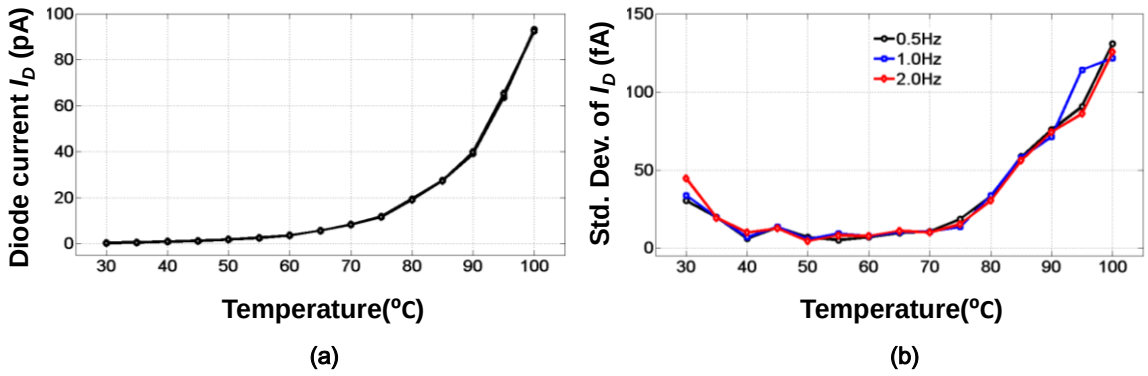

Figure 6.26: The profile of diode leakage current, I_D, (a) and standard deviations of I_D (b) for three different reset rates, 0.5Hz, 1.0Hz, and 2.0Hz.

The standard deviation (sigma) of the current is essentially the noise of I_D. The noise starts little higher at low temperature (30°C), as shown in Fig. 6.26(b). This is because at this low temperature the effect of the first fundamental tone raises up the noise floor little bit, as explained before. Also at lower temperatures, due to lack of enough pulses, the noise does not get averaged out much by the digital filter. Then the noise essentially flattens out for all three reset rates, and stays relatively flat between 40°C-70°C, after which the noise shows an increasing pattern. Ideally, the noise should be the same for all three reset rates. However, as the temperature increases the shot noise, and thermal noise from the capacitive switching also increases. Quantization noise does not vary with temperature. The overall pattern of the noise is also exponential like the pattern

of I_D. The following section addresses the different types of noise sources, and their contributions to the noise of I_D.

6.9 SOURCES OF NOISE IN THE SENSOR

The main sources of the noise in this Δ-Σ modulator based sensor are the quantization noise, shot noise, and thermal noise (kT/C noise). This section gives a brief description of these noise sources and their contributions to the noise at the output current measured.

6.9.1 Quantization Noise

Like in any A/D converter the Δ-Σ modulator here has quantization noise. The quantization noise current in the context of this modulator is determined with a 2Hz bandwidth (f_B) of the digital filter. The oversampling ratio of the digital filter is $f_S/2f_B$ = 25K, for a sampling rate of f_S = 100KHz. The number of samples obtained within the active window of the reset pulse is

$$number\ of\ samples = f_S \cdot \left(\frac{duty\ cycle}{f_{Reset}}\right), \tag{6.7}$$

Where, f_{Reset} is the frequency of the reset pulse Φ_1 applied, If all of these samples were all ones, then based on Equation (6.6),maximum possible current is given by

$$f_S \cdot \left(\frac{duty\ cycle}{f_{Reset}}\right) \cdot C_P \cdot VDD \cdot f_{Reset} = f_S \cdot (duty\ cycle) \cdot C_P \cdot VDD, \tag{6.8}$$

Thus, the quantization noise for the current I_D measured at the output can be defined as

$$Q_N(I_D) = \frac{f_S \cdot (duty\ cycle) \cdot C_P \cdot VDD}{\left(\frac{f_S}{2f_B}\right)}, \tag{6.9}$$

Finally, the quantization noise becomes

$$Q_N(I_D) = (duty\ cycle) \cdot C_P \cdot VDD \cdot 2f_B. \tag{6.10}$$

Thus, following Equation (6.10) above, the theoretical quantization noise, for an estimated C_P = 30fF, and power supply V_{DD} = 1.8, becomes

$$Q_N(I_D) = (0.95) \times (30 \times 10^{-15}) \times (1.8) \times 2 \times 2 \approx 200fA, \tag{6.11}$$

During measurements, to allow enough time for data collection a 95% duty cycle clock was applied to the chip for the reset clock Φ_1.

6.9.2 Diode Shot Noise

Shot noise arises from the random generation of carriers through a *p-n* junction, and the power density of the shot noise (A^2/Hz) in a reverse-bias *p-n* junction is given by [55],[123]

$$S_{shot}^2 = 2qI_D. \tag{6.12}$$

Where, q is the electronic charge (1.6×10^{-19} Qulomb), and I_D is the diode reverse leakage current. The RMS shot noise (A/Hz) is given by

$$n_{shot} = \sqrt{2qI_Df}. \tag{6.13}$$

Where, f is the frequency in Hz. While quantization noise is a fixed noise, the RMS shot noise defends on square-root of the current I_D. So, the shot noise pattern is expected to look like the pattern of I_D, which is exponential.

6.9.3 Reset Noise

Every time the switch S_1 opens after resetting the modulator it injects a noise into the modulator. At the end of each reset this noise is sampled by C_P, and its RMS value is given by $\sqrt{kT/C_P}$ V, where k is the Boltzmann constant, and T is the temperature in ºK.

6.9.4 Feedback Noise

Every time the feedback DAC recharges the diode junction capacitance it injects a noise into the modulator. The RMS noise due to DAC capacitor switching is $\sqrt{kT/C_{DAC}}$, V. DAC capacitor injects a noise into the modulator through charge sharing, the power of which is given by

$$noise_{DAC}^2 = \left(\frac{kT}{C_{DAC}}\right)\left(\frac{C_{DAC}}{C_{DAC}+C_P}\right)^2, \tag{6.14}$$

If the DAC switches n number of times during one active phase of Φ_1, then it will inject the same thermal noise *n* times, and treating them uncorrelated, the total DAC noise power injected into C_P can be given by

$$noise_{DAC}^2 = n \cdot \left(\frac{kT}{C_{DAC}}\right)\left(\frac{C_{DAC}}{C_{DAC}+C_P}\right)^2. \tag{6.15}$$

Assuming, the noise sources are uncorrelated, the total RMS value of capacitive thermal noise from the reset and feedback noise sources is given by

$$noise_{cap} = \sqrt{\frac{kT}{C_P} + n \cdot \left(\frac{kT}{C_{DAC}}\right)\left(\frac{C_{DAC}}{C_{DAC}+C_P}\right)^2}. \tag{6.16}$$

In this design, $C_{DAC} \approx 100fF$, C_P is estimated as ≈ 30fF, so the total noise at room temperature becomes about 400μV for n = 1. The capacitor C_P will experience this noise during its discharge. The sensors have been characterized for a discharge voltage of 75mV, this 400μV of noise very small in comparison. However, as the temperature increases the output of the modulator will have more pulses during the same active window of Φ_1. That means, the DAC will be injecting more noise at the input of the comparator. Thus, at higher temperature the DAC feedback noise is expected to increase.

	Reset Rate 2Hz			
temp (^{0}C)	currents (pA)	sigma (fA)	Shot noise (fA)	Total noise (fA)
30	0.3523	44.7	0.4748	44.7025
35	0.5084	19.4	0.5704	19.4084
40	0.8265	10	0.7273	10.0264
45	1.1959	12.6	0.8749	12.6303
50	1.7312	4.5	1.0526	4.6215
55	2.5214	8.1	1.2703	8.1990
60	3.518	7.8	1.5005	7.9430
65	5.6559	11	1.9026	11.1633
70	8.205	9.9	2.2915	10.1618
75	11.6052	15.4	2.7253	15.6393
80	19.0863	30.4	3.4950	30.6002
85	27.3319	56.1	4.1824	56.2557
90	39.7829	74.4	5.0459	74.5709
95	65.2285	86.1	6.4611	86.3421
100	92.5501	125.7	7.6962	125.9354

Table 6.3: Diode shot noise and total noise for the modulator of Table 6.2.

The effect of the shot noise can be looked at with an example. From the diode currents presented in Table 2, the shot noise can be calculated according to Equation (6.13), and it is shown in the Table 6.3 above. Also shown is the total noise which was calculated from the standard deviation (sigma) of I_D and shot noise assuming they are uncorrelated. The pattern of the shot noise for this modulator is shown in Fig. 6.27.

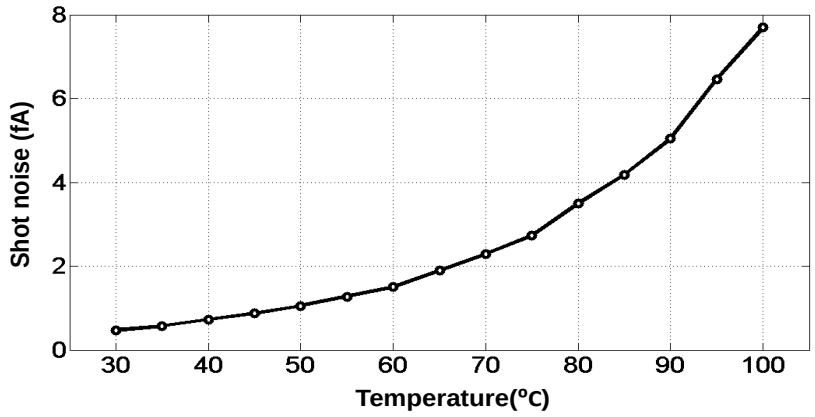

Figure 6.27: Diode shot noise for the modulator of Table 6.2.

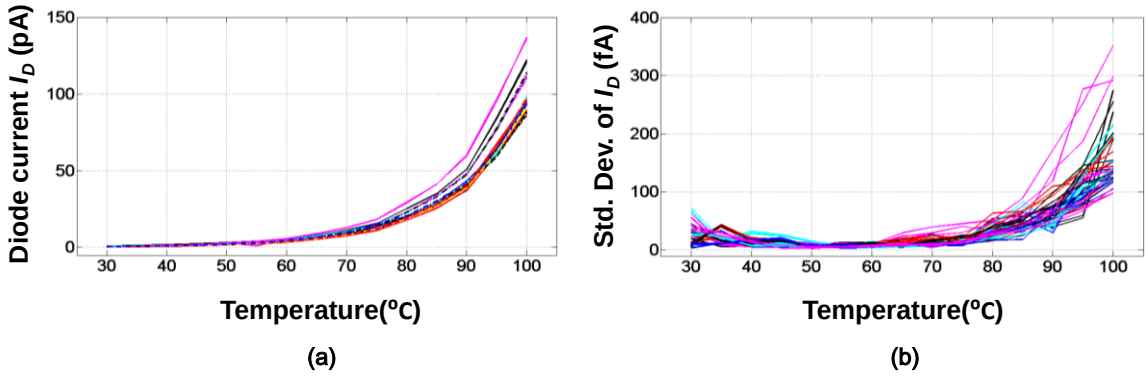

Figure 6.28: Diode currents I_D (a), and their sigma (noise) values (b), for all 16 sensors measured.

Measured diode currents and their standard deviations (sigma) for all 16 sensors measured are shown in Fig. 6.28(a) and (b) respectively. Each sensor was characterized for three reset rates, 0.5Hz, 1.0Hz, and 2Hz. There are three plots for the three reset rates for each sensor. So, there are total 48 plots in each of the Figs. 6.28(a) and (b). The noise of the currents were evaluated with the externally implemented digital filter with a bandwidth fixed at 2Hz. From the measured data, it is seen the Δ-Σ modulator based

design can determine diode temperature dependent reverse-bias leakage current with a very high accuracy.

6.10 INACCURACY OF TEMPERATURE MEASUREMENTS

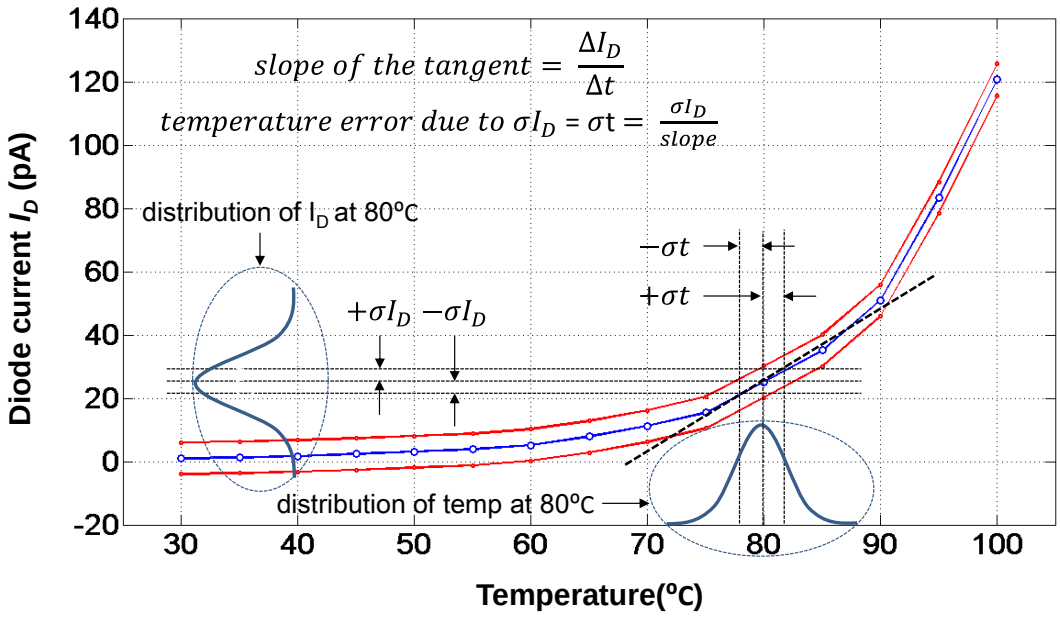

Figure 6.29: Measurement of inaccuracy of temperature.

From Fig. 6.28 it is expected that the high accuracy of current measurement at the output of the Δ-Σ modulator based sensor can be used to measure on-chip temperature very accurately. Assuming a normal distribution of measured I_D with the standard deviations, σI_D, as shown in Fig. 6.28, the inaccuracies of temperature measurement can be measured as shown in Fig. 6.29. In this figure, the blue curve shows measured I_D, and the two red curves show $I_D \pm \sigma I_D$. In order to show the three curves clearly σI_D is heavily exaggerated here. As an example, σI_D of I_D at 80^0C is mapped to a standard deviation of

temperature, σt. The σt is the inaccuracy of temperature measurement. If a tangent is drawn at the I_D curve at 80^0C, then the inaccuracies of temperature, σt, can be calculated as

$$\sigma t = \frac{\sigma I_D}{\text{slope of the tangent}}. \tag{6.17}$$

Thus from σI_D, and slope of the tangent at every temperature, the inaccuracies of temperature measurement are calculated according to Equation (6.17).

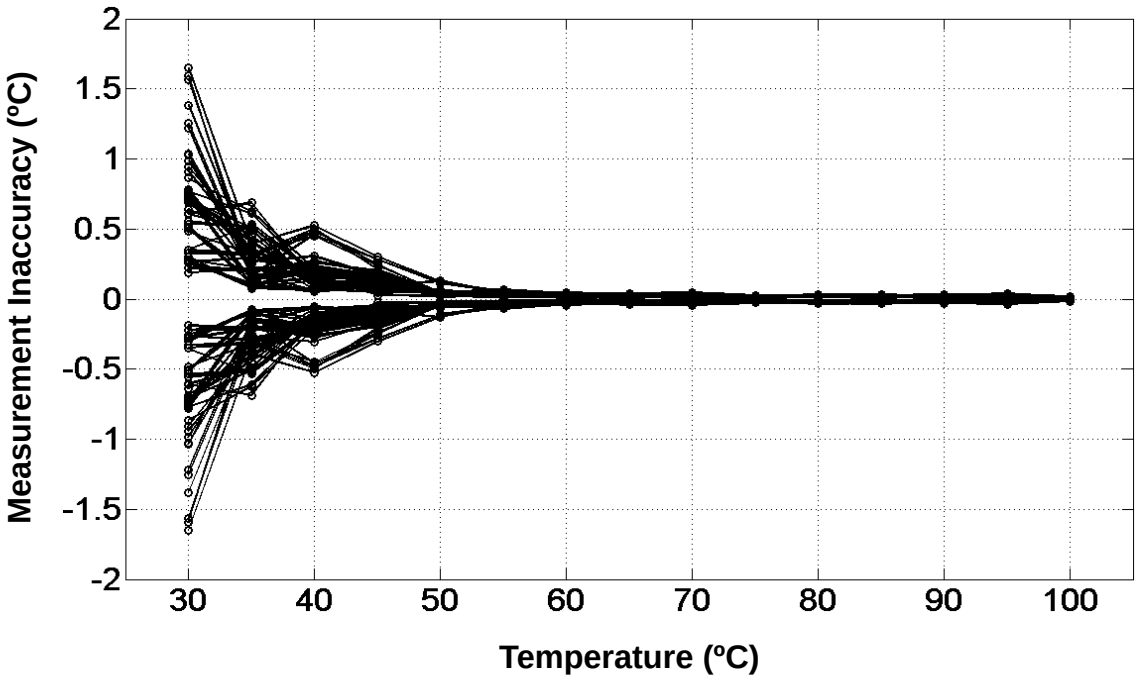

Figure 6.30: Measurement inaccuracy vs. temperature for 16 different sensors.

The measurement inaccuracies of temperatures with one sigma of I_D ($\pm\sigma I_D$) are shown in Fig. 6.30. This figure shows the inaccuracies of all 16 sensors for the reset rates of 0.5Hz, 1.0Hz, and 2.0Hz, and over the temperature range of 30°C - 100°C. At the lowest temperature of 30°C due to lack of enough pulses the noise was not averaged out much. Also, as demonstrated earlier some of the sensors have tones around 4Hz, and they contributed some extra noise. Due to these, the inaccuracies at the lowest temperature are higher. However, as temperature is increased the averaging helps to reduce the noise, and also the tones are moved is higher frequencies. As such, the inaccuracies go down at higher temperatures.

It is important to mention here that, the sensors are expected to measure higher temperatures more accurately so that the chip can take corrective measures to protect it from overheating. From the measured results shown in Fig. 6.30 it is evident that the proposed Δ-Σ modulator based sensors can meet this goal sacrificing some accuracy of measurement at lower temperatures.

Chapter 7: Summary and Future Works

7.1 SUMMARY

This research demonstrates a new technique of on-chip temperature measurement by utilizing the temperature dependent reverse-biased leakage current of a *p-n* junction diode as the operand for temperature. In order to prove the concept, and applicability of this new technique, the theory, and mathematical modeling of the concept behind this new technique have been presented followed by successful design and implementation of on-chip temperature sensors.

The temperature sensor successfully designed, and developed in this research is suitable for ultra-low power application where the physical size of the sensor needs to be also very small. The specific application that is targeted in this research is large SoCs, like multi-core microprocessor, where many temperature sensors need to be placed on the same chip. Thus, they need to very small in size so that they can be placed in the closest proximity of all possible hot spots, and also their power consumption needs to be very low.

To prove the theory and concept, at first a time-to-digital converter based temperature sensor was designed, and fabricated in GlobalFoundries 32nm SOI CMOS technology. The theory, design, fabrication, and post-silicon experimental results of this sensor were presented in Chapter 4. The measured data from the fabricated chips and their comparison from recently developed sensors show promising results. This sensor

occupies an area of ~39µm by ~27µm (about 0.001 mm^2), and it consumes about 100µW from a single 1.65V supply.

Next, a first-order delta-sigma modulator was implemented in TSMC's 180nm CMOS Bulk technology, where the *p-n* diode, along with its junction capacitance, was used as a continuous-time integrator. In this implementation, the temperature dependent diode reverse-biased current of the diode was measured from the 1-bit digital data of the modulator by implementing an off-chip digital filter. The measured diode current, and the noise ratio demonstrate that such a modulator can be utilized to measure the temperature dependent diode current.

In this implementation, a total of 16 modulators were placed on the same chip. The digital outputs of the modulators were measured one at a time with a 4-bit select mux which was designed and implemented on the same chip. Thus, this implementation requires only one off-chip digital filter to process outputs of the modulators to measure the diode currents and their standard deviations in each one of them. The measurements were carried out over the temperature range of 30^0C-100^0C, and multiple cycles of measurements were taken at each temperature. From the measured diode currents and standard deviations the inaccuracies of temperature measurements were calculated. The sensors developed here show very low inaccuracy at higher temperature above 30^0C while the inaccuracies increase at and below 30^0C.

The modulator implemented in this research occupies an area of ~25µm by ~22µm (about 0.0005 mm^2), and its worst case power consumption, from a single 1.8V supply, is about 4µW. The ultra-small size, and extremely low power consumption of

this modulator makes it the perfect choice for implementing a complete thermal monitoring system in a large SoC, like today's multi-core microprocessor.

7.2 SUGGESTIONS FOR FUTURE WORKS

In order to develop a complete and comprehensive on-chip thermal monitoring system, the following suggested works can also be designed, and developed on-chip.

7.2.1 On-Chip Digital Filter

The digital filter utilized off-chip in this research, can be designed and developed on chip. This is a completely digital circuit that requires simple accumulator (adder), and latches. In today's sub-micron digital technology such a digital circuit can be developed in small geometry. Moreover, in the system level approach presented in this research, the outputs of the sensors placed on the same chip can be read serially, and thus they can be processed by one digital filter. As a result, only one filter needs to be implemented on-chip, and it will not drastically increase the size of the overall thermal monitoring system.

7.2.2 On-Chip Look Up Table

An on-chip look up table can store the measured current profile as a function of temperature of the diodes in the sensors, and this can be done for all diodes in all the sensors one time at production. Then, during the operation of the chip, the thermal

monitoring system can read the digital data of the sensors, process them with the digital filter to measure the diode current, and finally use the look up table to report the temperature of the chip to the processor. In microprocessor, there exists numerous look up table for various applications. Thus, adding one for temperature measurement should not be a burden for the architects and designers.

7.2.3 Use Larger Diode to Increase Speed and Accuracy

The sensor developed in this research exhibits slow response time at lower temperatures, at and below 30^0C. This is due to the fact that the reverse current of the tiny *p-n* diode, of 10μm by 10μm used in this sensor, is extremely low at these low temperatures. The extremely low diode current produces very few pulses at the output of the modulator which does not contribute much averaging to reduce noise. For this reason, the noise in current measurement is also high at these low temperatures.

A bigger diode can be used to increase diode current which is expected to increase both the response time and the accuracy of current measurement at the output of the modulator. The overall area of the sensor with a bigger diode should still be small enough to support on-chip temperature measurement of microprocessors by deploying them in the closest proximity to all possible hot spots.

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